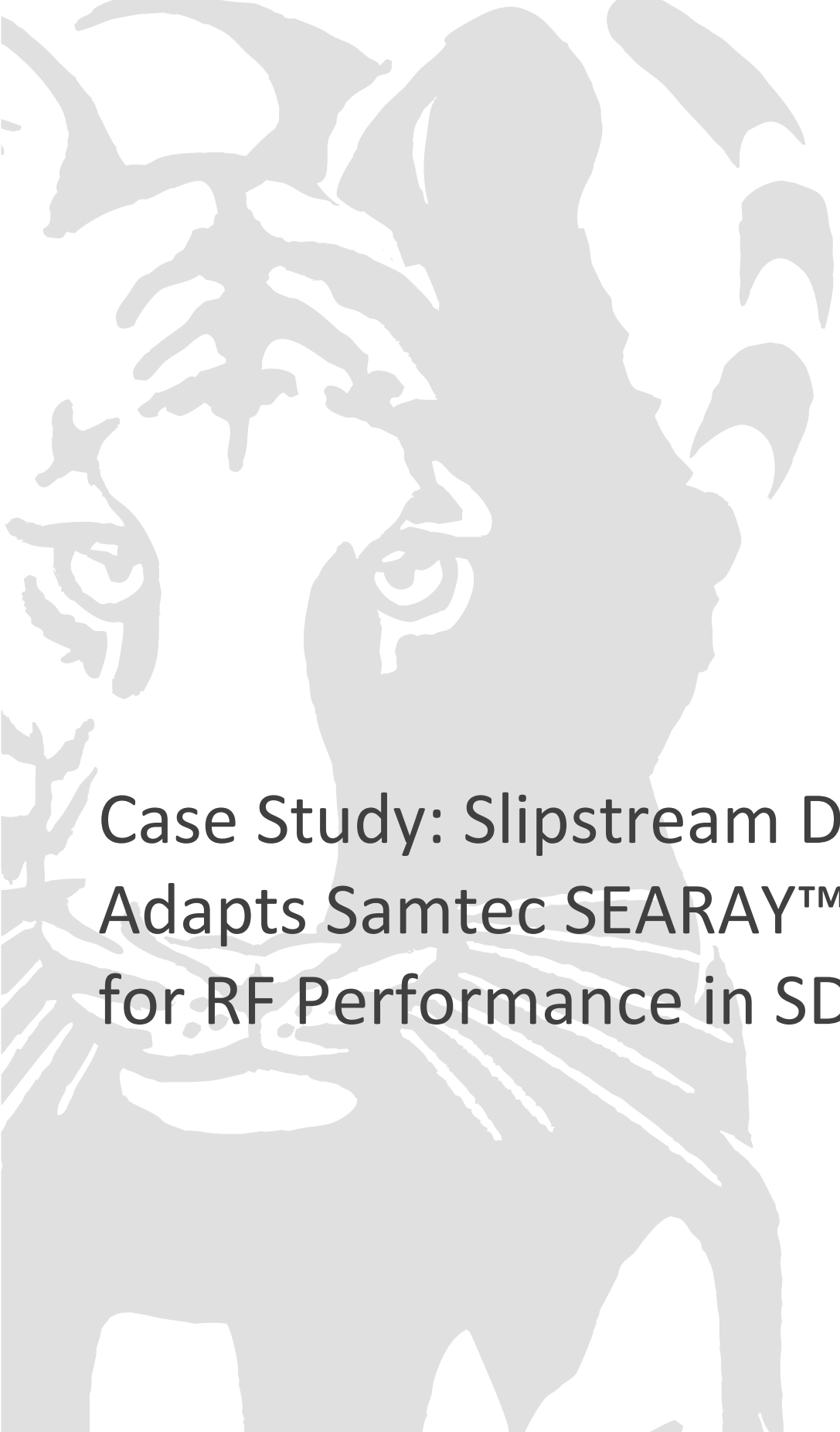

Case Study: Slipstream Design Adapts Samtec SEARAY™ connectors for RF Performance in SDR

October 2025

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Introduction

Software-defined radio (SDR) requirements are starting to exceed the performance capabilities of many traditional RF components. This challenge invites RF system architects to select connectors that were originally designed to meet the demanding signal integrity specifications of high-speed digital applications. This case study details how designers at Slipstream Engineering Design Ltd. (Slipstream) used Samtec SEARAY™ connectors with a customized PCB launch (connector to board transition) to achieve the necessary RF performance for their next-generation modular ASTRO™ card solution for SDR. Samtec refers to this approach as Analog over Array™ technology.

The Design

An SDR platform offers functional flexibility and adaptability through reconfigurable hardware. The Slipstream approach uses RFSoC devices that incorporate multiple RF channels in a compact PCIe® and VPX form factor. Their modular approach to system design incorporates RF cards that are application and frequency specific. These cards can be plugged into the Slipstream digital hardware platform to create a customized SDR platform. The compact, multi-board, SDR platform uses a dual-slot PCIe form factor and a high-density interconnect (HDI) approach.

Figure 1 illustrates the generic ASTRO SDR platform, incorporating an 8-lane PCIe carrier card. The application specific RF Front-end (RFFE) card incorporates 8 transmit 8 receive (8T8R) channels and is designed to operate in the 5G NR N78 and N77u bands (3.4-4.2 GHz). The ASTRO SDR platform allows for the RFFE board to be a plug-and-play module that can be swapped depending on the application of interest. In addition to the SEARAY connectors, the platform also includes Samtec Magnum RF® connectors to route the 8 Tx/Rx signals and some clock signals to the front panel. Slipstream engineers selected the Magnum RF connectors because they are ganged and miniaturized, which is beneficial for a very small form factor, as well as for their inter-channel isolation.

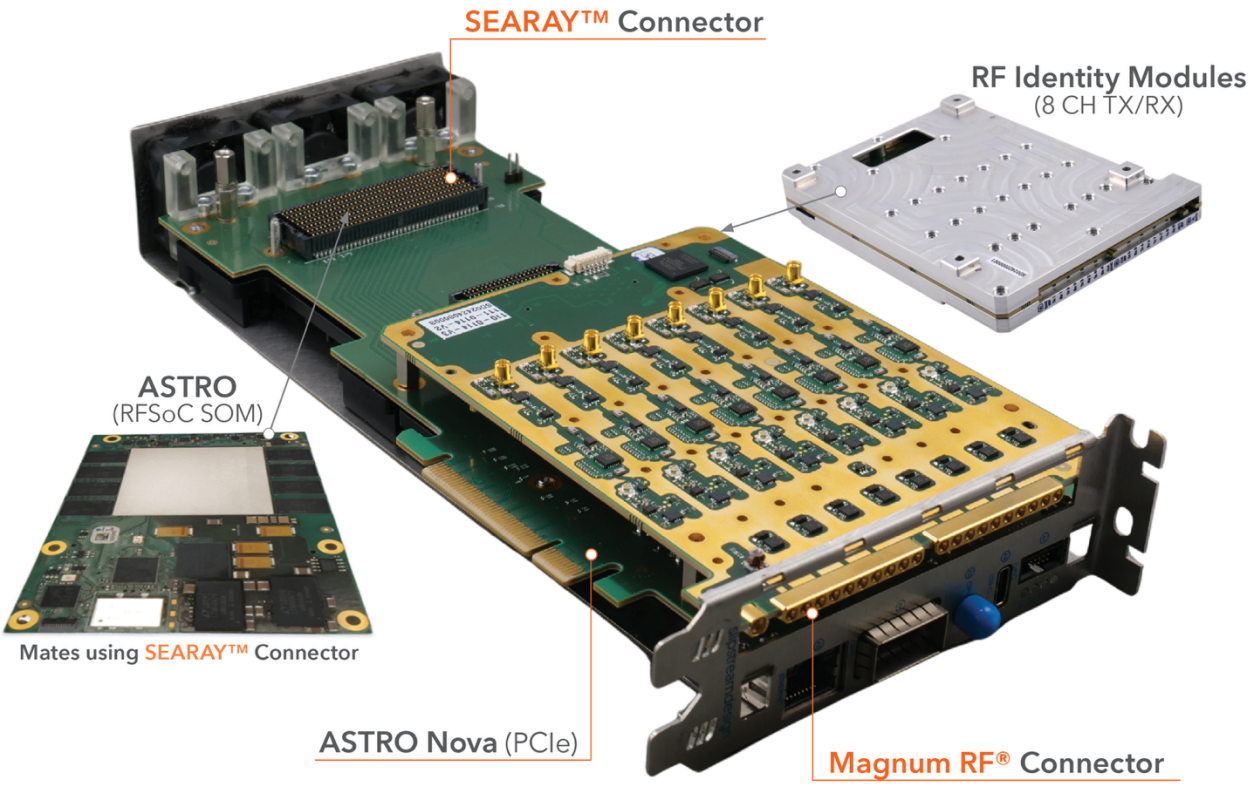


Figure 1: Slipstream's SDR platform includes the ASTRO card that houses a Gen 3 RFSoC and an 8T8R channel RFFE in a dual-slot PCIe form-factor. The ASTRO card uses the Samtec SEARAY connectors, and the carrier card is equipped with Samtec Magnum RF ganged connectors.

Overcoming Challenges

Routing the RF signals from the RFSoC device to the RFFE board through multiple connectors while maintaining return loss and crosstalk performance was the major design challenge.

To achieve the desired functionality, a high layer-count PCB with fine track widths and microvias was required. High-density field array SEARAY connectors were used in the multi-board transitions. These Samtec connectors are traditionally used for high-speed digital signal interconnections, but, in this implementation, they route RF signals up to 6GHz.

The differential traces from the connector were routed onto the internal layers to minimize losses due to radiation and to minimize crosstalk between channels (see Figure 2). The transitions to the internal layers are achieved using differential thru via and micro via structures. Since these differential via transitions form part of the connector-to-board launch, careful design of the region was required to minimize the effect of discontinuity and to preserve signal integrity.

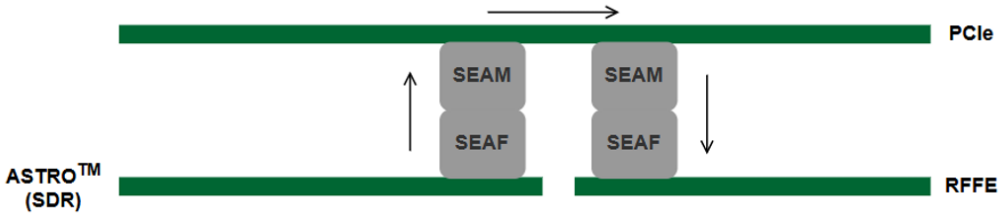


Figure 2 Multi-board connections using Samtec's SEARAY connectors.

The Slipstream team designed a test board for evaluation of this connector assembly. They also used Ansys HFSS to simulate a SEARAY SEAM-SEAF connector assembly with an 11 mm stack-up height using a 3D component model obtained from Samtec. Differential thru via and microvia structures were simulated separately and then incorporated with the connector pads to design an optimized PCB launch for the chosen PCB stack-up. The two models were simulated together to obtain the complete board-to-board performance. The target specifications are outlined in Table 1.

Table 1 Target specifications for connector-to-board transition

Maximum frequency of interest	6 GHz
Target impedance for the differential traces	100 Ω
Worst-case return loss	-20 dB
Maximum insertion loss	-0.5 dB
Crosstalk between channels	-60 dBc

The PCB stack-up and via definitions for the test board are presented in Figures 3 and 4. Microvias were used in this design to achieve the desired high-density interconnections. (Microvias are laser-drilled vias, typically of a smaller size than a thru hole via, that are used to connect adjacent layers in a PCB. Vertically aligned microvias are called stacked microvias and have been exploited in this work, as illustrated in Figure 4.) A finished 0.15 mm diameter thru hole with a pad size of 0.50 mm and a 0.15 mm diameter microvia with a 0.30 mm pad size were used in the design. Microvias were copper-filled, whereas the plated thru hole vias were resin-filled. Isola I-Tera MT40 was used as the substrate of choice as it is an FR4-based prepreg that is compatible with multi-layer processes. In addition, it has a well-controlled dielectric constant and low loss tangent making it suitable for RF applications.

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.02mm	4.1	
1	Top Layer		Signal	1oz	0.037mm		
	Dielectric 1	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
	Dielectric 2	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
2	L02_SIG/GND		Signal	1oz	0.037mm		
	Dielectric 3	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
	Dielectric 4	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
3	L03_SIG/GND		Signal	1/2oz	0.0175mm		
	Dielectric 5	I-Tera MT40 2X2116&3313	Core		0.45mm	3.45	0.02
	Dielectric 6	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
	Dielectric 7	I-Tera MT40 2X2116&3313	Core		0.45mm	3.45	0.02
4	L04_SIG/GND		Signal	1/2oz	0.0175mm		
	Dielectric 8	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
	Dielectric 9	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
5	L05_SIG/GND		Signal	1oz	0.037mm		
	Dielectric 10	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
	Dielectric 11	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
6	Bottom Layer		Signal	1oz	0.037mm		
	Bottom Solder	Solder Resist	Solder Mask		0.02mm	4.1	
	Bottom Overlay		Overlay				

Figure 3: 6-layer PCB stackup for the test PCB

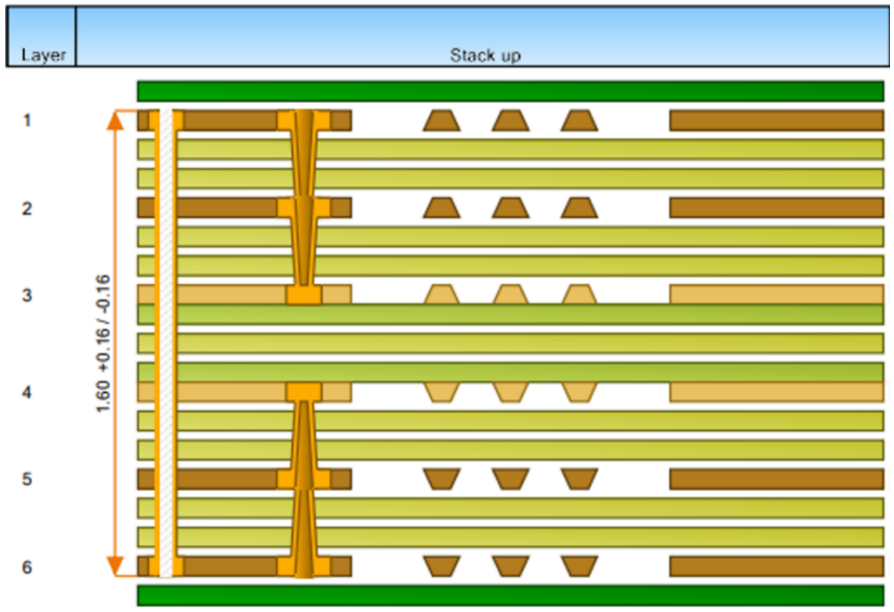


Figure 4: Via definitions for the test PCB showing thru hole plated via and stacked microvias used in the design.

Importance of Stackup Simulation

The connector launch must incorporate the connector pin pads, which are 0.64 mm in diameter and a pitch of 1.27 mm. Incorporating these pads with the differential via transitions has the effect of introducing additional capacitance to the launch area. Hence, a more inductively coupled via spacing is chosen for the connector launch to

compensate for the additional capacitance of the connector pads. A thru via spacing of 0.85 mm was chosen as a starting point for the connector launch design.

Samtec provided useful models and measurements to help create test simulations to gauge the suitability of their connectors.

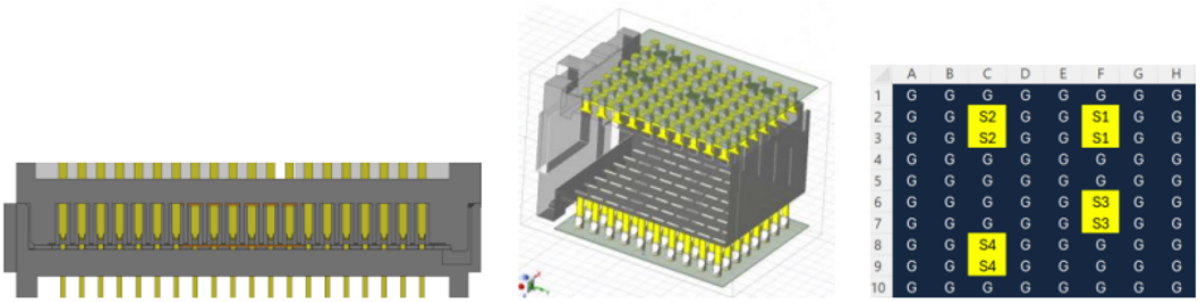


Figure 5: Mated view of the SEAX assembly, an encrypted 3D EM model of the SEAX connector assembly and the corresponding pin-mapping. Signal pairs are indexed based on their port names in the simulation. The connector terminal indices for the simulation are as identified in the pin mapping above.

Figure 5 demonstrates an Ansys HFSS 3D component model of Samtec's SEARAY connector stack-up with 8 rows and 10 columns. The connector stack-up was simulated in isolation to determine the pin mapping required to achieve the desired inter-channel isolation.

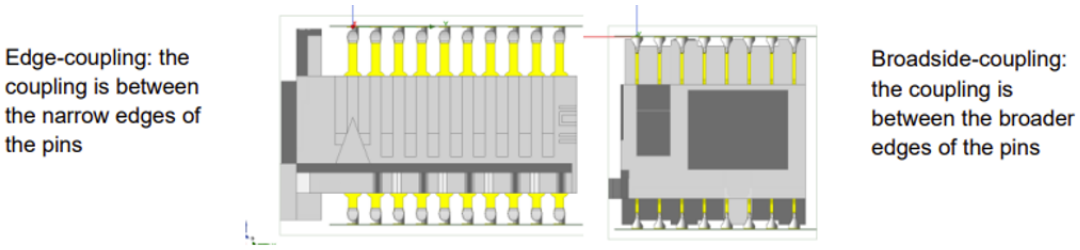


Figure 6: Edge-coupling vs. Broadside-coupling of the SEARAY connector pins.

The differential signal pairs were arranged along the column to achieve edge coupling (see Figure 6) versus to broadside coupling as initial simulations indicated that edge coupling configuration provided better return loss performance. The connector pin mapping was assigned to investigate the crosstalk performance achieved with two versus four ground pins between two differential signal pairs. The higher the number of ground pins between any two signal pin pairs, the better the crosstalk performance. However, this is at the expense of a larger connector size and consequently, more PCB real estate. Worst case return loss of -17 dB and maximum insertion loss of -0.27 dB was observed at 6 GHz. The return loss of the SEAF is approximately 1.8 dB worse than that of its SEAM counterpart, potentially due to the longer pin lengths of the SEAF connector. It is favorable to reduce the connector stack height as a larger stack height implies more insertion loss and higher crosstalk.

The connector crosstalk performance for the chosen pin mapping is displayed in Figure 7. Increasing the ground pin pairs from 2 to 4 improved the inter-channel isolation by approximately 11.5 dB. It must, however, be noted that as the number of aggressor channels (other signal pairs) around a victim channel is increased, the crosstalk observed will degrade.

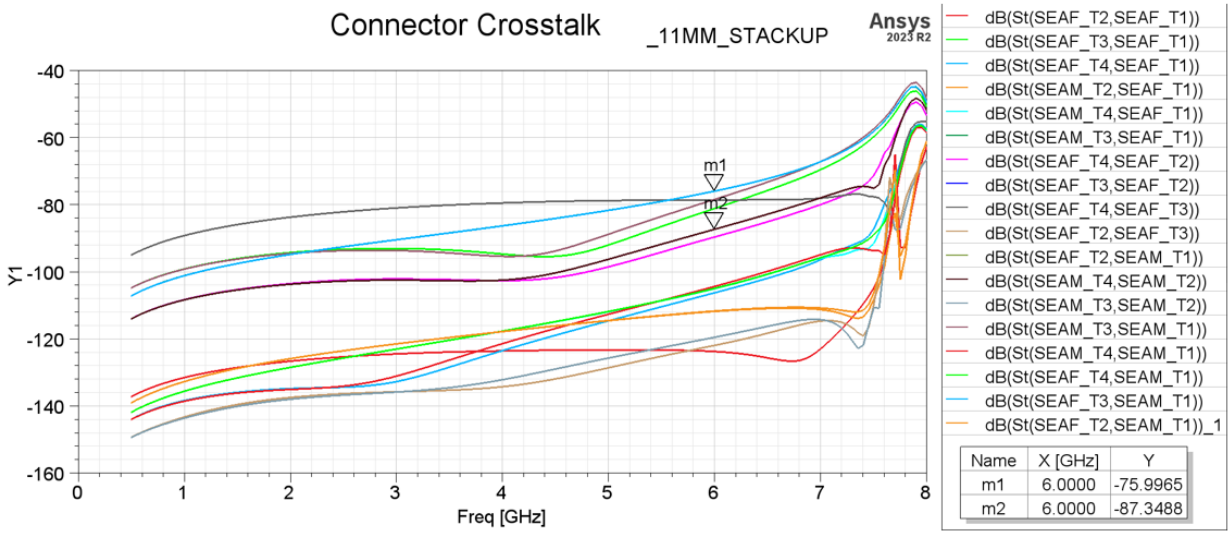
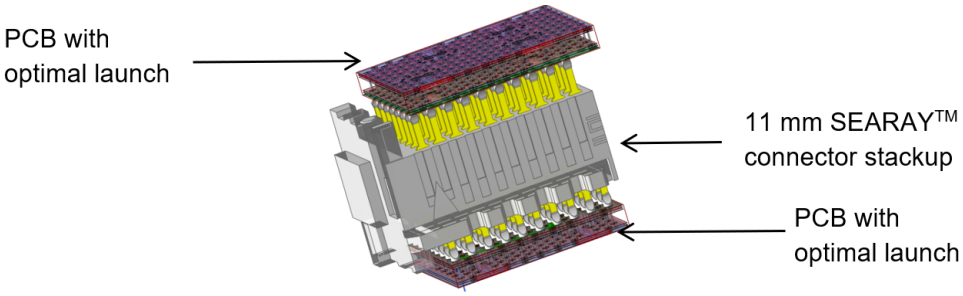


Figure 7 Simulated crosstalk performance of the SEAX connector assembly.

The simulation in Figure 8 shows that the board-to-board crosstalk performance is similar to the connector crosstalk performance, implying that the pin mapping through the connector is dominating the crosstalk performance achieved. It must be noted that these connectors are typically intended to be used in digital applications where crosstalk is not a key specification parameter.



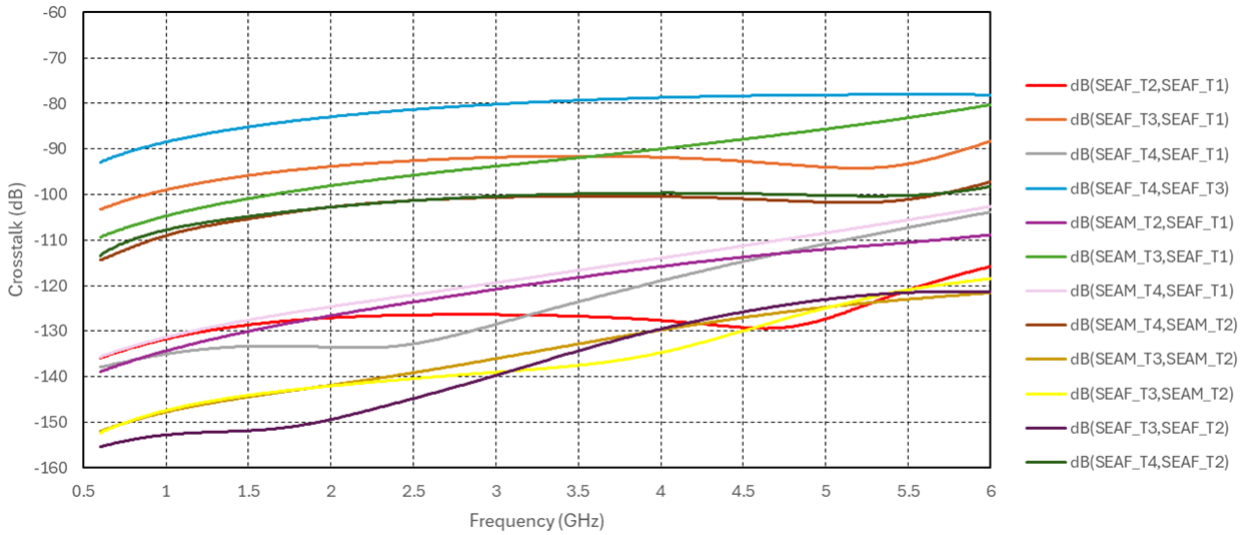


Figure 8: 3D EM model of the SEARAY™ connector assembly between two PCBs and the corresponding crosstalk simulation. The connector terminals are defined in the pin mapping in Figure 5.

More Details

The data in this case study was taken from Design aspects of a wideband RF Front-end for an Adaptable Radio Platform by Dr. Rucha Smith, Slipstream Engineering Design Ltd.

Follow these links for more information on products mentioned in this case study:

- SEARAY™ High Density Open Pin Field Arrays
- Magnum RF® Ganged RF Original Solutions, Multi-Port High Frequency
- Analog Over Array™ Technology
- ASTRO (RFSoC SOM) - Slipstream Design
- ASTRO Ecosystem - Slipstream Design