Mechanical Design of High Data Rate Cable Assembly for VITA 57.4

Application Note

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Mechanical Design of High Data Rate Cable Assembly for VITA 57.4

For VITA 57.4 Applications

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1 Abstract

FPGA development can encompass many different applications and needs. In some cases, the addition of mezzanines cards may present a challenge to mate with its host due to space constraints or even ease of access. Samtec has developed the FMC+ HDR Cable Extension which gives the FPGA developer an additional 397.8 mm of length to test the carrier cards away from the host without signal / performance degradation.

The cable is ideal for benchtop testing, system debugging, probing, FPGA development, or for regularly accessing a system where cards would need to be separated from the host board. This paper will explore:

- Mechanical & Electrical design of the FMC+ HDR Cable Extension.
- FPGA development using the FMC+ HDR Cable Extension.
- Qualification testing results for the FMC+ HDR Cable Extension.
- Specific applications for the FMC+ HDR Cable Extension.

2 Mechanical Design of the HDR Cable Assembly for FMC+ Applications

Some FPGA mezzanine cards may present a challenge to unmate from their host due to ease of access and size constraints. FPGA developers now have an option to extend the reach of the host board 397.8 mm without signal / performance degradation through the Samtec developed HDR Cable Assembly for FMC+.

The HDR-199453-01-FMC is designed for use with VITA 57.4 systems. The HDR cable assembly uses Samtec's High Speed Twinax and Coax cables as the medium to extend the reach of the system. The Samtec SEARAY™ connector assemblies are also mounted on opposite sides. See Image 1 for the layout.

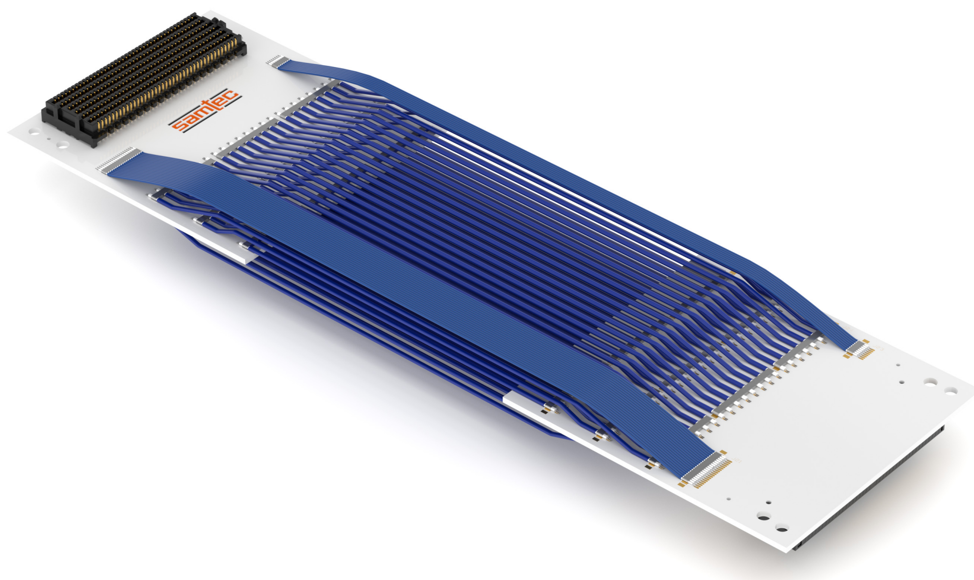

Image 1. HDR-199453-01-FMC HDR Cable Assembly

2.1 *Mechanical Design Factors in the FMC+ HDR Cable Assembly*

Since many of the applications that involve VITA 57.4 systems are on highly populated boards with sensitive components; it is important to have an easy way to access the FMC+ carrier. The FMC+ HDR Cable Assembly provides this access as shown in Image 2. The cable assembly fulfils the following features:

1. FPGA development is the focus of the cable. Additional length should be allowed without a degradation to the signal / performance in the system.
2. The FMC+ carrier can be located in an area when space constraints exist, and there is a need to move the connection point to easily assessable location to avoid damage.
3. Boards on the cable assembly should be designed to work in conjunction with the Micro Jack Screw Standoff (JSOM).
4. Disassembly should remain easily accessible to not interfere with other components.

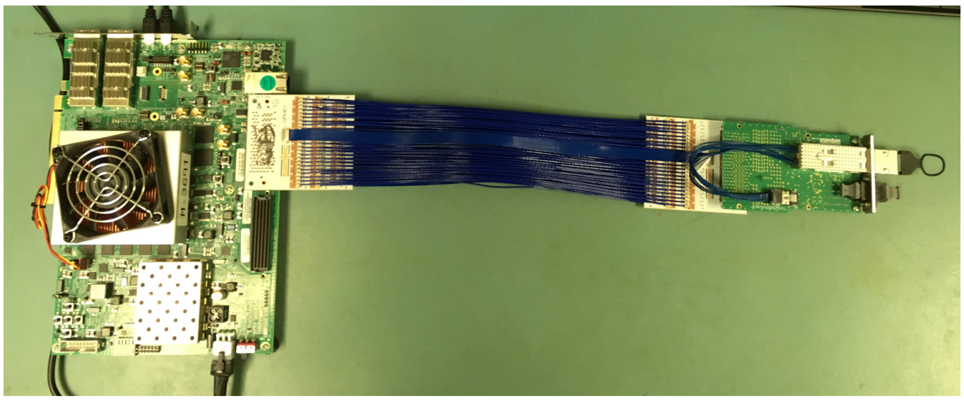

Image 2. VITA 57.4 application of the Xilinx UltraScale+ VCU118 FPGA utilizing the FMC+ HDR Cable Assembly

2.2 *Design and Pinout of the HDR Cable Assembly for FMC+*

The FMC+ HDR Cable Assembly is designed at a length of 397.8mm with connector mounting on opposite sides of the cable. This was designed to emulate the mating directly to the host board without effecting the performance of the system. Side 1 the cable uses the Samtec socket ASP-184330-01 and Side 2 uses the Samtec terminal ASP-184329-01.

The pinout is mapped 1—1 for the system and is shown below in Table 1. This ensures that any system designed to meet VITA 57.4 will function with this cable assuring near invisibility to the system.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND
ALL GROUNDS COMMON AND TIED TO CABLE SHIELD														

Table 1 –FMC+ HDR Cable Assembly Signal Map

2.3 *Testing the FMC+ HDR Cable Assembly*

2.3a Test Setup

To determine electrical performance of the HDR-199453-01-FMC, the Xilinx VCU118 was used in two different configurations. Test Setup 1 utilizes the FMC+ copper loopback (REF-194914-01) vs Test Setup 2 utilizing the 28G FireFly FMC+ loopback (REF-200772-28G-16-01). The VCU118 was utilized as the FMC+ carrier along with the two different loopback cards, see Figure 1 and Figure 2. Details of the signal paths are shown below for both loopback setups.

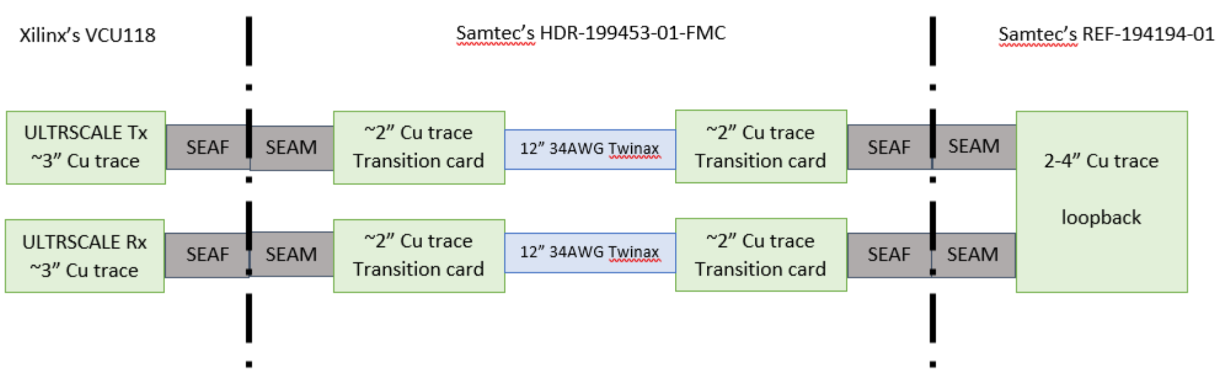

Figure 1: Test setup 1 utilizing the FMC+ Copper Loopback Card

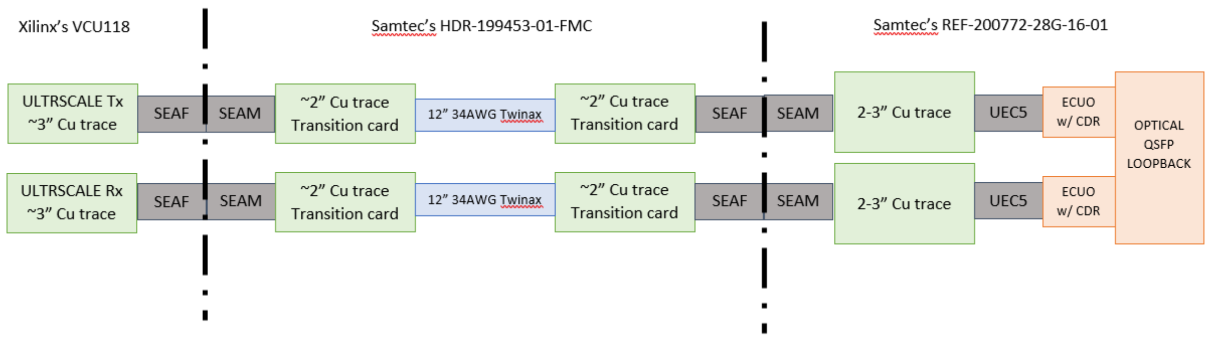

Figure 2: Test setup 2 utilizing the 28G FireFly FMC+ Loopback Card

Both setups utilize similar setups, with the exception of the loopback cards, and was to show that the FMC+ HDR Cable System will perform with varying end setups.

2.3b Testing Results

Test Setup 1 ran over all 24 channels and was found to be error free for over 15 hours of testing with a BER < 1e-15. There was no pre-emphasis and DFE was enabled for the test. The eye diagram is shown in Figure 3 and the resulting data in Table 2.

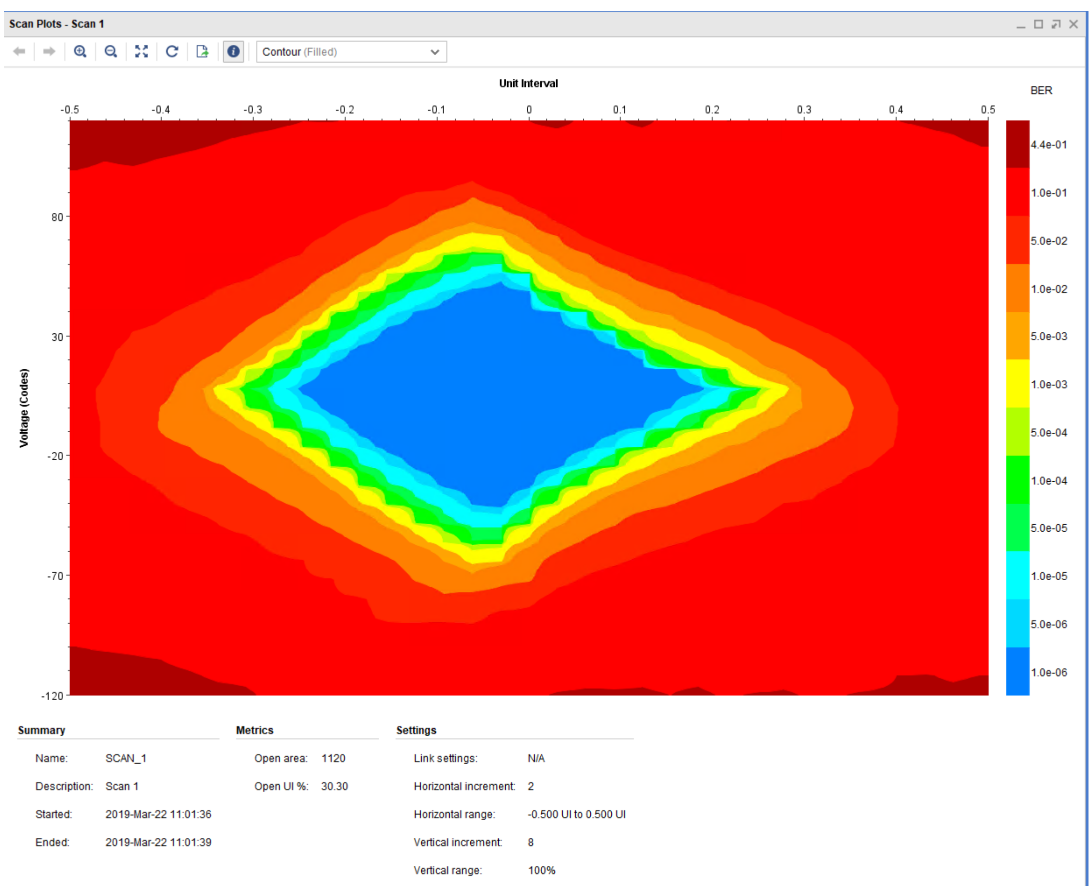

Figure 3: Eye Diagram for Test Setup 1

Name	TX	RX	Status	Bits	Errors	BER
Ungrouped Links (0)						
Found Links (24)						
Found 0	MGT_X0Y4/TX	MGT_X0Y4/RX	28.010 Gbps	1.493E15	0E0	6.7E-16
Found 1	MGT_X0Y5/TX	MGT_X0Y5/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 2	MGT_X0Y6/TX	MGT_X0Y6/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 3	MGT_X0Y7/TX	MGT_X0Y7/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 4	MGT_X0Y8/TX	MGT_X0Y8/RX	27.994 Gbps	1.493E15	0E0	6.7E-16
Found 5	MGT_X0Y9/TX	MGT_X0Y9/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 6	MGT_X0Y10/TX	MGT_X0Y10/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 7	MGT_X0Y11/TX	MGT_X0Y11/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 8	MGT_X0Y12/TX	MGT_X0Y12/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 9	MGT_X0Y13/TX	MGT_X0Y13/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 10	MGT_X0Y14/TX	MGT_X0Y14/RX	27.968 Gbps	1.493E15	0E0	6.7E-16
Found 11	MGT_X0Y15/TX	MGT_X0Y15/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 12	MGT_X0Y24/TX	MGT_X0Y24/RX	27.965 Gbps	1.493E15	0E0	6.7E-16
Found 13	MGT_X0Y25/TX	MGT_X0Y25/RX	27.973 Gbps	1.493E15	0E0	6.7E-16
Found 14	MGT_X0Y26/TX	MGT_X0Y26/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 15	MGT_X0Y27/TX	MGT_X0Y27/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 16	MGT_X0Y28/TX	MGT_X0Y28/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 17	MGT_X0Y29/TX	MGT_X0Y29/RX	27.943 Gbps	1.493E15	0E0	6.7E-16
Found 18	MGT_X0Y30/TX	MGT_X0Y30/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 19	MGT_X0Y31/TX	MGT_X0Y31/RX	28.041 Gbps	1.493E15	0E0	6.7E-16
Found 20	MGT_X0Y32/TX	MGT_X0Y32/RX	27.991 Gbps	1.493E15	0E0	6.7E-16
Found 21	MGT_X0Y33/TX	MGT_X0Y33/RX	27.987 Gbps	1.493E15	0E0	6.7E-16
Found 22	MGT_X0Y34/TX	MGT_X0Y34/RX	28.000 Gbps	1.493E15	0E0	6.7E-16
Found 23	MGT_X0Y35/TX	MGT_X0Y35/RX	28.000 Gbps	1.493E15	0E0	6.7E-16

Table 2: Data for Test Setup 1

Test Setup 2 ran over all 16 loopback channels and was found to be error free over the duration of 2.5 hours of testing with a BER < 4e-15. The eye diagram is shown in Figure 4 and the resulting data in Table 3.

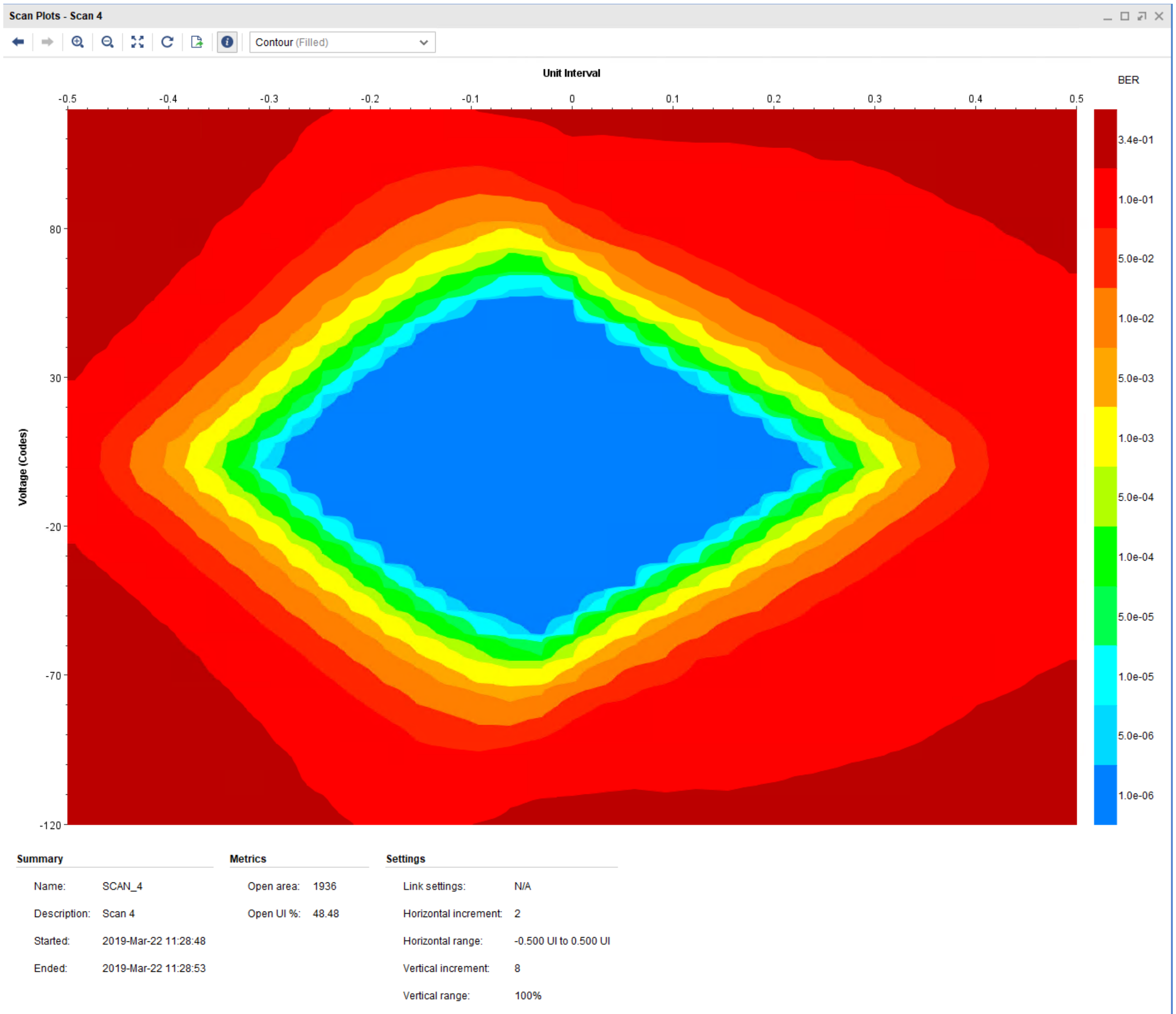

Figure 4: Eye Diagram for Test Setup 2

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled
Ungrouped Links (0)													
Link Group 0 (16)							Reset	PRBS 31-bit	PRBS 31-bit	Multiple	Multiple	Multiple	✓
Link 4	MGT_X0Y11/TX	MGT_X0Y8/RX	28.021 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 5	MGT_X0Y10/TX	MGT_X0Y9/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 6	MGT_X0Y9/TX	MGT_X0Y10/RX	28.012 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.22 dB (00001)	7.43 dB (10111)	766 mV (10100)	✓
Link 7	MGT_X0Y8/TX	MGT_X0Y11/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 8	MGT_X0Y12/TX	MGT_X0Y12/RX	27.966 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 9	MGT_X0Y15/TX	MGT_X0Y13/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 10	MGT_X0Y13/TX	MGT_X0Y14/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 11	MGT_X0Y14/TX	MGT_X0Y15/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 12	MGT_X0Y24/TX	MGT_X0Y24/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 13	MGT_X0Y25/TX	MGT_X0Y25/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 14	MGT_X0Y26/TX	MGT_X0Y26/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 15	MGT_X0Y27/TX	MGT_X0Y27/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	7.43 dB (10111)	720 mV (10010)	✓
Link 16	MGT_X0Y29/TX	MGT_X0Y28/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.41 dB (00110)	6.94 dB (10110)	720 mV (10010)	✓
Link 17	MGT_X0Y31/TX	MGT_X0Y29/RX	28.023 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓
Link 18	MGT_X0Y30/TX	MGT_X0Y30/RX	28.000 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	7.43 dB (10111)	720 mV (10010)	✓
Link 19	MGT_X0Y28/TX	MGT_X0Y31/RX	28.009 Gbps	2.542E14	0E0	3.934E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.92 dB (00100)	6.94 dB (10110)	720 mV (10010)	✓

Table 3: Data for Test Setup 2

2.4 *Application Recommendations*

The FMC+ HDR Cable Extension is designed to offer FPGA designers the ability to easily access the FMC+ carrier for VITA 57.4 applications, see Image 2. The assembly is ideal for benchtop testing, system debugging, probing, FPGA development, or for regularly accessing a system where cards would need to be separated from the host board. The specified cable for VITA 57.4 applications is as follows:

- 397.8 mm end to end length options w/ connectors mounted Opposite Side
  - High Data Rate Cable, (HSPC) female to (HSPC) male – HDR-199453-01-FMC

3 Conclusions

With Samtec's FMC+ HDR Cable Assembly, FPGA development in heavily populated areas becomes much easier to manage. The FMC+ HDR Cable Assembly expands the work area for FMC+ applications and provides the user with more room and easier access to mate and unmate a mezzanine card.

Those who need additional room for benchtop testing, system debugging, probing, FPGA development, or regularly accessing a system where the card needs to be separated from the host board can utilize the FMC+ HDR Cable Assembly without degradation of signal / performance within the system. Samtec offers the FMC+ HDR Cable Assembly as a standard offering to work with all VITA 57.4 applications.

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