VITA 57.4 FMC+ Loopback Cards

Application Note

APRIL 2024

VITA 57.4 FMC+ Loopback Cards

For VITA 57.4 Applications

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Change History

Revision #	Reason	Author	Date
01	Initial Release	Matt Burns	09/01/2019
02	Fixed grammar errors, Updated Figure 7.	Matt Burns	09/27/2019
03	Updated Section 7.2	Matt Burns	04/03/2024

1 Abstract

FPGA carrier card developers require easy-to-use options to confirm the operation of the VITA 57.4 FMC+ expansion connector typically found on these platforms. With Samtec's VITA 57.4 FMC+ Loopback Cards, testing the HSPC and HSPCe interfaces on FPGA carrier cards becomes much easier to manage.

Samtec's family of VITA 57.4 FMC+ Loopback Cards include the HSPC Loopback Card (REF-197618-01) and the HSPC/HSPCe Loopback Card (REF-197693-01). The VITA 57.4 FMC+ Loopback Cards are ideal for benchtop testing, system debugging, probing, or FPGA development.

Both cards provide FPGA designers an easy to use loopback option for testing low-speed interfaces and high-speed multi-gigabit transceivers on any FPGA development board or FPGA carrier card. It can run system data or BER testing on all channels in parallel. This makes evaluation and development with an FPGA much easier and an ideal substitute for 28 Gbps test equipment.

This paper will explore the following details of the VITA 57.4 FMC+ Loopback Cards:

- Mechanical Dimensions and Assembly Features
- Connector Pin Assignments and Block Diagrams
- Software Reference Designs
- Qualification testing set-up and test results

2 Mechanical Dimensions

Both the HSPC Loopback Card and the HSPC/HSCPe Loopback Card conform to the mechanical dimensions of FMC+ Manual as defined within ANSI/VITA 57.4-2019 Section 3. Specific mechanical dimensions for both cards are highlighted below.

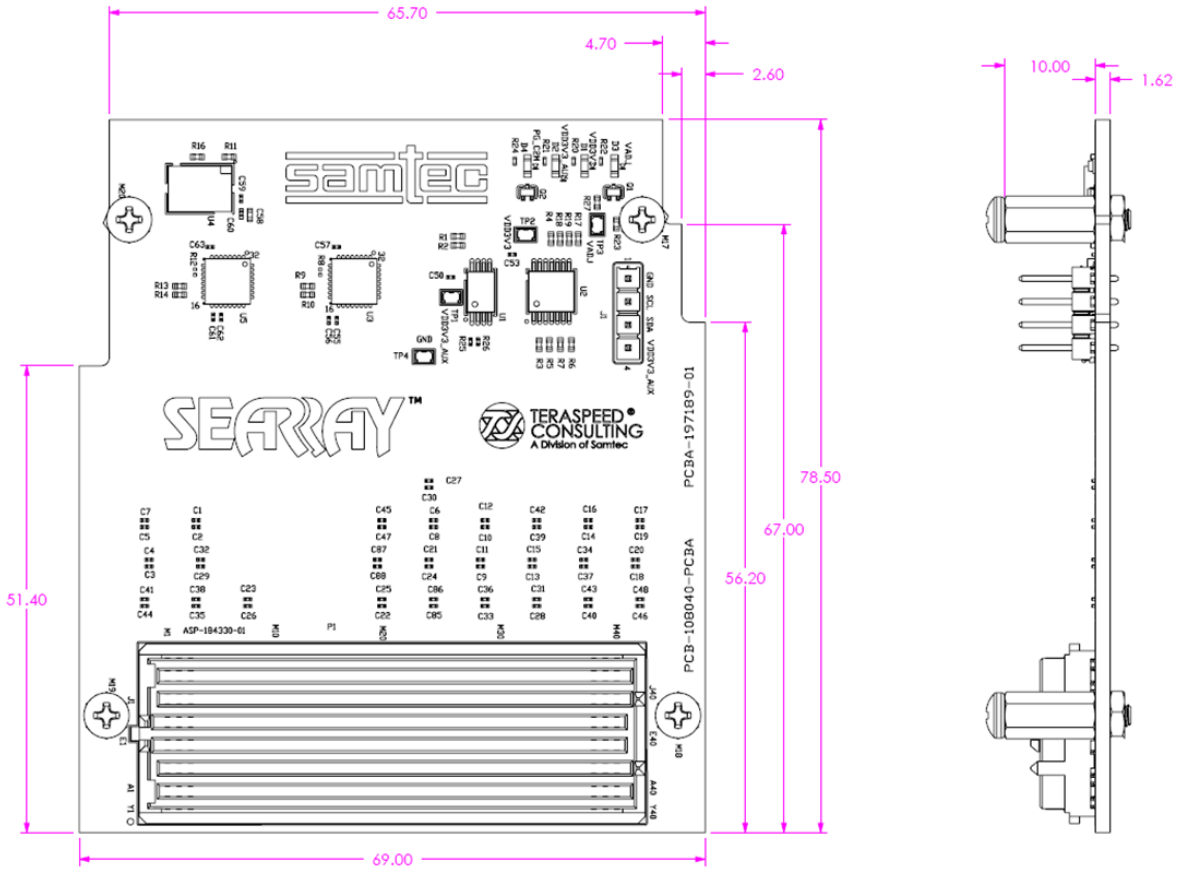

Figure 1 - Mechanical Dimensions for HSPC Loopback Card

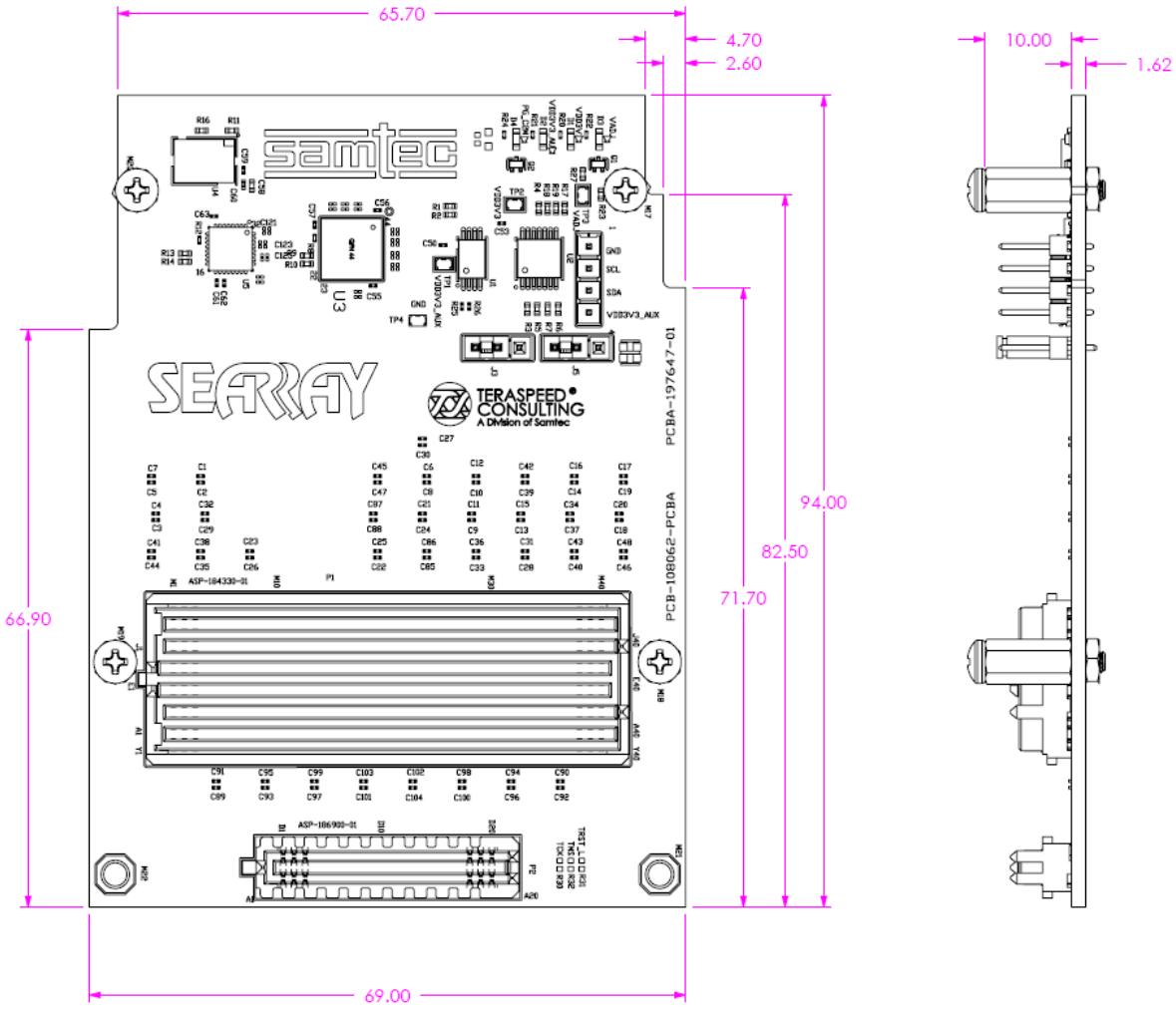

Figure 2 - Mechanical Dimensions for HSPC/HSPCe Loopback Card

3 Mechanical Design Features

Since many of the applications that involve VITA 57.4 systems are on highly populated with sensitive components, it is important to have an easy way to access the FMC+ carrier. The FMC+ Loopback Cards provide several mechanical features that ease mating and unmating.

The FMC+ Loopback Cards feature:

1. The FMC+ Loopback cards have been designed to work in conjunction with the Micro Jack Screw Standoff (JSOM).
2. Use JSOMs to carefully mate and unmate the FMC+ Loopback Cards to the FPGA carrier to avoid damages.
3. An Allen-key unscrews and expands the jack screw, dividing the PCBs in a steady, even motion until the mezzanine is safely separated from its host.

4 Connector Pin Assignments

Both the HSPC Loopback Card and the HSPC/HSCPe Loopback Card conform to the Connector Pin Assignments of HSPC and HSPCe connectors as defined within ANSI/VITA 57.4-2019 Section 5. Specific pin assignments for both cards are highlighted below.

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

Figure 3 - HSPC Connector Pin Assignments

4 x 20	A	B	C	D
1	GND	GBTCLK6_M2C_P	GND	HSPCE_PRSNT_M2C_L
2	GND	GBTCLK6_M2C_N	GND	RES6
3	DP24_C2M_P	GND	DP24_M2C_P	GND
4	DP24_C2M_N	GND	DP24_M2C_N	GND
5	GND	DP25_C2M_P	GND	DP25_M2C_P
6	GND	DP25_C2M_N	GND	DP25_M2C_N
7	DP26_C2M_P	GND	DP26_M2C_P	GND
8	DP26_C2M_N	GND	DP26_M2C_N	GND
9	GND	DP27_C2M_P	GND	DP27_M2C_P
10	GND	DP27_C2M_N	GND	DP27_M2C_N
11	DP28_C2M_P	GND	DP28_M2C_P	GND
12	DP28_C2M_N	GND	DP28_M2C_N	GND
13	GND	DP29_C2M_P	GND	DP29_M2C_P
14	GND	DP29_C2M_N	GND	DP29_M2C_N
15	DP30_C2M_P	GND	DP30_M2C_P	GND
16	DP30_C2M_N	GND	DP30_M2C_N	GND
17	GND	DP31_C2M_P	GND	DP31_M2C_P
18	GND	DP31_C2M_N	GND	DP31_M2C_N
19	RES4	GND	GBTCLK7_M2C_P	GND
20	RES5	GND	GBTCLK7_M2C_N	GND

Figure 4 - HSPCe Connector Pin Assignments

5 Block Diagrams

Both the HSPC Loopback Card and the HSPC/HSCPe Loopback Card provide basic loopback functionality for testing general FPGA carrier cards that contain the HSPC and/or HSPCe interfaces. Each loopback card routes core signals to enable loopback functionality as defined within ANSI/VITA 57.4-2019 Section 5

Signals routed include:

- Gigabit data signals (MGTs)
- Gigabit reference clocks
- Control lines including JTAG (including IPMI support), I2C, addressing, and reserved signals
- All required power rails, sequencing, and control lines

Specific high-level signal routing for both cards are highlighted below.

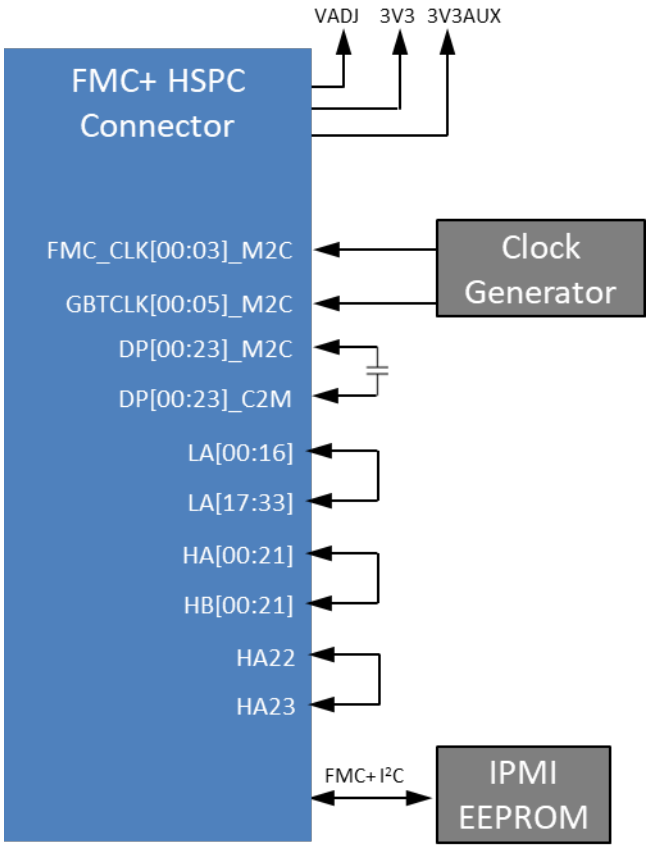

Figure 5 - HSPC Loopback Card Block Diagram

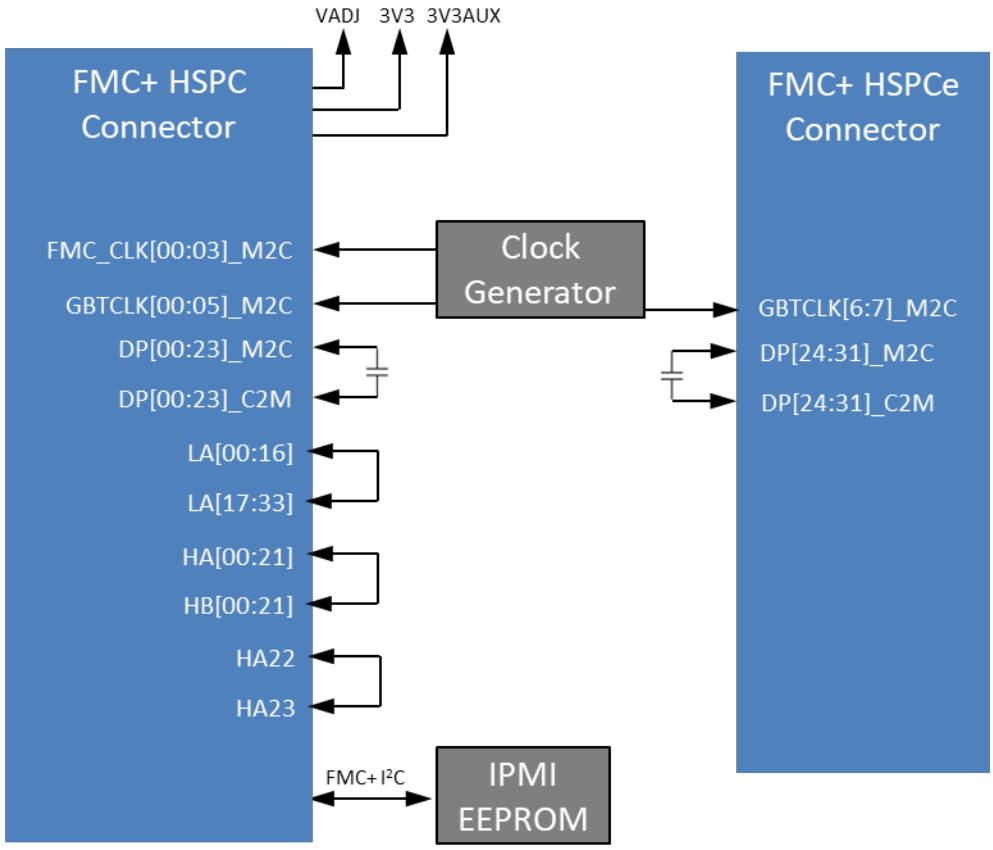

Figure 6 - HSPCe Loopback Card Block Diagram

Additional signal routing and circuitry details are contained in the schematics for both the HSPC Loopback Card and the HSPC/HSPCe Loopback Card. Schematics are available from Samtec under NDA. Please e-mail KitsAndBoards@samtec.com for more details.

6 Software Reference Design

Both the HSPC Loopback Card and the HSPC/HSCPe Loopback Card are pre-programmed with essential firmware and register setting to enable basic functionality. Firmware, register settings and accompanying software documentation are available from Samtec under NDA.

Please e-mail KitsAndBoards@samtec.com for more details.

7 Testing the FMC+ Loopback Cards Transceivers

The HSPC Loopback Card and HSPC/HSPCe Loopback Card have been designed to test low-speed signals and high-speed multi-gigabit transceivers on any FPGA development board or FPGA carrier card with the FMC+ interface.

7.1 *Test Setup*

General functional testing of power, control and low-speed signal are assumed with a successful power-up of the card. Key testing results are focused on verifying full-speed operation of the MGTs routed via the HSPC connectors.

To determine electrical performance of the HSPC Loopback Card, a Xilinx VCU118 was utilized as the FMC+ carrier along with the two different loopback cards. Test Setup 1 utilizes the HSPC Loopback Card. Test Setup 2 utilizes the HSPC/HSPCe Loopback Card.

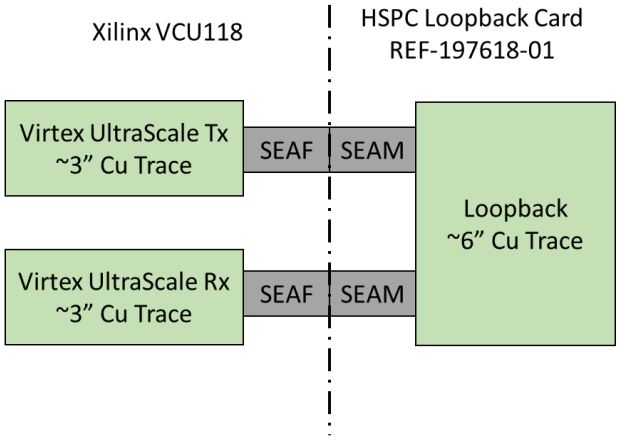

Figure 7 - Test Setup 1 Utilizing the HSPC Loopback Card

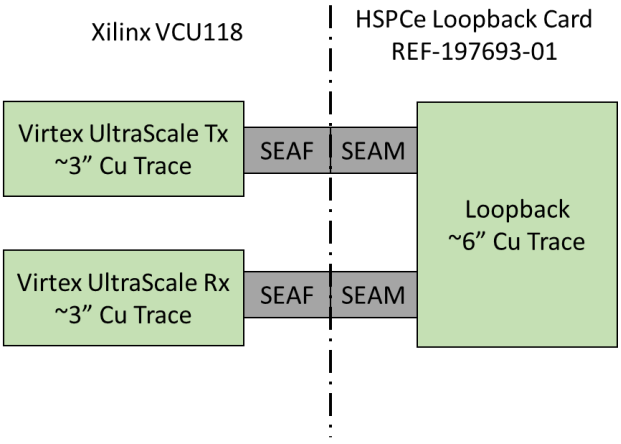

Figure 8 - Test Setup 2 Utilizing the HSPCe Loopback Card

7.2 Testing Results

Test Setup 1 ran over 24 channels and was found to be error free for over 15 hours of testing with a BER < 5.6e-15. Minimal signal conditioning was used and DFE was enabled for the test. The resulting data in Figure 9.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled
Found Links (24)							Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 0	MGT_X0Y4/TX	MGT_X0Y4/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 1	MGT_X0Y5/TX	MGT_X0Y5/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 2	MGT_X0Y6/TX	MGT_X0Y6/RX	28.001 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 3	MGT_X0Y7/TX	MGT_X0Y7/RX	28.011 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 4	MGT_X0Y8/TX	MGT_X0Y8/RX	27.988 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 5	MGT_X0Y9/TX	MGT_X0Y9/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 6	MGT_X0Y10/TX	MGT_X0Y10/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 7	MGT_X0Y11/TX	MGT_X0Y11/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 8	MGT_X0Y12/TX	MGT_X0Y12/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 9	MGT_X0Y13/TX	MGT_X0Y13/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 10	MGT_X0Y14/TX	MGT_X0Y14/RX	27.999 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 11	MGT_X0Y15/TX	MGT_X0Y15/RX	28.037 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 12	MGT_X0Y24/TX	MGT_X0Y24/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 13	MGT_X0Y25/TX	MGT_X0Y25/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 14	MGT_X0Y26/TX	MGT_X0Y26/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 15	MGT_X0Y27/TX	MGT_X0Y27/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 16	MGT_X0Y28/TX	MGT_X0Y28/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 17	MGT_X0Y29/TX	MGT_X0Y29/RX	28.034 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 18	MGT_X0Y30/TX	MGT_X0Y30/RX	28.012 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 19	MGT_X0Y31/TX	MGT_X0Y31/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 20	MGT_X0Y32/TX	MGT_X0Y32/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 21	MGT_X0Y33/TX	MGT_X0Y33/RX	27.996 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 22	MGT_X0Y34/TX	MGT_X0Y34/RX	28.000 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑
Found 23	MGT_X0Y35/TX	MGT_X0Y35/RX	27.943 Gbps	1.796E14	0E0	5.568E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	6.94 dB (10110)	846 mV (11000)	☑

Figure 9 - Data for Test Setup 1

Test Setup 2 ran over 24 channels and was found to be error free for over 15 hours of testing with a BER < 1e-14. Minimal signal conditioning was used and DFE was enabled for the test. The resulting data in Figure 10.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled
Ungrouped Links (0)													
Found Links (24)							Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 0	MGT_X0Y4/TX	MGT_X0Y4/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 1	MGT_X0Y5/TX	MGT_X0Y5/RX	27.813 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 2	MGT_X0Y6/TX	MGT_X0Y6/RX	27.855 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 3	MGT_X0Y7/TX	MGT_X0Y7/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 4	MGT_X0Y8/TX	MGT_X0Y8/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 5	MGT_X0Y9/TX	MGT_X0Y9/RX	27.762 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 6	MGT_X0Y10/TX	MGT_X0Y10/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 7	MGT_X0Y11/TX	MGT_X0Y11/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 8	MGT_X0Y12/TX	MGT_X0Y12/RX	27.853 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 9	MGT_X0Y13/TX	MGT_X0Y13/RX	27.813 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 10	MGT_X0Y14/TX	MGT_X0Y14/RX	27.790 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 11	MGT_X0Y15/TX	MGT_X0Y15/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 12	MGT_X0Y24/TX	MGT_X0Y24/RX	27.774 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 13	MGT_X0Y25/TX	MGT_X0Y25/RX	27.778 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 14	MGT_X0Y26/TX	MGT_X0Y26/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 15	MGT_X0Y27/TX	MGT_X0Y27/RX	27.788 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 16	MGT_X0Y28/TX	MGT_X0Y28/RX	27.813 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 17	MGT_X0Y29/TX	MGT_X0Y29/RX	27.802 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 18	MGT_X0Y30/TX	MGT_X0Y30/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 19	MGT_X0Y31/TX	MGT_X0Y31/RX	27.758 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 20	MGT_X0Y32/TX	MGT_X0Y32/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 21	MGT_X0Y33/TX	MGT_X0Y33/RX	27.759 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 22	MGT_X0Y34/TX	MGT_X0Y34/RX	27.814 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑
Found 23	MGT_X0Y35/TX	MGT_X0Y35/RX	27.820 Gbps	6.833E13	0E0	1.464E-14	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	6.47 dB (10101)	846 mV (11000)	☑

Figure 10 - Data for Test Setup 2

8 Conclusions

FPGA carrier card developers require easy-to-use options to confirm the operation of the VITA 57.4 FMC+ expansion connector typically found on these platforms. With Samtec's VITA 57.4 FMC+ Loopback Cards, testing the HSPC and HSPCe interfaces on FPGA carrier cards becomes much easier to manage.

Samtec's family of VITA 57.4 FMC+ Loopback Cards include the HSPC Loopback Card (REF-197618-01) and the HSPC/HSPCe Loopback Card (REF-197693-01). The VITA 57.4 FMC+ Loopback Cards are ideal for benchtop testing, system debugging, probing, or FPGA development.

Both cards provide FPGA designers an easy to use loopback option for testing low-speed interfaces and high-speed multi-gigabit transceivers on any FPGA development board or FPGA carrier card. The FMC+ Loopback Cards have been tested on numerous, popular FPGA evaluation kits and carrier cards. Data rates on the MGTs have been confirmed to 28 Gbps and beyond.

Additional details on can be found at www.samtec.com/kits.