Wideband RF Launches: More than Footprints on a PCB

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As the demand for higher frequencies and wider bandwidths continues its march upward, RF connectors need to keep up with or even exceed device bandwidth demands. Mating the RF connector to a PCB or substrate requires careful consideration of several factors to get the full performance out of the connector. This article provides an understanding of what makes successful launches work and covers design guidelines and an understanding of what knobs to turn to make connector launches perform well up to 100 GHz. As there are so many types of RF connectors, this article focuses on the compression-mount PCB type.

A compression-mount connector is compressed onto a PCB using mounting hardware to make a connection and can connect to either microstrip or stripline traces on the board. With the number of high-speed connections in PCBs increasing continually, compression-mount connectors provide several advantages. They are relatively compact, so several can be placed on a PCB, and as they can be placed anywhere on a PCB, compression-mount connectors can be located near the device the signal needs to reach, and they can also be reused.

Defining an RF launch

The launch includes the connector, signal via, and the via to the trace transition inside the PCB. To accurately gauge the performance of this combination, the tip of the connector and break-out region, including a short section of trace (about 2 mm), must be modeled and optimized together to achieve very broad bandwidths. RF launch designs are complex structures with no closed-form solutions and consist of many elements that need tuning in an EM solver to deliver maximum performance. Each of the sub-components shown in **Figure 1** represents a degree of freedom in the design of the launch.

The transition between PCB and connector tip has complex interactions requiring tuning, including contributions from both sides, to achieve the best performance. The connector landing pad size is dictated by the mechanical constraints of the connector and must be large enough to provide a reliable connection by accounting for manufacturing variations of connector and PCB fabrication but small enough to allow for designs to achieve the desired level of performance.

Electrically speaking, the drill hole size is the

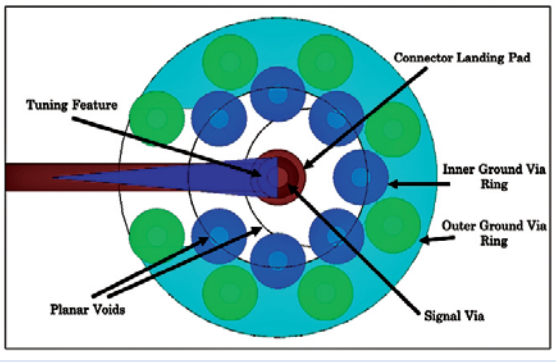

Figure 1: Sub-components of an RF launch

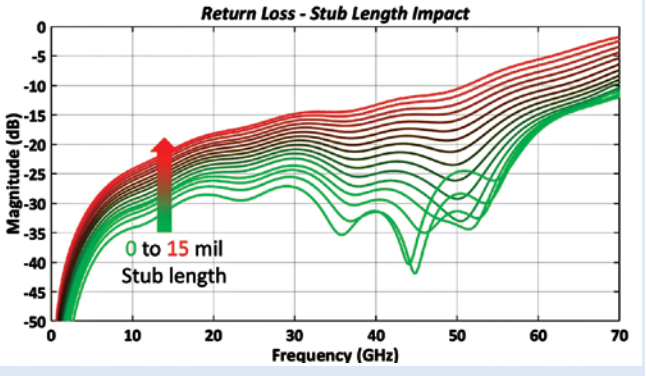

Figure 2: Via stub length impact on return loss

dimension that matters, not the finished hole size for a via. Having a list of common drill sizes used by the PCB vendor is very useful while trying to tune via launches. The drill size determines the minimum pad size of the via on the inner layers, and the smaller the minimum pad size, the better the via performance. Due to improved registration, laser-drilled micro vias can accommodate very small pad sizes, with an annular ring of as little as 2 mils with an L1:L2 transition (pad diameter = drill diameter + 2x annular ring). For deeper micro vias, the drill size and annular ring must be increased in size.

The tuning feature is used to equalize the impedance from the via pad/void region to the trace. The ground planes under the launch tie the ground rings together. Voids in the planes allow tuning the impedance seen by the signal as it travels down the via. When possible, it is best to create a "ground feature" on power planes and signal layers as it ensures adequate metal coverage along the via, improving the quasi-coaxial structure of the launch and its performance.

There are two rings of ground vias, and the performance of the launch is heavily dependent on them. The inner ring strongly impacts the impedance of the transition and cutoff frequency. The second ground ring helps seal the gaps between the vias of the inner ground ring, which limits crosstalk to adjacent transitions. Tuning the different subcomponents to obtain a wide bandwidth launch requires balancing several competing constraints.

The Impact of Via Stubs

When using a through via to transition to an internal layer, there is a stub created by the part of the via that extends below the transition layer. The higher the bandwidth goal, the more this stub impacts the performance. The impact of the stub is worst at a frequency where the stub length equals one-quarter of the wavelength:

$$f_0 \approx \frac{c}{4\,(Stub\ length)\sqrt{\varepsilon_R}}$$

Where,

F_o = Frequency where the stub = quarter wavelength (Hz)

c = Speed of light in vacuum (in./s)

Stub length = Length of stub (in.)

εR = Dielectric constant seen by the via

While f_o is the frequency at which the impact is most prominent, the via stub starts to degrade the performance of the via transition well before this frequency because it adds additional capacitance to the launch.

A common strategy to minimize the via stub's impact is to drill away most of the stub. In the back-drilling process, the PCB fabricator drills out the via stub from the side opposite the connector launch. However, no manufacturing process is perfect, and the back drill cannot get close to the signal launch layer for fear of damaging the contact between the via and trace.

Therefore, a residual stub is always left behind after the back-drilling process. There is also a tolerance associated with the leftover stub length. For example, a PCB fabricator might say the leftover stub length can be 8 mils +/-4 mil. A back-drilled via, in this case, can be left with a stub that is anywhere between 4 and 12 mils long, which is quite a large range. To be fair, this is a conservative example of stub length variation, and in many cases, smaller stubs may be achievable.

To illustrate the need to push for the smallest stub length, see the curves in **Figure 2**. There are 16 curves in the graph, each one corresponding to a stub length between 0 and 15 mils. The smaller the stub length, the higher the return loss across the band. To better visualize bandwidth impact, the frequency at which the return loss crosses the 15 dB level (VSWR = 1.4:1) is plotted in **Figure 3**. There are two main points to consider about the shape of the curve. First, the curve is not linear, with longer stub lengths causing a rapid drop-off in the bandwidth of the via transition, and for small stub lengths, the reduction in bandwidth is not significant.

So, pushing for a small residual stub and a tight tolerance provides significant benefits not only from the point of view of increasing the operating bandwidth of the launch but also from the point of view of all launches on the board behaving similarly to one another.

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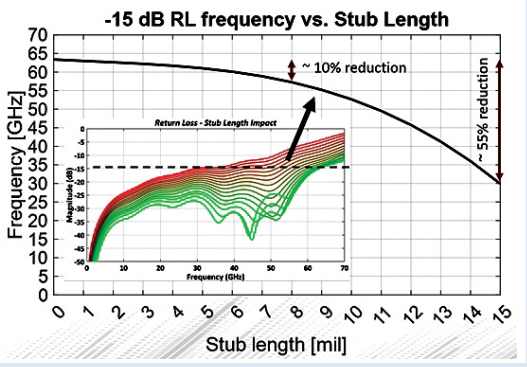

Figure 3: Bandwidth impact of via stubs of different lengths

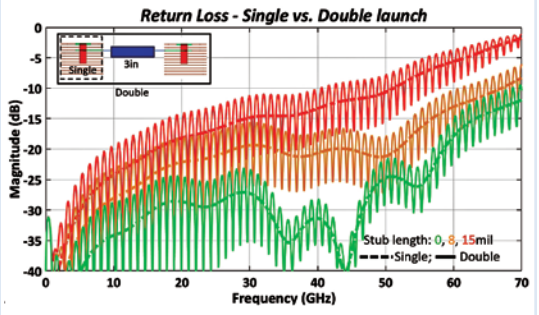

Figure 4: Multiple reflections between via stubs at either end of a trace magnify any performance limitations introduced by the via stub.

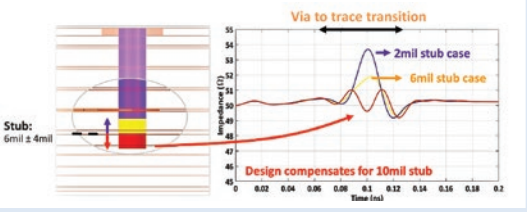

Figure 5: Impact of stub tolerance on compensation design

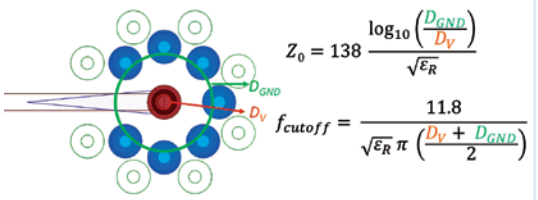

Figure 6: Equations to help with sizing the inner GND ring

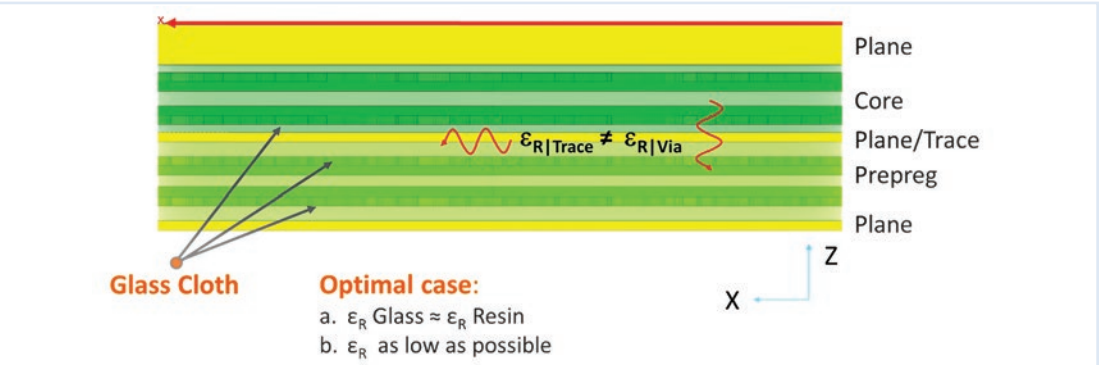

Figure 7: Dielectric constant in PCBs is direction dependent

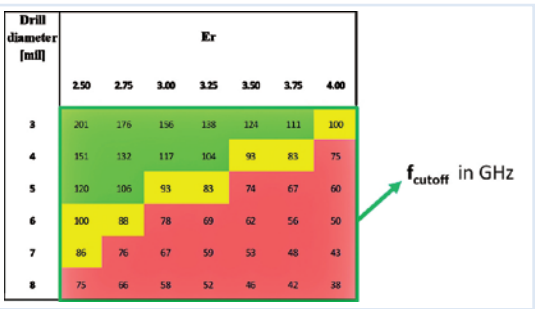

Figure 8: Higher order modes cutoff frequency as a function of drill diameter and ER

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Thus far, only the impact of a single stub has been considered, but every internal trace has at least two stubs, one at the launch and the other at the device side. So, any performance degradation introduced by the stub will be magnified by the reflections set up between the stubs at either end of the trace, as depicted in **Figure 4**. For each of the three stub lengths depicted in the figure, the return loss impact of reflections bouncing between two via launches at either end of the 3-in.-long, low-loss trace is shown in solid lines. The dashed line shows the comparative performance of a single launch, and in every case, it is significantly better than the double via case.

The best mitigation strategy is to go with laser vias with no stub at all. However, if back-drilled vias must be used, it is possible to compensate for the capacitance introduced by the stub to a limited extent in the design of the launch. In designing the compensation structure, it might be tempting to compensate for the worst-case stub length, but this can still result in poor performance if the stub tolerance is large. **Figure 5** clarifies this, where a tolerance of 4 mils on the 6 mil stub is assumed. The launch compensation is designed to provide the best impedance match for the worst-case stub length of 10 mils.

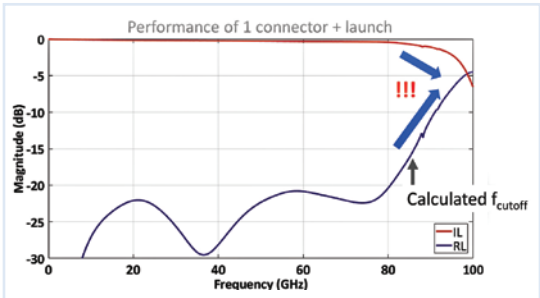

Figure 9: Rapid degradation in performance near and past the cutoff frequency of a launch

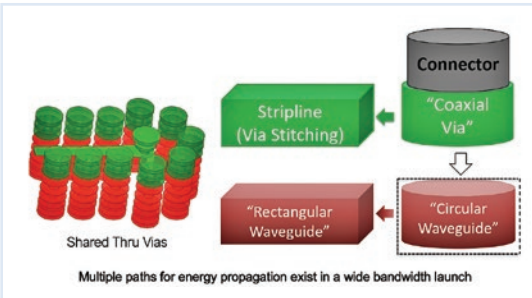

Figure 10: Physical structure of signal and GND vias of a launch (left) and conceptual drawing of the different physical parts of the launch structure (right)

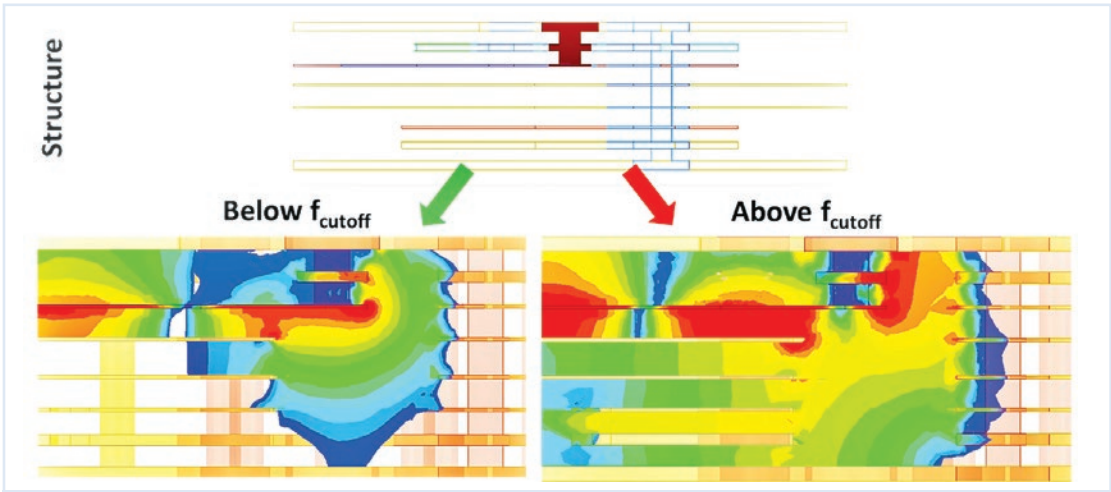

Figure 11: Electric field patterns in the launch area below and above the cutoff frequency

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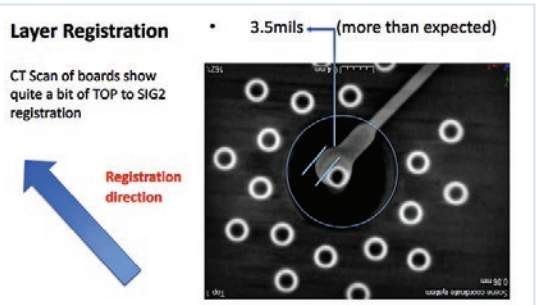

Figure 13: CT image showing misregistration of the inner layer with respect to the top layer

For a 10 mil stub, the impedance of the launch is within 1 ohm of nominal. The problem arises for vias with the stub length at the other end of the tolerance (2 mils). For this stub length, the launch looks quite inductive. Keep in mind that every stub on the board need not be the same length. The +/-4 mil tolerance can result in some vias looking inductive and others not, even when they are adjacent launches.

Correct Ground Ring Sizing

The inner ground ring has a strong influence on the performance of the launch. Two main factors determine the diameter of the inner GND via ring:

- The impedance of the launch area: **Figure 6** shows that the impedance of the launch area can be determined to the first order by treating the signal drill size as the center conductor diameter of the coax and the inner GND ring diameter as the shield diameter of coax. The nominal system impedance (e.g., 50 ohms) can be used as the target impedance for long vias.Short vias, however, are strongly impacted by the capacitive loading caused by the interaction between the launch and the end of the connector body. For this reason, a higher target Z_o, such as 70 ohms, is better. That way, the average effect of the connector + launch via is closer to 50 ohms.
- The cutoff frequency of the high-

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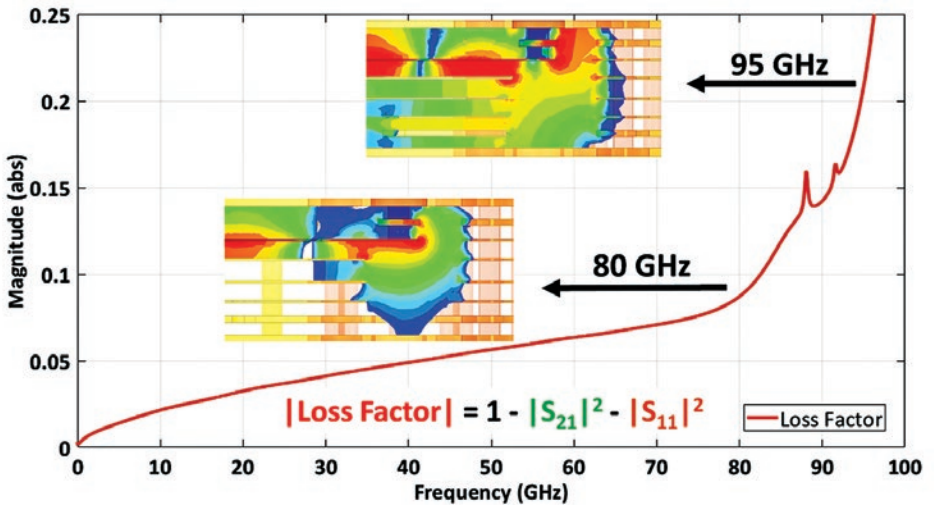

Figure 12: Plot of loss factor allows determination of whether launch performance is being impacted by higher order mode

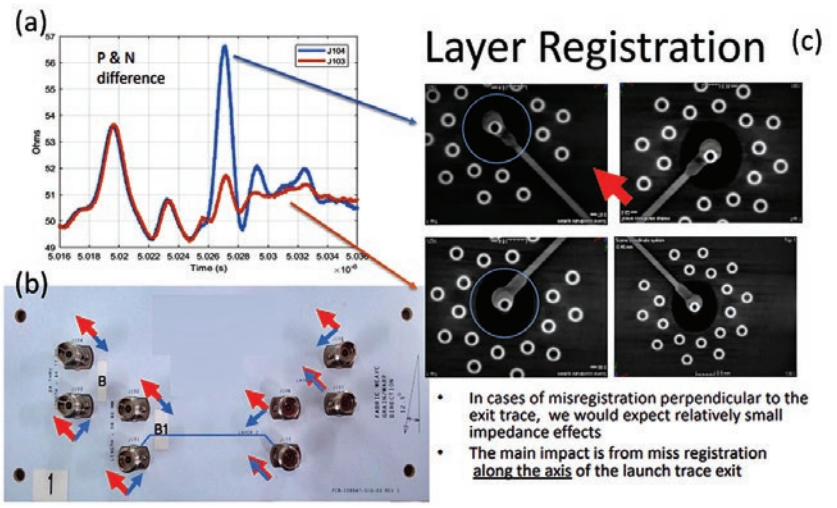

Figure 14: Impact of layer misregistration on connector launches

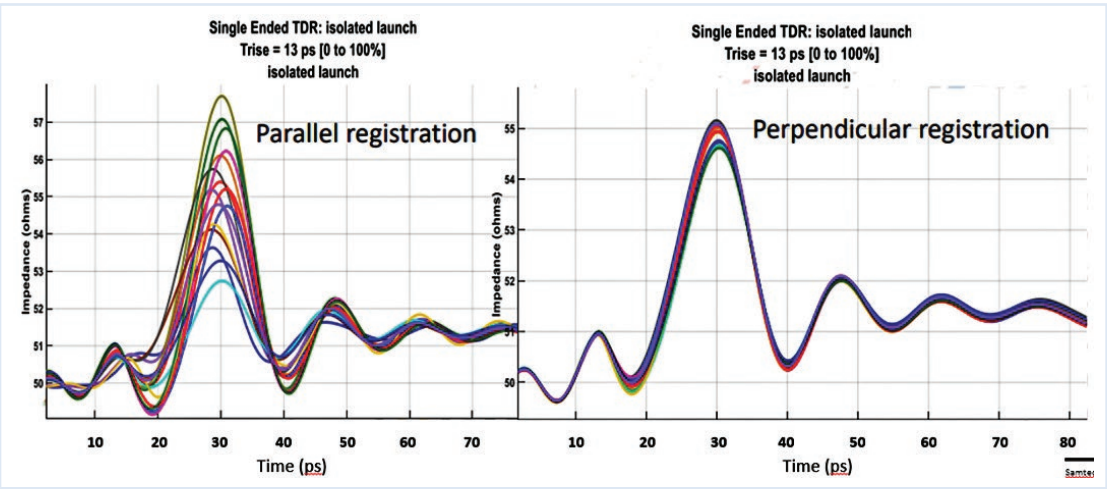

Figure 15: Impact of misregistration is dependent on the orientation of the trace launch

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er order modes supported by the launch: Normally, in a launch for a coaxial RF connector, only the fundamental mode to propagate is desired, which is the transverse electromagnetic mode (TEM). Above the cutoff frequency, the launch can support higher-order modes. When this happens, energy is spread among the different modes, and as the modes propagate differently, the signal gets distorted quickly. To prevent this, the launch needs to be designed so the cutoff frequency lies outside the bandwidth of interest.

Figure 7 shows that the cutoff frequency is inversely proportional to the GND ring's size and the dielectric constant seen when traveling down the via. The higher these numbers are, the lower the cutoff frequency and the lower the operating bandwidth of the launch. The formula for fcutoff in **Figure 7** provides the cutoff frequency in GHz when the diameters (Dv, DGND) are given in inches.

Both the impedance and the cutoff frequency are also inversely proportional to the dielectric constant (εR) seen by the signal as it travels down the via. It is important to note that this εR need not match the value seen by the trace. The reason is that PCBs are formed of laminates bonded together as composites and consist of glass fiber and resin. **Figure 8** shows a cross-sectional picture of a PCB.

There are both core layers and prepreg layers, each consisting of layers of glass cloth and resin. Since each of these layers has different dielectric properties, the effective dielectric constant seen by the signal depends on the direction it travels. In other words, PCBs are anisotropic as far as the dielectric constant is concerned. The higher the anisotropy, the greater the difference in dielectric constant seen by the via as compared to the trace.

To achieve wide-bandwidth launches, the dielectric constant of both the resin and the glass should be low and equal. This ensures the lowest possible dielectric constant around the via and, therefore, the highest cutoff frequency. The table in **Figure 9** shows that to reach cutoff frequencies higher than 90 GHz, signal drill diameters of less than 5 mils and dielectric constants of less than 3.1 are needed. The values in **Figure 9** can serve as a useful starting point in guiding the design of an RF launch.

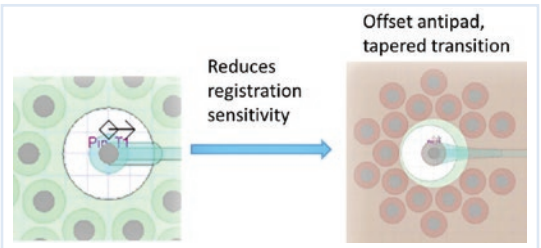

Figure 16: Use a tapered via-to-trace transition to minimize misregistration impact

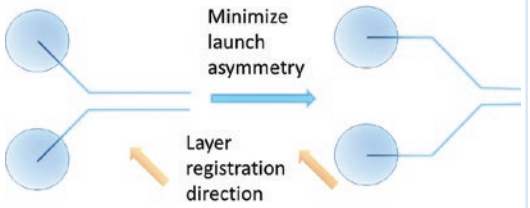

Figure 17: Route channels the same way to minimize differences between them

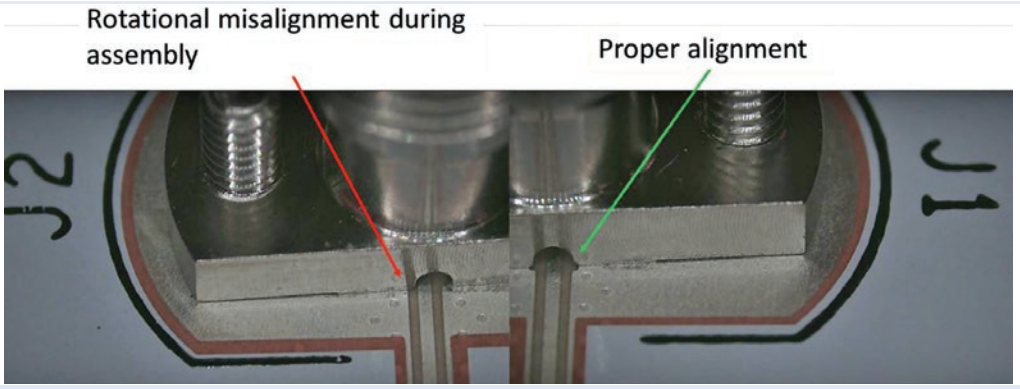

Figure 18: Connector misalignment introduced during assembly

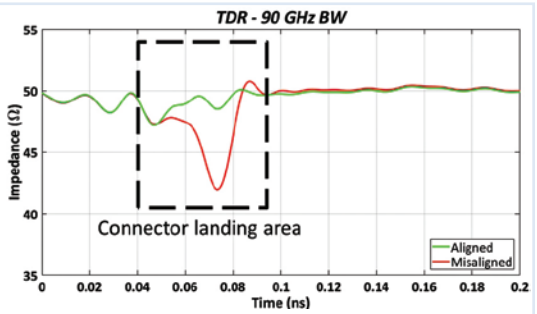

Figure 19: TDR of the connectors shown in Figure 18

Figure 9 makes it possible to understand mathematically why the performance of the launch quickly degrades around the cutoff frequency, as seen in **Figure 10**. To get a physical explanation of what is happening, refer to **Figure 11**. The structure of the launch via and the surrounding GND vias is shown on the left side of the figure. The portion of the vias colored in green represents the portion that the signal energy should travel in. As the GND vias are through vias, they continue below the reference layer of the trace to form waveguide structures below the signal reference layers.

To better visualize this, a conceptual schematic is shown on the right half of **Figure 11** that shows that the connector launches the energy into the coaxial portion of the launch with the signal energy then propagating down a stripline. However, below the trace reference layer, the GND

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vias form a circular waveguide under the signal via. The plane layers form several rectangular vias and stitch GND vias under the trace reference layer. The circular waveguide and rectangular waveguides under the trace are non-TEM structures, so they cannot propagate energy below the cutoff.

With this understanding, it's important to look at how energy flows in the launch at different frequencies. Shown in **Figure 12** are the electric field patterns in the launch below fcutoff (on the left half) and above fcutoff (on the right half). Below fcutoff, the energy stays contained within the stripline layers and the circular waveguide below the signal via cannot propagate energy, which is the desired outcome.

However, above fcutoff, the circular waveguide can now propagate energy, remove energy from the TEM mode traveling down the stripline, and send a portion of it through the rectangular cavities below the trace reference layer. This is undesirable because the energy can spread through the plane cavities to other parts of the board and cause crosstalk, radiation, and other effects. Staying below fcutoff therefore has the utmost importance in obtaining a high performance, wide bandwidth launch.

While the field plots shown in **Figure 12** aid in understanding the physical effects causing poor performance, computing the field plots is computationally quite intensive and takes significant time. There is a faster way to see if the launch performance is being adversely impacted by allowing the propagation of higher-order modes. **Figure 13** shows a metric called the loss factor. The loss factor is a measure of the amount of energy not reaching any of the ports of the structure. For a 2-port structure, for example, $|S_{11}|^2 + |S_{21}|^2$ is the total energy flowing through port 1. This energy gets either transmitted to port 2 ($|S_{21}|^2$) or reflected to port 1 ($|S_{11}|$)^2. In this case, the loss factor is 1- ($|S_{11}|^2 + |S_{21}|$)^2.

Figure 13 also shows that below fcutoff the energy loss increases gradually and corresponds to the energy lost in copper and dielectric losses. Above fcutoff however, the loss factor increases rapidly. This indicates that higher-order modes carry energy to other parts of the structure, and the launch is no longer performing as desired.

Misregistration Compensation

Misregistration refers to the fact that all the internal and outer layers of the PCB are not perfectly aligned. **Figure 14** shows an example of this. Here the inner layer is offset by 3.5 mils from where it would be expected. When designing launches for wide bandwidth, shifts of this order can result in the structure behaving quite differently than what it was designed to do.

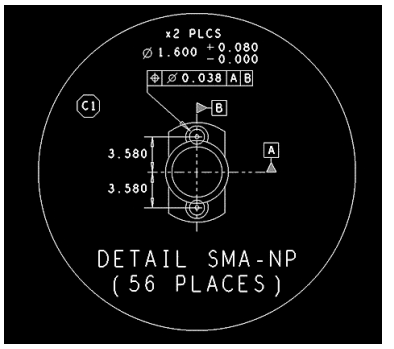

Figure 20: PCB fab drawing callout for connector mounting holes positioning tolerance

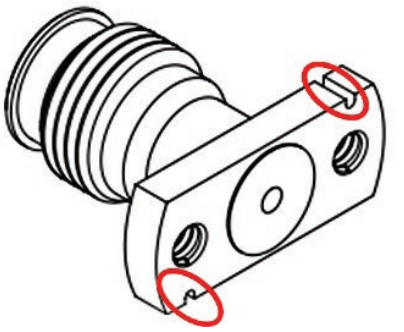

Figure 21: Notches milled in the foot of Samtec's compression mount connector to aid in the connector assembly.

There are several factors to consider here. The first is that the exact amount of misregistration is hard to quantify ahead of time. The second aspect is that misregistration can have a directional impact on measured results. **Figure 15a**, for example, shows a TDR of the two legs of a differential pair. The leg shown in blue clearly has an inductive spike that is caused by the clearances on the reference planes of the trace being shifted with respect to the via-to-trace tuning feature.

To better understand this, look at parts b and c of **Figure 15**. **Figure 15b** shows a photograph of the PCB while **Figure 15c** shows a CT image of the same board. At each of the connector locations in **Figure 15a**, there are two arrows shown, one in red and the other in blue. The red arrow indicates the direction in which the misregistration occurred. The blue arrow shows the direction in which the differential trace launches under the connector.

In this example, the trace launch direction in some cases is parallel to the direction of misregistration, while in other cases it is perpendicular to the direction of misregistration. The CT image in **Figure 15c** shows the direction of misregistration in red and four traces that launch from under the connector in comparison to the misregistration direction.

Comparing the TDR in **Figure 15** with both the photograph and the CT images it becomes clear that when the misregistration is parallel to the direction of the trace exit, the impact on the TDR is much more than when it is perpendicular to it. The reason for this is that the size of the antipad and the shape of the via-to-trace transition are tuned relative to each other. When the antipad on the reference plane moves, the impedance seen by the signal in the via-to-trace transition is impacted much stronger than when the misregistration is perpendicular to the direction of the trace launch. **Figure 15** quantifies this effect.

In **Figure 16a**, the TDR for several traces that launch parallel to the direction of misregistration is plotted. **Figure 16b**, on the other hand, shows the TDR of traces that launch perpendicular to the direction of misregistration. Clearly, the variation in the impedance profile of traces launching parallel to the direction of misregistration is significantly greater than the variation seen for trace launches perpendicular to the direction of misregistration. The difference in impedance between the legs of the differential pair is problematic, and the fact that it is inconsistent from one pair to the next or even one side of the differential pair to the other makes it next to impossible to remove this effect when measuring a device.

Now that the effect of how misregistration can impact electrical performance has been presented, it's helpful to look at mitigation strategies. This is by no means a complete list, as other parameters can also be tweaked to reduce manufacturing sensitivity. Talking to a PCB fabricator is the best way to understand all the options available.

Strategy 1: Instead of using a rounded rectangle shape to transition from the via to the trace (**Figure 17**, left), use a tapered transition shape (**Figure 17**, right). This way, even if there is misregistration of the antipad in the reference layer, the impedance impact will be minimized.

Strategy 2: When routing legs of a differential pair or multiple channels of a bus, we want all the lanes to look as identical to each other as possible and launch all the channels the same way.

Figure 18 shows an example of this for a differential pair. Instead of launching the traces at 45 deg. and bringing them together to form a differential pair (**Figure 18**, left), launch all the lanes parallel to each other (**Figure 18**, right). Once they have left the connector launch area, the traces are brought

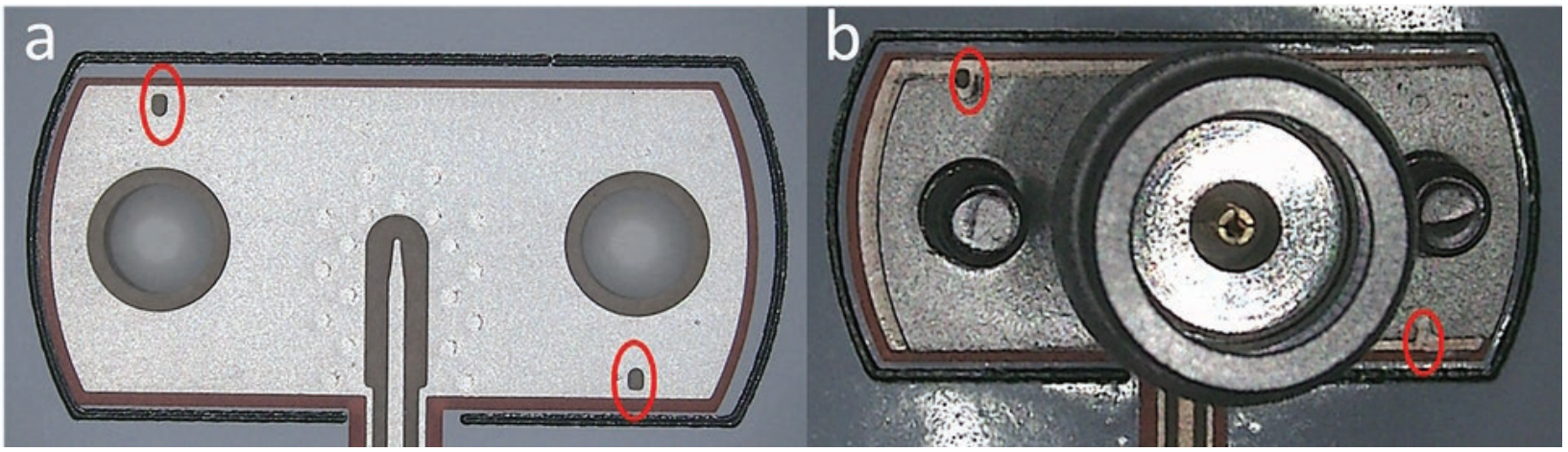

Figure 22: A PCB with copper-defined features for alignment (a) and connector with notches aligned to PCB alignment features (b)

together to the differential pair spacing.

Launch Performance Issues Introduced during Connector Assembly

So far, issues related to the design and fabrication of the launch have been addressed, but once the PCB has been fabricated the connectors need to be installed on the PCB. Two main assembly processes used for connectors are solder reflow and compression mount to the PCB, either directly or through some sort of interposer. For this article, only issues with compression mounting are addressed.

The connector is placed on the PCB to assemble a compression-mount connector without pressing down on the surface. Screws are then fed from the opposite side of the PCB and threaded within screw holes in the foot of the connector. There is usually a torque specification in the connector datasheet for how tight the screws need to be torqued down to ensure good and reliable contact. Care must be taken while tightening the screws to make sure the connector does not move around during the process. If the connector is moved around, it is possible to destroy the landing pad of the connector launch.

Even when care is taken during the assembly of the connector, as the screws are tightened to their final positions, the forces on the connector can cause them to rotate. **Figure 19** shows an example of misalignment that can occur due to this rotation.

Figure 19a shows that because of the connector rotation that occurred during assembly, the connector's ground body is now very close to the surface trace. **Figure 19b** shows what the properly mounted connector position should look like. Misalignment of the order shown in **Figure 19a** will cause capacitive loading at the launch.

Figure 20 shows a 90 GHz bandwidth TDR of the two connector positions shown in **Figure 19**. It shows an approximately 8 ohm capacitive dip introduced by the misalignment. When working with very wide bandwidths, even small misalignments can have a significant impact on the resulting performance.

One method that can be used to mitigate the risk of tearing off the pad while tightening the connector and misaligning during assembly is to reduce the size of the screw holes used to mount the connector. There is a manufacturing tolerance in the positioning of the screw holes.

By keeping this positional tolerance to a minimum and ensuring a tight tolerance for the size of the hole, the ease of assembly of the connectors is simplified. There will be minimal need to move the connector around to get to the proper position. Getting this accuracy, though, involves a couple of additional steps.

As shown in **Figure 20,** the positional tolerance of the connector mounting holes is specified to be tight. To get a tighter tolerance, the hole drilling is done using an optical inspection step that locates the landing pad of the connector. The drilling positions are then picked based on this position. That way, each connector's mounting holes are drilled with respect to the copper features of that location. It is important to constrain the position of the holes in both the X and Y axes. Constraining the position along the axis joining the mounting hole locations to the center pin location is insufficient.

A tight tolerance for the size of the screw hole is also specified. This reduces the play in the screw hole, limiting the amount of room available for the screw to move, thus minimizing the chances of connector rotation during the process of tightening the mounting screws. A feature of Samtec connectors that is very useful during the assembly process are notches that are milled into the foot of compression-mount connectors (**Figure 21**).

If copper features are defined to match the location of these notches, it becomes very easy during assembly to check the positional accuracy of the assembled connectors and make fine adjustments, if needed. This is especially helpful when assembling compression-mount connectors that connect only to striplines. In this case, there are no doghouse openings at the foot of the connector to verify the positional accuracy of the connector, making the notches invaluable.

An additional benefit is that since the notches align with copper features in the PCB, any offset between the mounting hole location and landing pad location is easily noticed. This removes any doubt on whether assembly effects are detrimentally impacting subsequent measurements. An example of a PCB with a footprint having copper-defined features is shown in **Figure 22a**. **Figure 22b** shows the final result of the assembled connector, whose notches are aligned with the copper features, thus ensuring that the connector center pin is centered on the PCB landing pad.

Conclusion

This article shows that very wide bandwidth RF launches can be implemented even with vias included in PCBs. That does not mean it is trivial because competing requirements, mechanical, manufacturing, or cost, must be considered and balanced simultaneously. The article also discusses some of the most important design considerations. Optimizing these factors requires working with a PCB company to understand the manufacturing limits.

Ultimately, getting to 90 to 100 GHz bandwidths will often require pushing the edge of today's fabrication limits, so understanding the limits at the start of the design process helps reach a high-performance launch, which means high-fidelity connections to a device.

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