



Thermal Design of QSFP-DD Cages and Heatsinks

Application Note

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Thermal Design of QSFP-DD Cages and Heatsinks

For High Power, High Density Applications

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Change History

Revision #	Reason	Author	Date
01	Initial Release	Thom Hall	03/5/2018

1 Abstract

At the time of its writing, the QSFP-DD MSA defined the form factor for the industries smallest 400GbE module providing the highest port density. Upwards to 14Tb/s bandwidth of capability, in a 1U 36 port configuration.^{1,2} With the increase in bandwidth there comes a cost. To realize a 36 port single rack unit at the 400GbE there is significant heat to be managed, 504 watts aggregate need to be dissipated from the bank of transceiver modules while maintaining the module temperature at 70°C. This does not include power supply, CPU, and ASIC power that need to be dissipated.

With the upcoming introduction of Ethernet Switch Asics capable of managing 32 ports at 400GbE, this paper will explore:

- Factors in the QSFP-DD design that affect the thermal performance.
- Reference thermal design of a 1U switch, 32 channels at 14W per channel.
- Solutions Samtec Inc. has developed to insure thermal integrity of the system.

2 Thermal Design of QSFP-DD Cages and Heatsinks for High Power, High Density Applications

At the time of its writing, the QSFP-DD MSA defined the form factor for the industries smallest 400GbE module providing the highest port density. Upwards to 14Tb/s bandwidth of capability, in a 1U 36 port configuration.^{1,2} With the increase in bandwidth there comes a cost. To realize a 36 port single rack unit at the 400GbE there is significant heat to be managed, 504 watts aggregate need to be dissipated from the bank of transceiver modules while maintaining the module temperature at 70°C. This does not include power supply, PSU, and ASIC power that need to be dissipated.

With the upcoming introduction of Ethernet Switching ASICs capable of managing 32 channels of 400GbE, a reference design focusing the thermal management of the QSFP-DD modules is needed. While Samtec is not in the business of designing and manufacturing QSFP-DD modules, we are in the business of designing and manufacturing QSFP-DD MSA compatible connectors, cages, heatsinks for flyover applications. Largely, the reference design will focus on the parameters that Samtec can influence, while leaving as much design flexibility and compatibility with differing module architectures as possible. This paper will talk to factors in the QSFP-DD design that affect the thermal performance, the thermal design of a modular reference 32 port 1U switch loosely based on the Facebook Wedge 100S³ utilizing Samtec's proprietary flyover technology.

2.1 Thermal Design Factors in the QSFP-DD

Much of the heat generated within an optic transceiver is from the optic engine. With the thermal sensitivity of the VCSELS within the module, as much heat as possible needs to be shunted to the heatsink. To that, the thermal path needs to be optimized. In general, the following features are needed:

1. The optic engine needs to be located on the heatsink side of the QSFP-DD paddle card.
2. The optic engine needs to be as centrally located as possible to the module to heatsink thermal window.
3. The shell needs to be as close as possible to the optic engine to take advantage of the high thermal conductivity of the shell material.
4. A high performance thermal interface material needs to be utilized to prevent a dead air space from insulating the optic engine. Note that foam type thermal interface materials have a compression dependent thermal conductivity, so design for maximum compression without risking damage to the optic device is desirable.
5. The thermal interface between the top shell and the heat sink need to be maximized. This includes minimizing the surface roughness of both the top shell of the module and the contact surface of the heat sink. It also includes maximizing the normal force at the interface to attain as much microscopic deformation as possible.
6. The heat sink fins need to be at the maximum height and length as the design envelope can allow.
7. The heat sink fin thickness and pitch need to be optimized to the available airflow and allowable pressure drop.
8. The air flow bypass around the fins needs to be minimized.
9. The heat generating subsystems within the switch need to be arranged in ascending order of sensitivity, namely ambient to the optic modules, to switching ASIC, to CPU, to power management.

2.2 QSFP-DD Thermal Path

2.2a Heat Sources

The sources for heat generation (Figure 1) within the module are (1) the module microcontroller and (2) the optic engine. The module microcontroller will have a power consumption rate in the single digit microwatt range.⁴ With such a low heat generation rate as compared to the Optic Engine the microcontroller is considered a static device in thermal analysis, although appropriate coupling to the heat sink is still desired to prevent overheating via parasitic heat transfer.

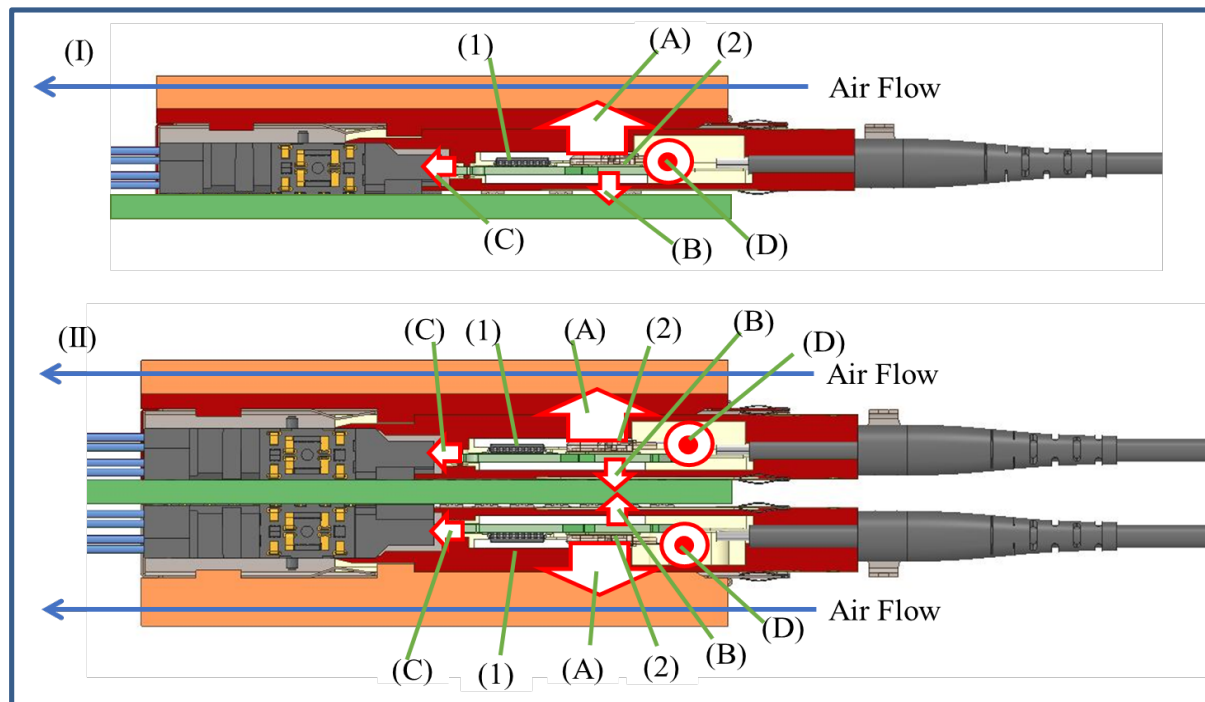


Figure 1 – Heat Sources and Transfer Paths: (I) Single Sided Configuration, (II) Dual Sided (Mezzanine) Configuration; Heat Sources (1) Controller Device, (2) Optic Engine; Heat Transfer Paths (A) to Heat Sink, (B) to Printed Circuit Board, (C) to QSFP-DD connector, (D) sides of cage.

The Optic Engine includes the VCSEL Drivers, VCSELS, transimpedance amplifiers (TIA), photodiodes, lenses, and local heat management components. Within this group the component with the lowest allowable temperature specification drives the specification. Typically this is the VCSEL. While the operating temperature of the VCSEL array is being increased by various manufacturers⁵, a target max operating temperature for the VCSEL is at 70°C. Use of more ruggedized VCSELS allows for increased head room in the thermal specification and will in turn increase the reliability of the system.

The QSFP-DD MSA sets the power levels as per Table 1, with the thermal range classifications as per Table 2. The goal for the system level design is to maintain a maximum of 70°C while dissipating 14W per module of heat.

Table 1

QSFP-DD Power Classifications ⁶

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

Table 2

QSFP-DD Temperature Range Classifications ⁷

Class	Case Temperature Range
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

2.2b Heat Paths

Referring to Figure 1, there are four paths to dissipating the optic engine heat.

Path (A) is the primary route, with the heat moving from the optic engine, to the thermal interface material, to the upper shell of the transceiver module, through the module/ heatsink interface through the heat sink, to the inlet air.

Path (B) is the secondary route with heat leaving the optic engine through the module PCB to the lower shell then radiating to the system PCB.

Path (C) is from the optic engine conducting through the module PCB to the electrical interconnect then to the system board.

Path (D) is from the optic engine along sideways across the module PCB to the sides of the shell then radiating to the side walls of the cage then the heat is either conducted to the system PCB or is released by convection from the side walls of the cage.

2.3 Correlation CFD and Wind Tunnel Analysis using Multilane QSFP-DD Heater Module

To determine the efficacy of the Multilane QSFP-DD Heater module (ML Heater) as a test vehicle and baselining the performance of an extruded heat sink, a correlation study was performed. A solid model of the Multilane QSFP-DD generated from accurate measurements of the module. The basic structure is a PCB with resistor in the forward and rear areas. (Figure 2) There is a connector on the rear of the PCB to connect to a controller for heating and controlling the resistors. The heat is coupled to the module shell via 4 pieces of thermal interface material QSFP-DD shell.

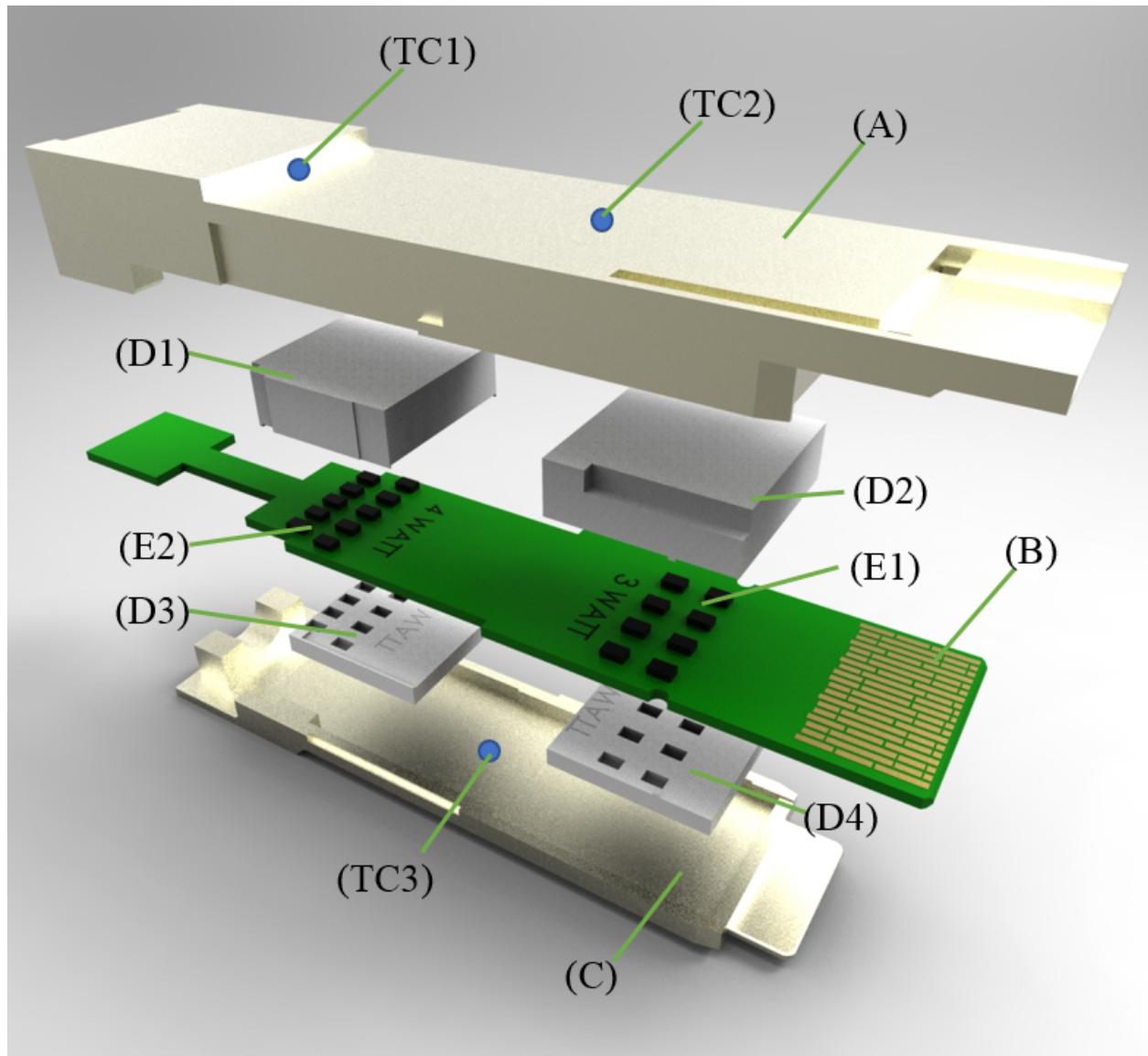


Figure 2. – Multilane QSFP-DD Heater Module: (A) Upper Shell, (B) PCB, (C) Lower Shell, (D1-D4) Thermal Interface Material, (E1-E2) resistor banks for heating on both sides of module PCB, (TC1-TC3) are the thermocouple locations for physical testing.

Figure 3 outlines the test setup for the correlation study. It is 4 Samtec FQSFP-DD's arranged in a belly to belly mezzanine configuration. The Multilane Heater Modules were excited to 7 Watts: 3 watts on the forward (E1) group of resistors and 4 watts on the rearward (E2) group of resistors.

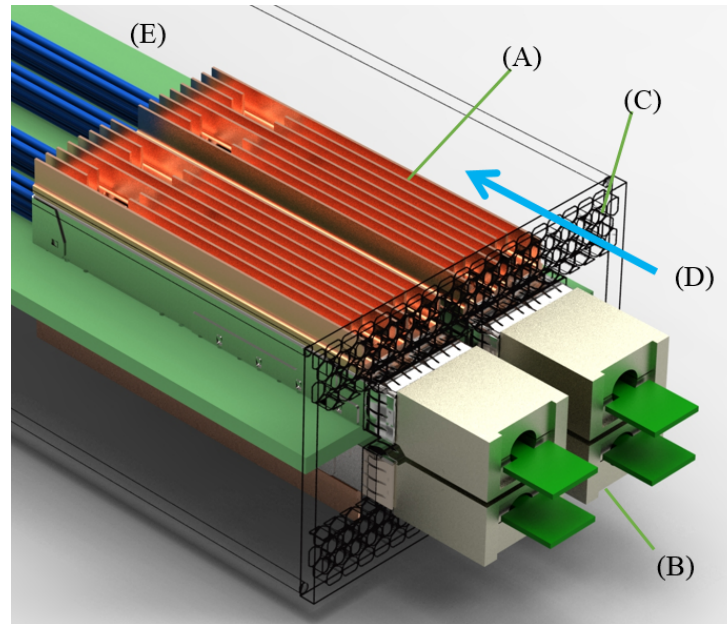


Figure 3. – Test Setup: (A) Samtec FQSFP-DD Cage connector and heatsink, (B) Multilane QSFP-DD heater modules excited to 7 Watts, (C) 80% Open Grill, (D) Direction of Airflow which is 800LFM measured at a cross section about (E).

Figure 4 shows the temperature profile within the module/cage/heatsink assembly. The heat is not getting distributed effectively to the shell and is not being directed to the module/ heatsink interface.

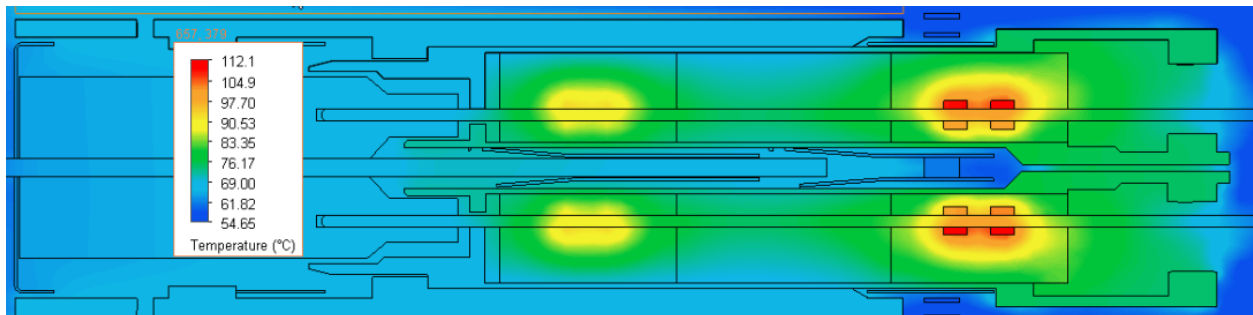


Figure 4. – Temperature profile from simulation

Referring to Figure 5, there are some drawbacks to the heater design which limits its efficacy as a test vehicle. The major issue is how the heat is shunted to the upper shell. When designing an active module, much care is taken to ensure the hotspots on the shell are near the module/heatsink interface. In the ML Heater, the most direct heat paths are to the lower shell. Due to the different compression rates and thicknesses of the thermal interface materials, (D3) and (D4) conduct the heat much better than (D1) and (D2). According to the Dynacast website⁸, the thermal conductivity of Zamak 3, a common alloy used in module shells, is 113 W/m-K, approximately 100x the calculated conductivity of the TIM (Table 3). The conductivity of the shell should have been better leveraged to move the heat.

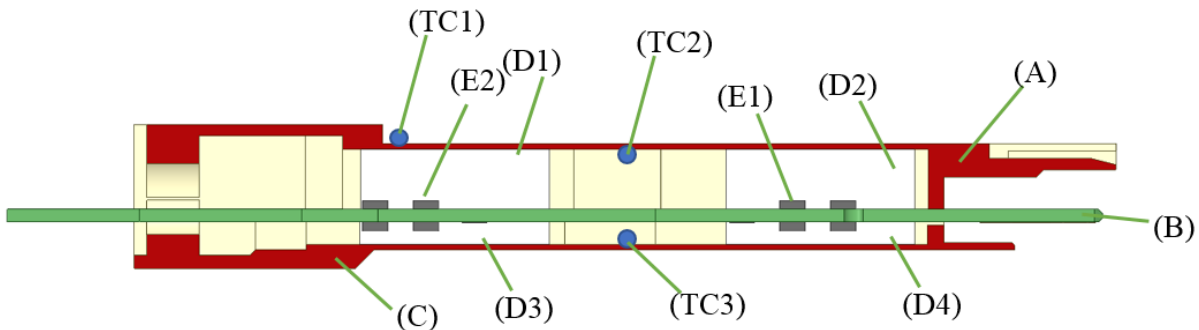


Figure 5. – Cross Section of Multilane QSFP-DD Heater Module: (A) Upper Shell, (B) PCB, (C) Lower Shell, (D1-D4) Thermal Interface Material, (E1-E2) resistor banks for heating on both sides of module PCB, (TC1-TC3) are the thermocouple locations for physical testing.

Table 3

Conductivity of Multilane Heater Module Thermal Interface Material

Pressure	T=2mm	T=5mm
5 psi	1.11 W/m-K	1.17 W/m-K
10 psi	1.19 W/m-K	1.27 W/m-K
15 psi	1.29 W/m-K	1.37 W/m-K

In addition to the structural limitations of the heater module, the airflow bypass about the fins greatly inhibited the heat transfer. In Figure 6 we see that the velocity of the bypass airstreams was in the 9 to 12 m/s, while the air streams in contact with the fins were in the 3 to 6 m/s range.

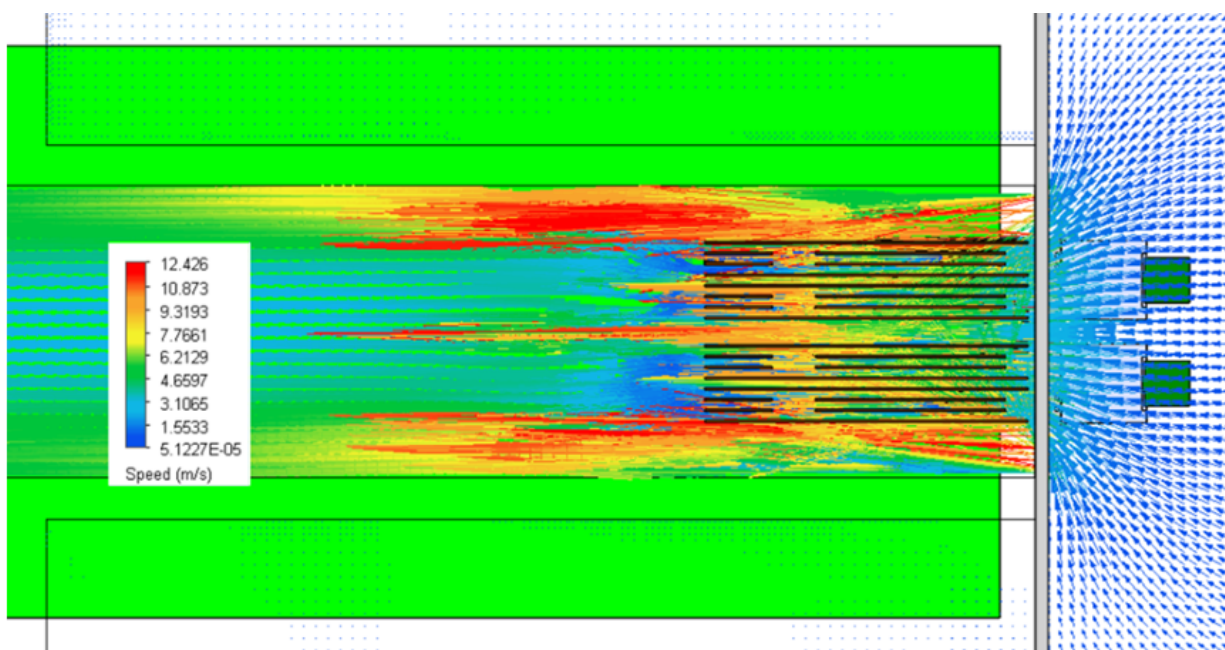


Figure 6. – Velocity profile from simulation

Seeing that there was no way to extrapolate the heatsinks performance due to the bypass the experiment was run again using a single module, cage, and heatsink assembly. An air shield (Figure 7) was rapidly prototyped to cover a portion of the vent in the previous test setup and to bring the air flow channel to within 2 mm of the fin profile (Figure 8). A physical test was run varying the power to the module between 2 w and 14 watts, while varying the air flow rate from 1 to 7 cfm. Figure 9 reports the results of that test normalized as the differential temperature between thermocouple 2 and the ambient inlet temperature. Using Figure 9 a systems engineer can estimate the required ducted airflow needed to maintain a target temperature, given an assumed power load.

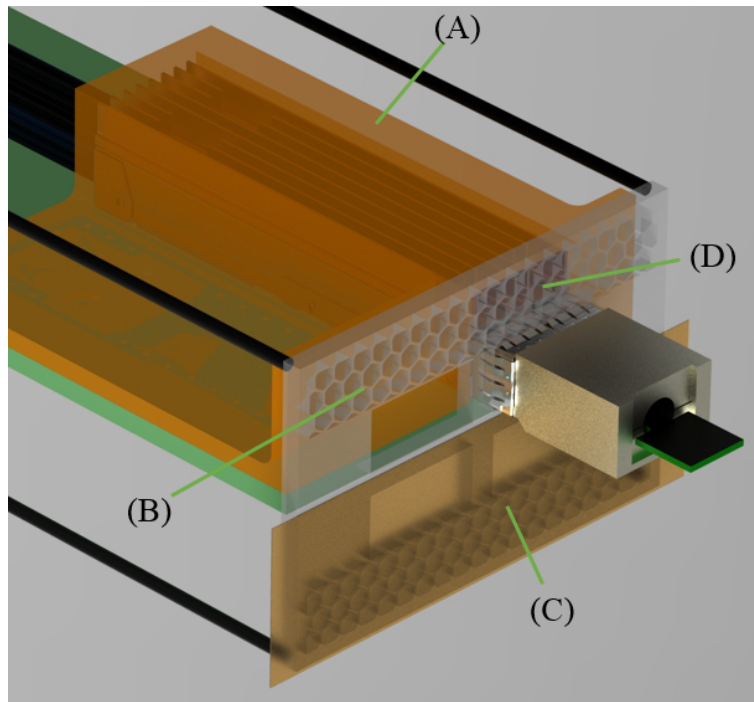


Figure 7. – Second Test Setup: (A) SLA Air Shield; (B) SLA covers open grid; (C) lower grid was covered to force all airflow through (D).

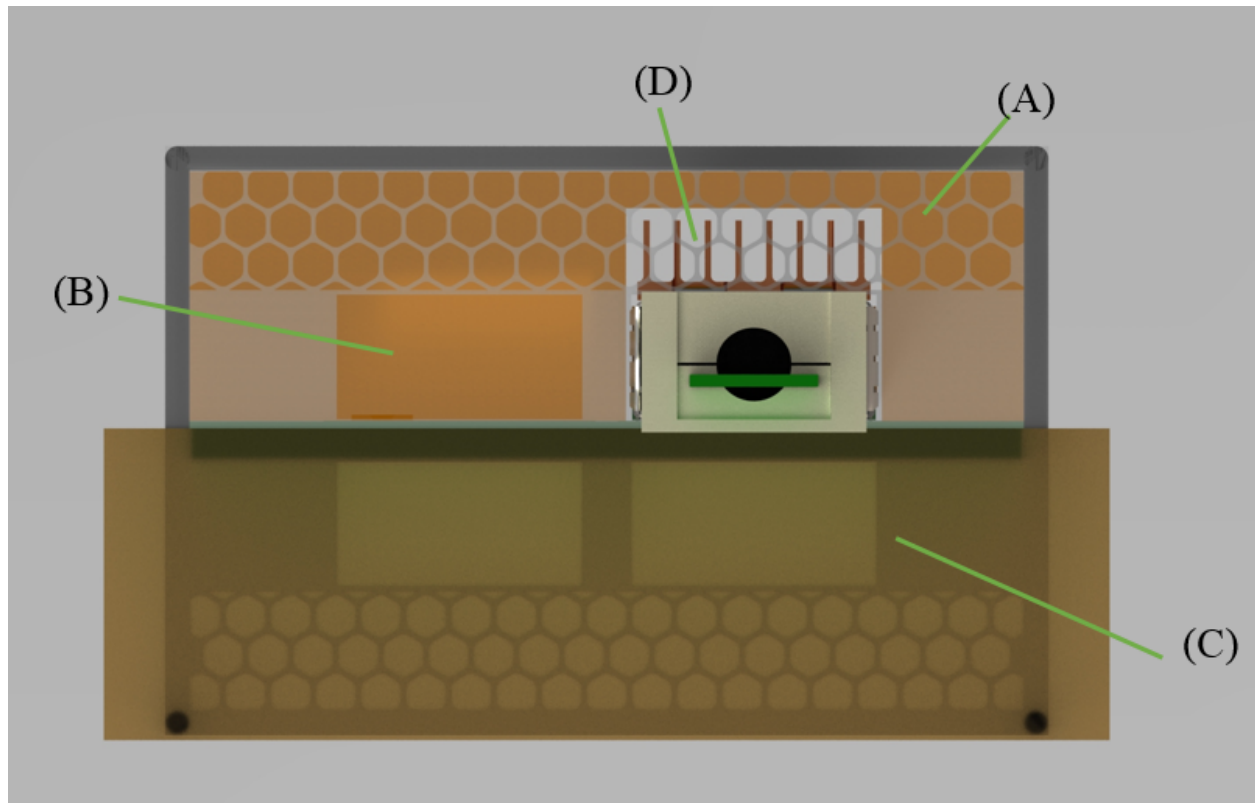


Figure 8. – Second Test Setup: (A) SLA Air Shield; (B) SLA covers open grid; (C) lower grid was covered to force all airflow through (D).

Thermocouple 2 T-Rise from Ambient = F(power,airflow)

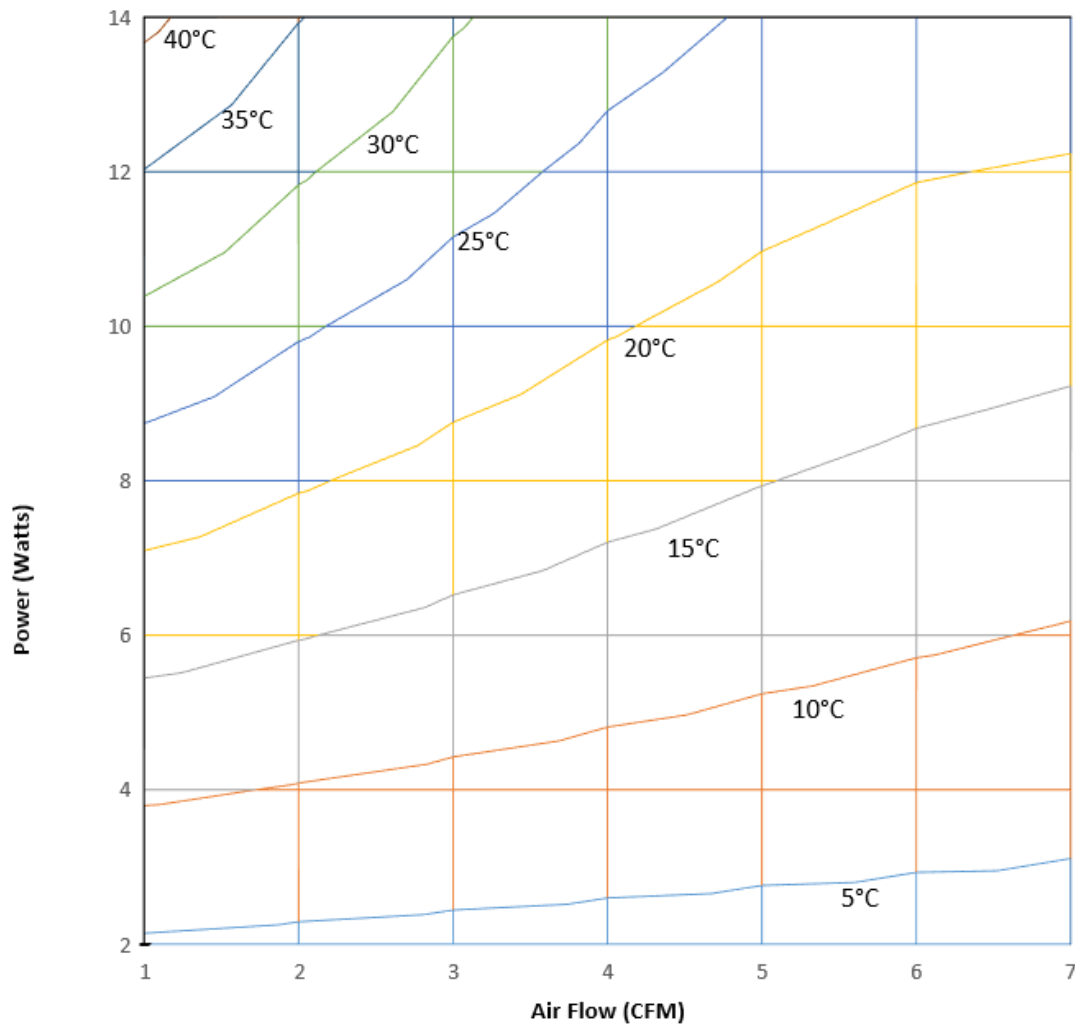


Figure 9. - Results of Second Test: normalized to differential temperature between Thermocouple 2 (inside the upper shell) and the ambient inlet air temperature.

Table 4 shows the relative correlation between the simulated and physical tested temperature. The physical test showed better performance than the simulated, indicating that simulations will lean toward pessimistic results.

Table 4

Correlation of Shell Temperature Simulation to Physical Testing

Location	Simulation	Physical Test
Thermocouple 1	67.53°C	66.43°C
Thermocouple 2 (Heat Sink Window)	68.57°C	61.6°C
Thermocouple 3	75.47°C	71.0°C

2.4 Thermal Reference Design of a Rack Switch System

As a basis of our reference design we will use the Facebook Wedge 100S³. (Figure 10) The design and specifications of that system are offered royalty free through the Open Compute Project. The Samtec wedge reference design (Figure 11) arranges each of the major subsystems into their own module. This modularity allows for improved signal integrity by routing over coax the high-speed signal from the IO module to the stitching ASIC module. This modularity also allows for improved air flow control through the assembly to better manage the thermals.

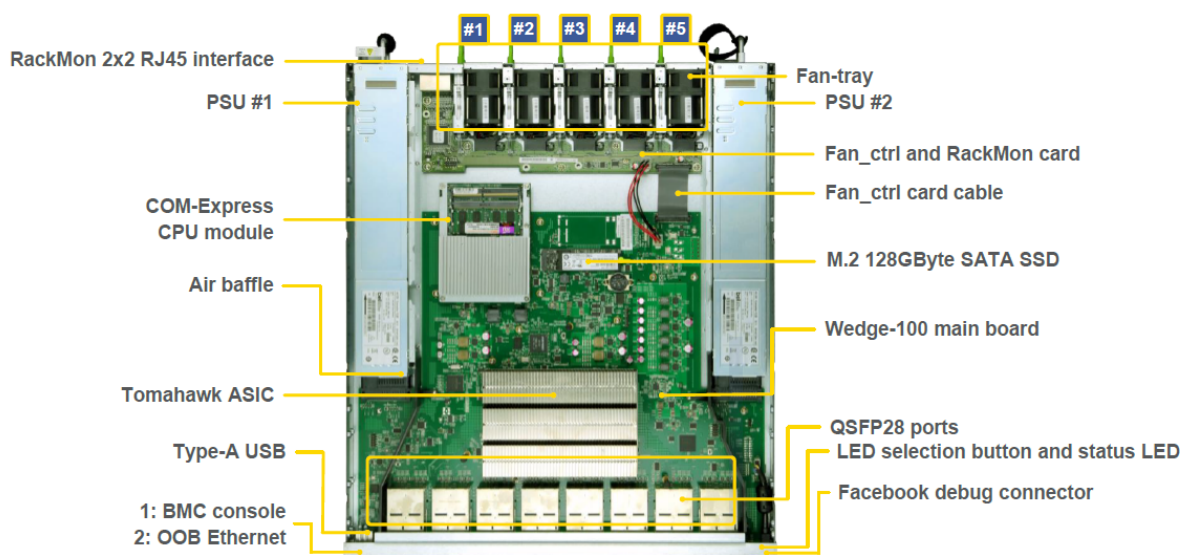


Figure 10. – Top View of Facebook Wedge 100S. From Facebook Wedge 100S Rev 1.3, Figure 3, January 2017.

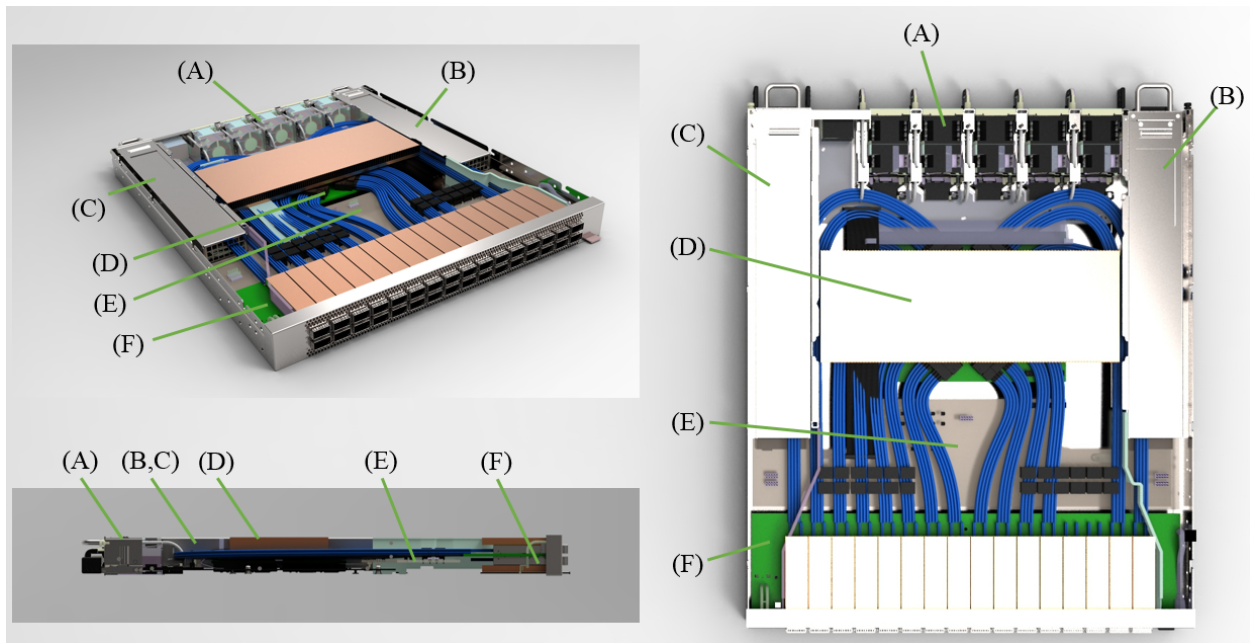


Figure 11. – Conceptual Architecture: (A) Fans (B,C) Power Supply Units, (D) Switching ASIC Module, (E) CPU and Power Distribution Module, (F) IO Module with 32 Samtec FQSFP-DD routed via 34 AWG twinax cable to the (D) switch ASIC.

Figure 12 shows how the modules divide the air flow into an upper airstream and lower airstream. The cable routing from the IO module to the Switch ASIC module, is captured between the power distribution/cpu module and a sheet metal air diverter. This reduces the pressure drop due to turbulence induced by the cables, and simplifies the system for simulation.



Figure 12. – Air flow paths: (1) Upper Route; (F) through the FQSFP-DD, bypass the CPU board (E) by a cable management panel, through the ASIC Heatsink (D), and through the Fan (A): (2) Lower Route; (F) through the FQSFP-DD, cooling CPU board (E), bypassing the ASIC Heatsink (D), and through the Fan (A).

The initial question in the system is on the volumetric capacity of the fans to provide adequate airflow for cooling the FQSFP-DD's. Figure 13 is the PQ Curve for counter rotating fan Delta GFB0412EHS-DA06, which was recommended in the Facebook Wedge 100S OCP Specification. Assuming the pressure drop of between 0.5 and 2 inches H₂O, the flow rate range would be approximately 20 to 30 CFM. That flow rate would equate 100 to 150 CFM for the system, or 3.2 to 4.7 CFM per QSFP-DD module average. Referring to Figure 9, for a 14 watt QSFP-DD module, and a target heatsink/module interface temperature of 70°C, the ambient temperature would need to be in the 40°C to 45°C range.

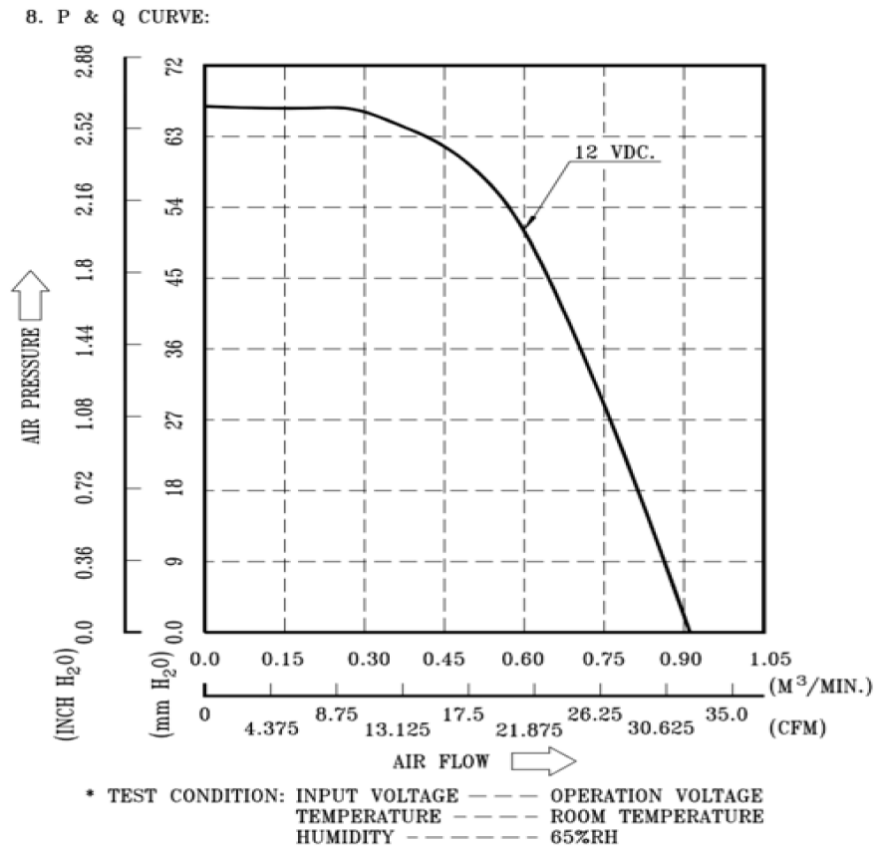


Figure 13. – PQ Curve for counter rotating fan Delta GFB0412EHS-DA06

2.5 Simulation and Correlation

Simulations were run to predict the pressure drop more accurately, determine the velocity field and the relevant temperatures. Figure 15 shows the velocity field through the upper row of the FQSFP-DD's. The linear velocity in the FQSFP-DD heat sink area is about 12.3 m/s, which equates to 2.74 cfm. Referring to Figure 9, at 14W and 2.74 cfm we should see about a 31°C temperature rise above ambient. The simulation results showed a 29-31°C increase in temperature from ambient, a close match to the chart predicted results.

2.6 Improvement to Increase Allowable Ambient Temperature

To increase the allowable ambient temperature, two tactics were employed. First is to increase the surface area of the heatsink, second is to increase the velocity through the heatsink. To increase the area the design was re-spun to a zip fin design (Figure 14) that allowed the number of fins to be more than doubled. However, by increasing the number of fins, the air flow was expected to decrease due to an increase in surface friction so a different fan was specified. Figure 15 shows a comparison of PQ curves for various fans available through Digikey. The Sanyo 9CRH0412P5J001 was specified because at the earlier simulated pressure drop range there is a reported increase in flow of 10 cfm per fan, or 50 cfm for the system. Additionally, because there is an expected increase in the pressure drop, the Sanyo was chosen because there was little expected reduction in flow with the pressure increase.

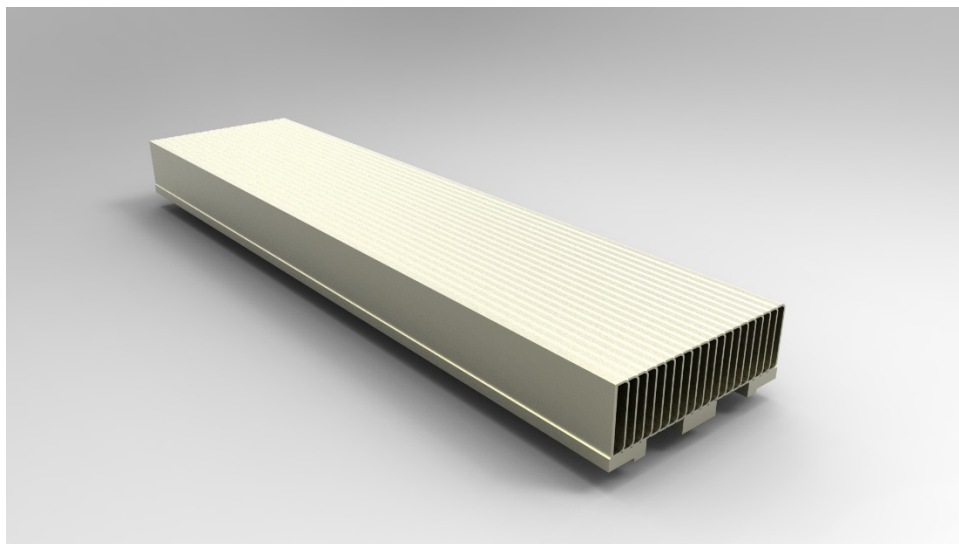


Figure 14. – Zip Fin Heatsink

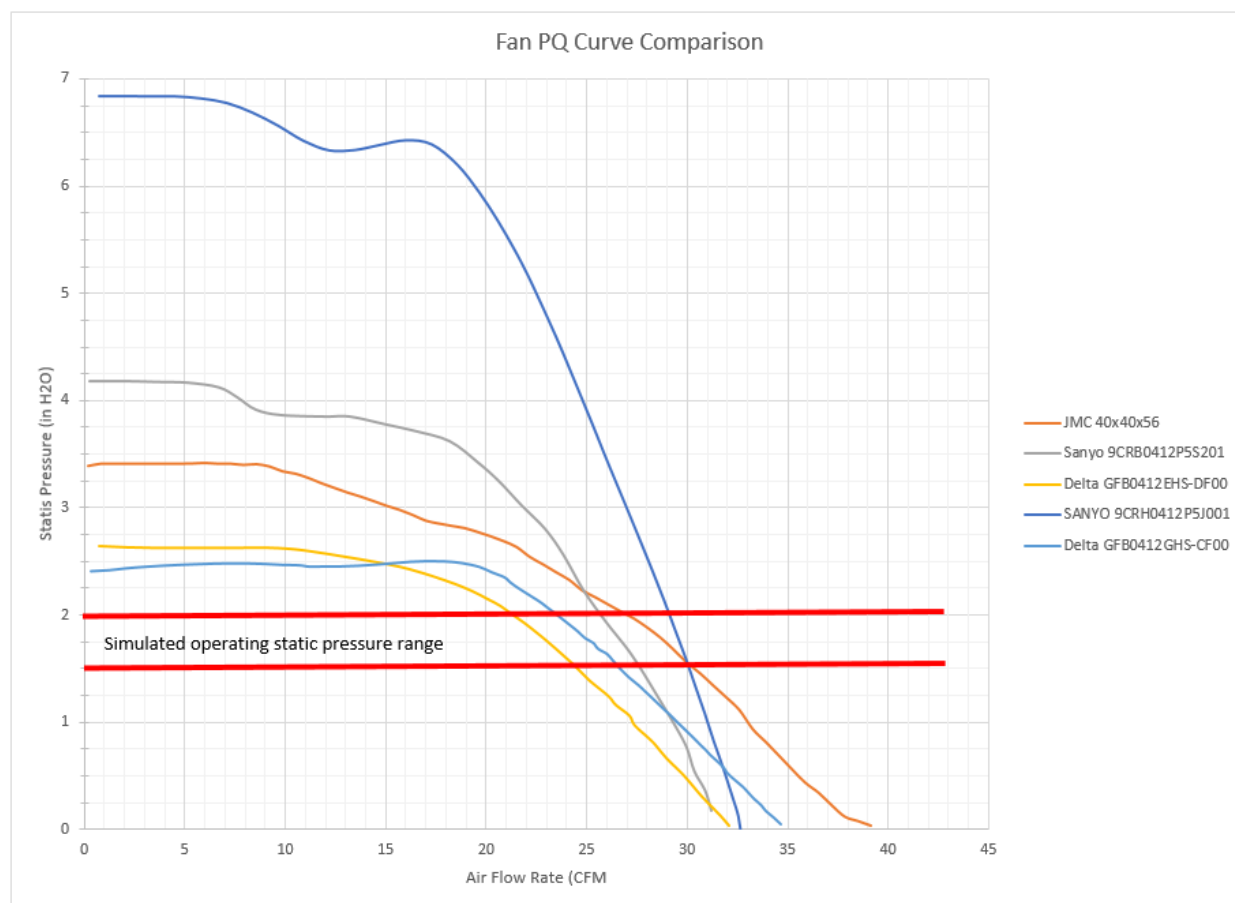


Figure 15. – Comparison of various 40mm X 40mm X 56mm Fan PQ Curves.

Simulation of the system (Table 5) showed a mere 11.8°C of the thermal interface over ambient allowing for applications with an ambient of 55°C with margin.

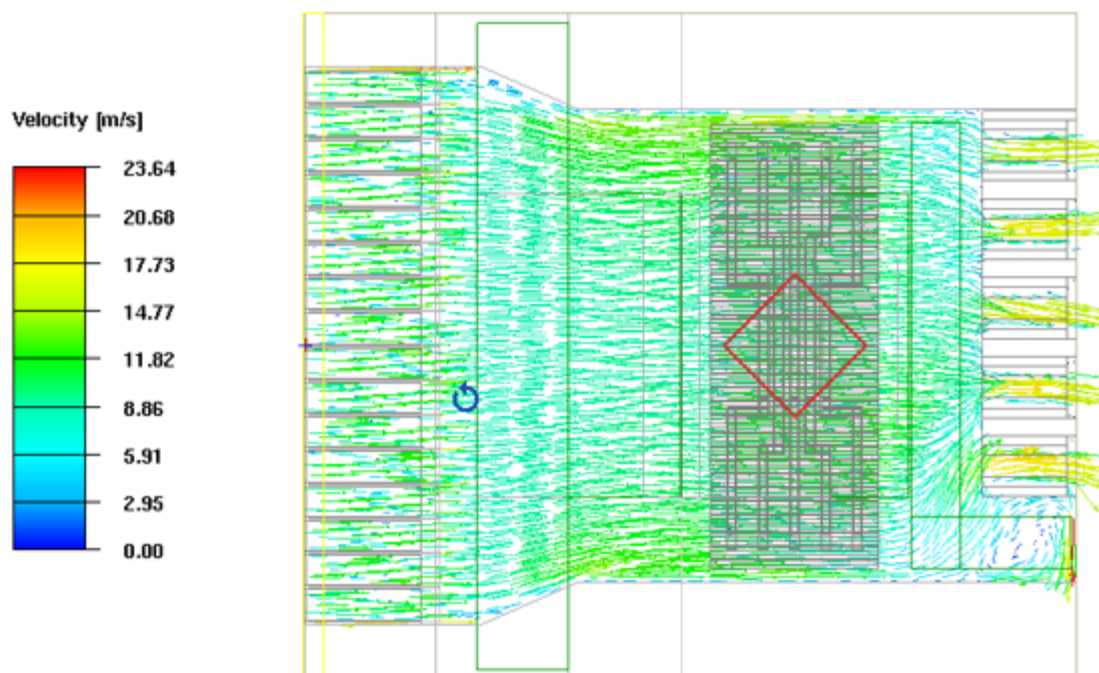


Figure 16. – Velocity Simulation Results, Samtec modular switch architecture.

Table 5

Simulation Results for Zip Fin Configuration

Top Row								
QSFP-DD Port	1	2	3	4	5	6	7	8
Temp Increase °C	11.1	11.0	11.1	11.0	11.0	11.0	11.0	11.0
QSFP-DD Port	9	10	11	12	13	14	15	16
Temp Increase °C	11.0	11.0	11.0	11.0	11.0	11.0	11.1	11.0
Bottom Row								
QSFP-DD Port	17	18	19	20	21	22	23	24
Temp Increase °C	11.5	11.6	11.7	11.7	11.7	11.7	11.8	11.8
QSFP-DD Port	25	26	27	28	29	30	31	32
Temp Increase °C	11.8	11.7	11.7	11.6	11.6	11.6	11.6	11.5

2.7 Continuing Work

With Samtec's novel heatsink and cage design, more exotic cooling methods can be employed. The springs are spaced so a heat pipe can be run along the length of the heat sink to dump the heat in a secondary heatsink. A thermo electric cooler can be used to move the heat from the module. Additionally, the heat sink system can use fluid cooling to manage the heat.

We are in the process of prototyping the Zip Fin version of the heatsink, and are planning to characterize the heat sink and generate a performance map similar to Figure 9.

2.8 Conclusions

Samtec's FQSFP-DD is uniquely positioned to answer the needs of a wide variety of applications, not only from the bandwidth, but also from the thermal perspective. We have a design capable of tiered thermal solutions. From simple extruded and machined heatsinks, to zip fin, to heat pipes, and fluidics. And we have partnered with industry leaders in thermal management to take on, and manage any application specific design and manufacturing of thermal solutions for the FQSFP-DD.

3 Footnotes

¹ QSFP-DD MSA, "Accelerating 400GbE Adoption with QSFP-DD", March 2017, <http://www.qsfp-dd.com/wp-content/uploads/2017/03/QSFP-DD-whitepaper-15.pdf>, accessed December 15, 2017.

² QSFP-DD MSA, "QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER", Revision 3.0 September 2017, <http://www.qsfp-dd.com/wp-content/uploads/2017/09/QSFP-DD-Hardware-rev3p0.pdf>, accessed December 15, 2017.

³ Open Compute Project, Networking Working Group, Facebook Wedge 100S 32x100G, Revision 1.0, February 2017, <http://www.opencompute.org/wiki/Networking/SpecsAndDesigns>, accessed December 15, 2017.

⁴ Atmel Atmega328/P 8-bit AVR Microcontroller, http://www1.microchip.com/downloads/en/DeviceDoc/Atmel-42735-8-bit-AVR-Microcontroller-ATmega328-328P_Datasheet.pdf, accessed December 15, 2017.

⁵ Phillips Photonics, <http://www.photonics.philips.com/pdf/VCSEL-ULM850-14-CHIPS.pdf>, accessed December 15, 2017.

⁶ QSFP-DD MSA, Power Classes and Maximum Power Consumption, Section 4.2.1, Revision 3.0 September 2017.

⁷ QSFP-DD MSA, Thermal Requirements, Section 6.1, Revision 3.0 September 2017.

⁸ Zamak 3 Physical Properties, <https://www.dynacast.com/zamak-3>, accessed December 19, 2017

⁹ Mack, B., and Graham, T., "Pluggable Optics Module – Thermal Specifications, Part 1," Electronics Cooling, June 2016, <https://electronics-cooling.com/2016/07/pluggable-optics-modules-thermal-specifications-part-1/>, accessed December 15, 2017.

¹⁰ Mack, B., and Graham, T., "Pluggable Optics Module – Thermal Specifications, Part 2," Electronics Cooling, October 2017, <https://www.electronics-cooling.com/2016/10/pluggable-optics-modules-thermal-specifications-part-2/>, accessed December 15, 2017.

¹¹ Open Compute Project, Networking Working Group, Facebook Wedge 100S 32x100G Specification, Revision 1.3, January 2017.

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