Designing DC-Blocking Capacitor Transitions to Enable 56Gbps NRZ & 112Gbps PAM4

Scotty Neally, Samtec Teraspeed Consulting
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Speakers

Scotty Neally

Signal Integrity Consultant
Samtec Teraspeed Consulting

Scotty Neally is an experienced signal integrity consultant with a background in high density PCB design and measurement, automation of signal integrity design flows, and currently focuses on system design for emerging technologies.

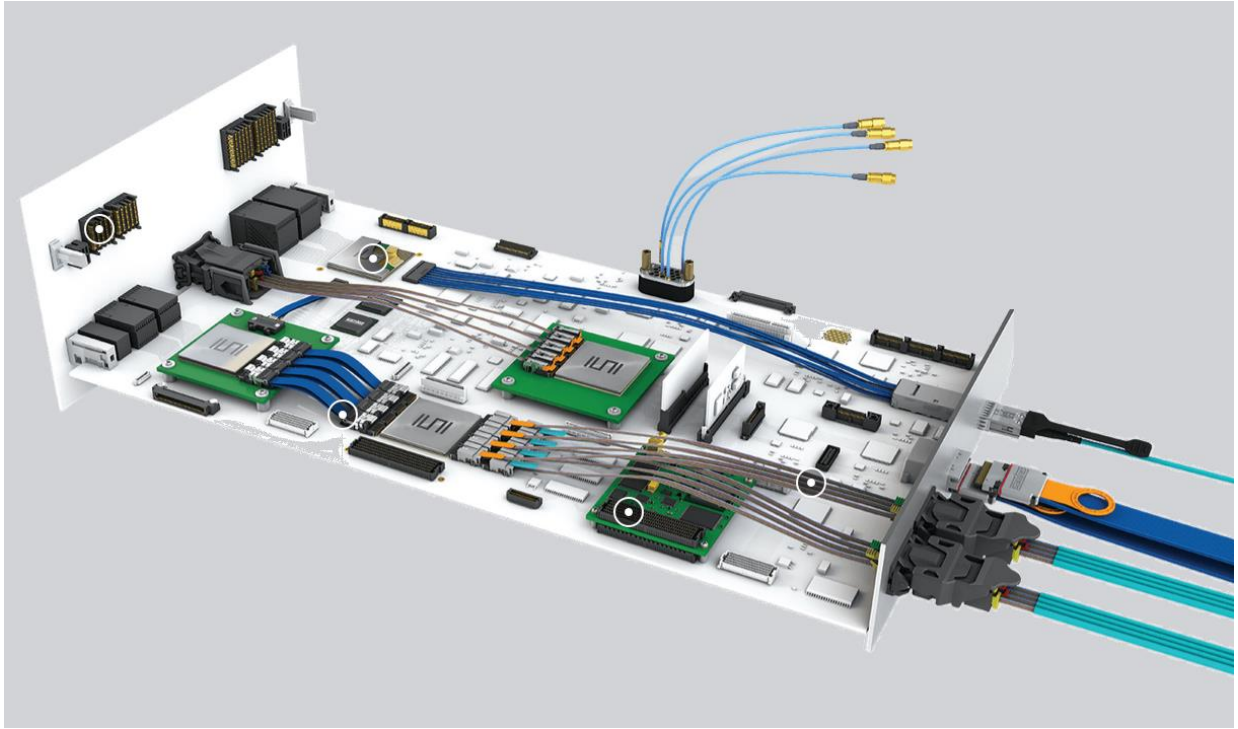
Scott McMorrow

CTO, Signal Integrity Products
Samtec Teraspeed Consulting

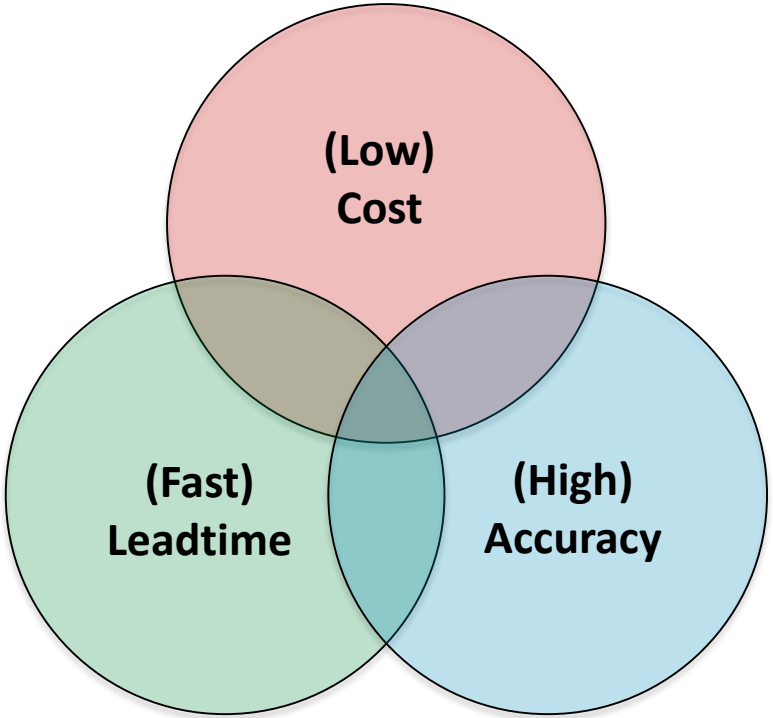
Scott McMorrow is an expert in high-performance design and signal integrity engineering, with a broad background in complex system design, interconnect and signal integrity engineering, modeling and measurement methodology, and professional training, spanning over 25 years.

System Design

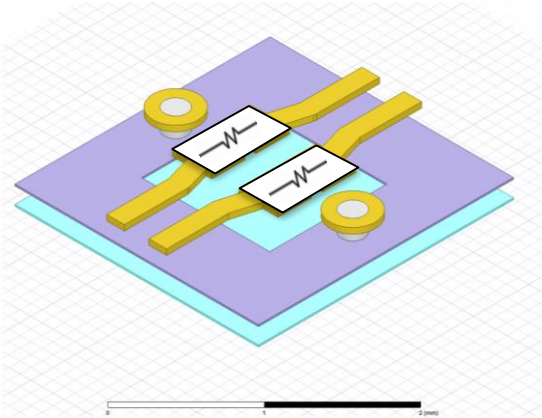
- **Tradeoffs**
  - Cost
  - Leadtime
  - Performance
    - *Reliability*



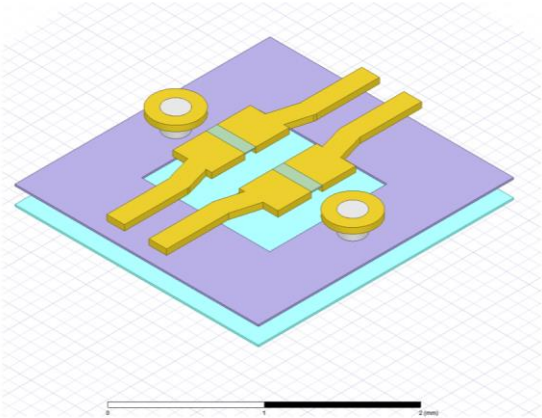
Decision Diagram



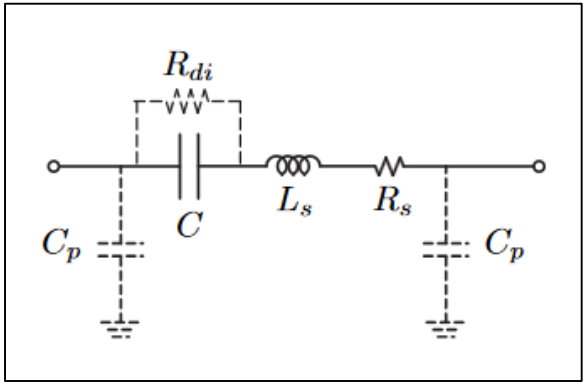
Traditional Capacitor Models



Shorting Resistor

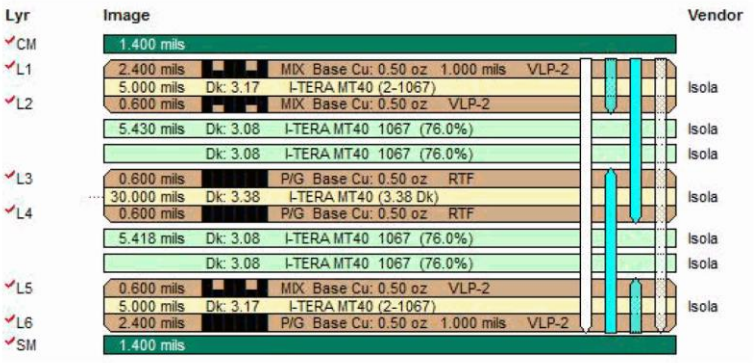


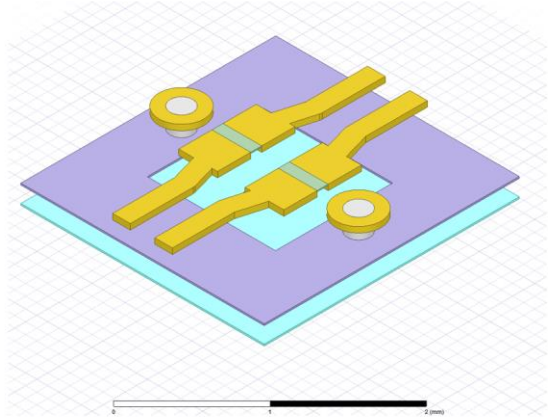
PEC Plane

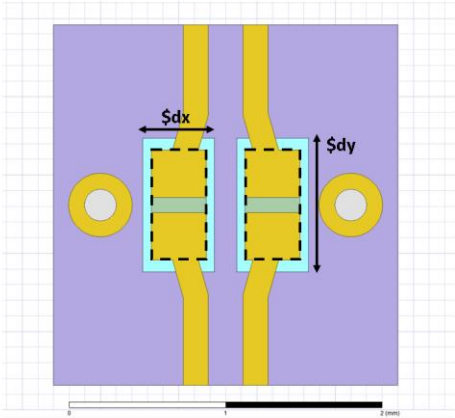


RLC Model

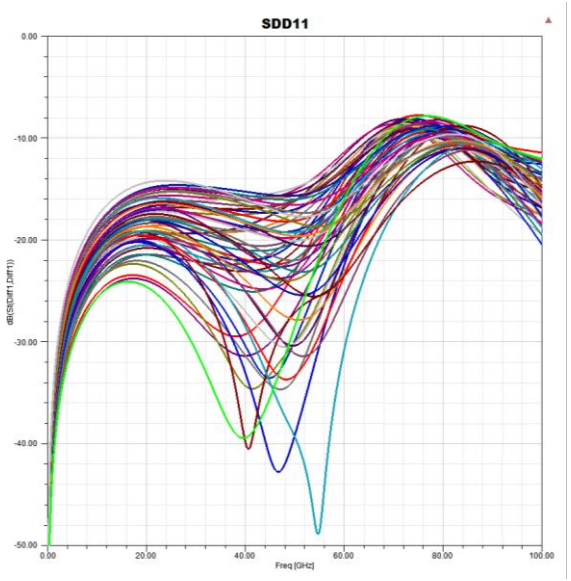
DC Blocking Capacitor Design Layout

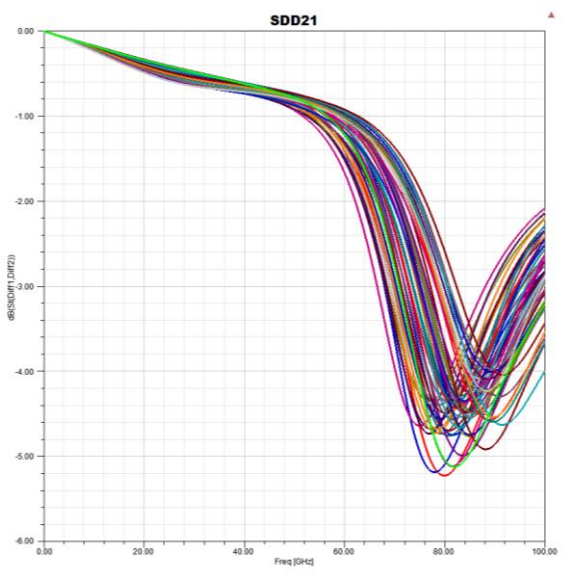


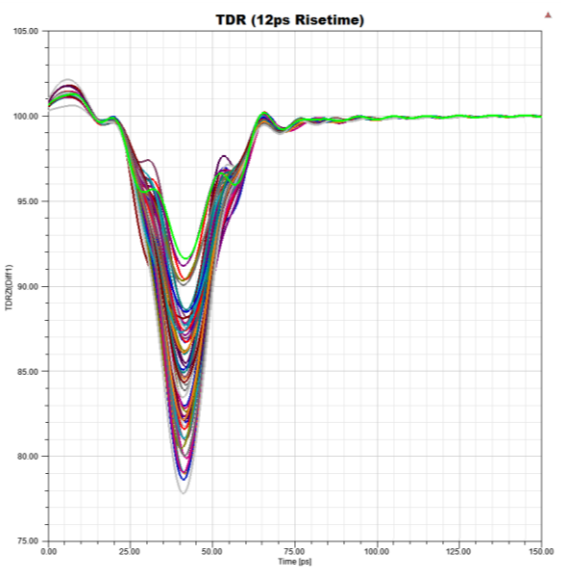




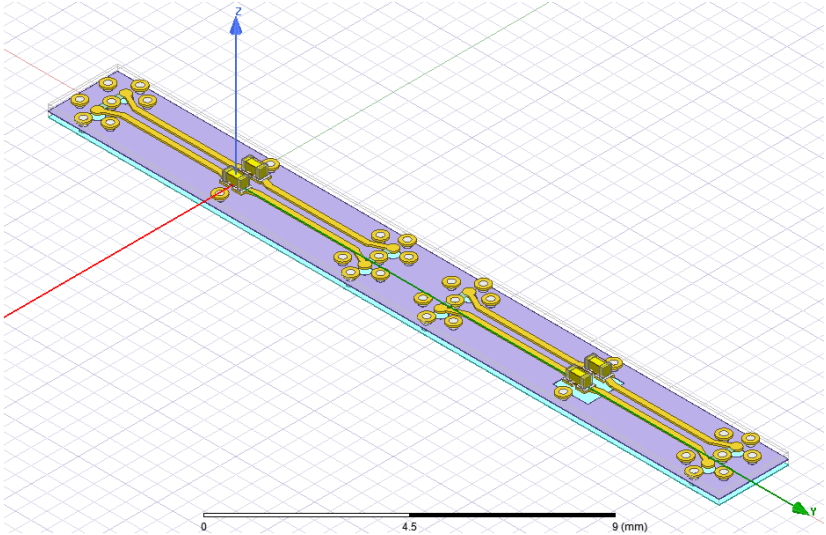
Design Optimization



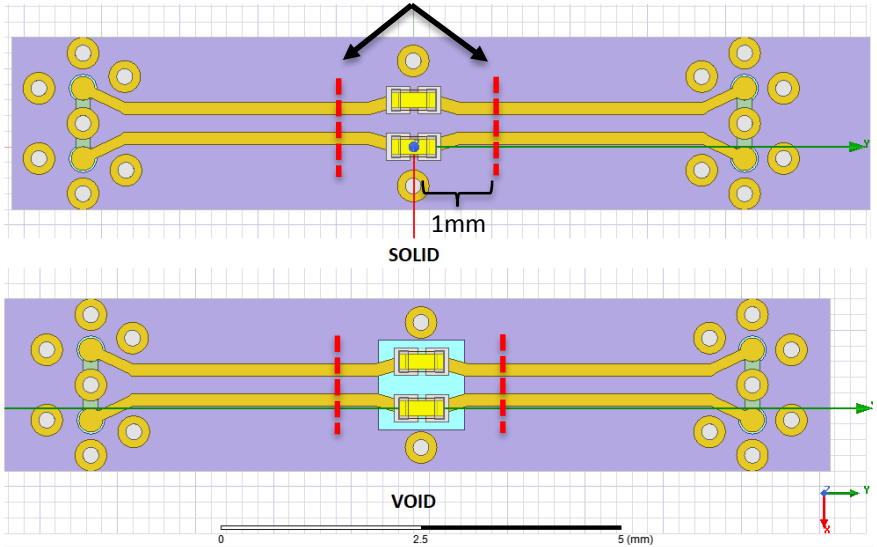




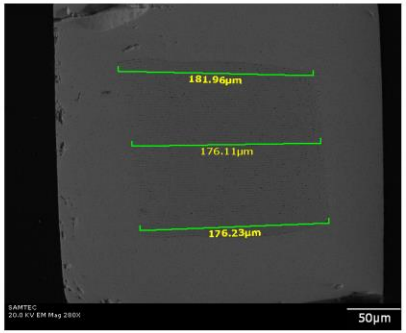
Test Vehicle Preview



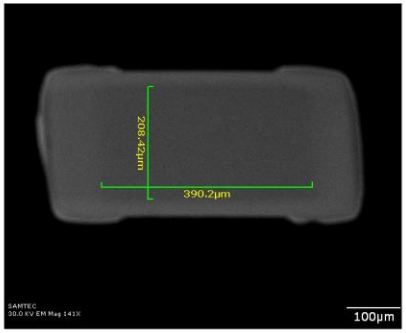
De-embedded Reference Plane



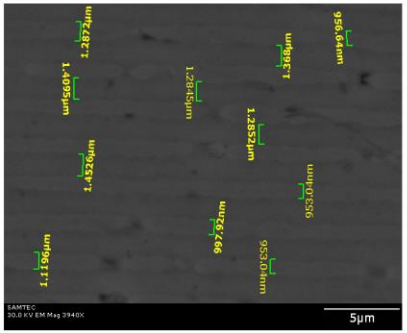
MLCC SEM Measurements



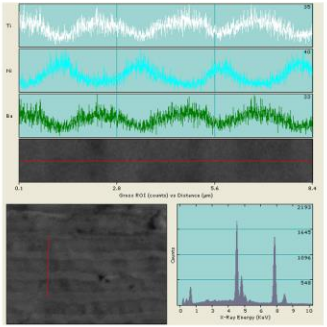
A. Side View



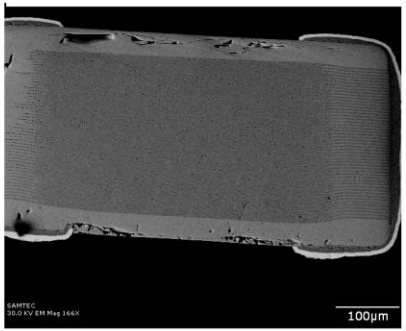
B. Top View



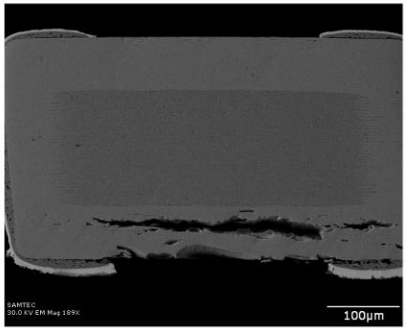
C. Cross-Section



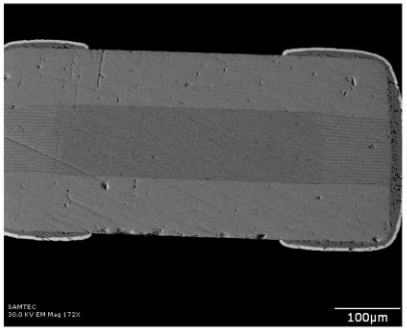
D. Line Scan



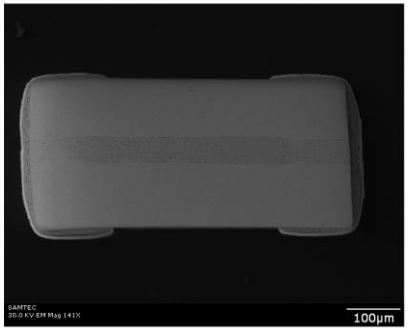
E. 220nF Front View



F. 150nF Front View



G. 47nF Front View



H. 22nF Front View

HFSS Model

$$C = \frac{E_o * E_r * n * A}{d}$$

C = capacitance

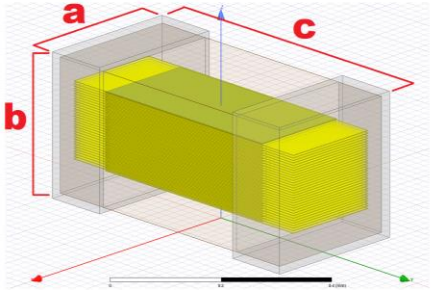
E_o = vacuum permittivity

E_r = relative dielectric constant

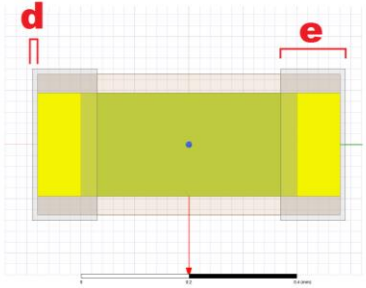
n = number of layers (n + 1 electrodes)

A = area of electrode overlap

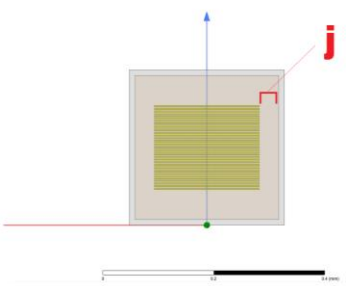
d = dielectric thickness between layers



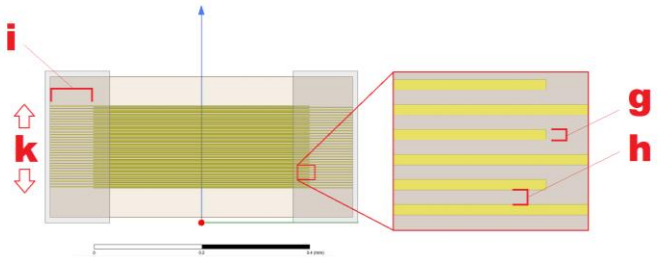
A. Isometric View



B. Top View



C. Side View



D. Front View

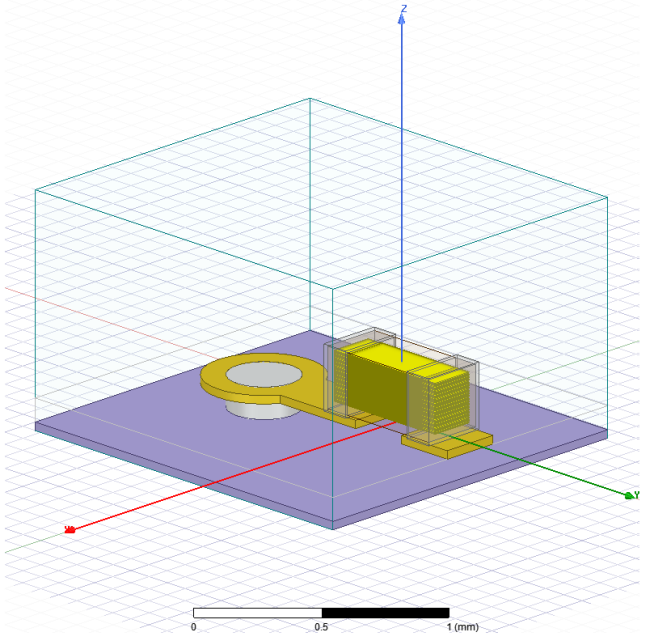
	Name	Value	Unit	Evaluated Value
a	$cap_w	300um-2*$shell_thk		280um
b	$cap_h	300um-2*$shell_thk		280um
c	$cap_l	600um-2*$shell_thk		580um
d	$shell_thk	10	um	10um
e	$shell_depth	120	um	120um
f	$center_h	$cap_h/2		140um
g	$plate_thk	1	um	1um
h	$plate_sep	1.4	um	1.4um
i	$plate_clear	80	um	80um
j	$shell_gap	35	um	35um
k	$nPlate	64		64

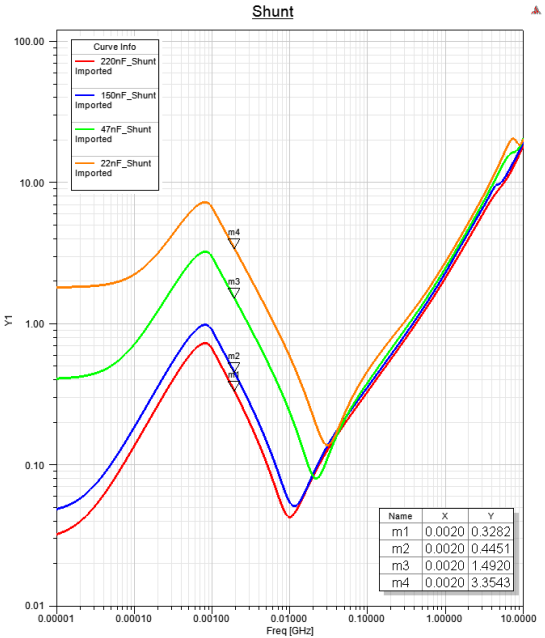
E. Design Variables

Case Size	Capacitor Value (nF)	MFG, P/N	n Plates	Er	Estimated Capacitance (nF)	Tolerance (%)
201	220	TDK, C0603X7S0J224K030BC	90	5000	214.48	-2.51%
201	150	TDK, C0603X7S0J154K030BC	64	5000	151.82	1.21%
201	47	TDK, C0603X7S0J473M030BB	40	2500	46.99	-0.02%
201	22	TDK, C0603X7S0J223K030BB	20	2500	22.89	4.06%

Shunt Simulation

$$C = \frac{1}{2\pi * f * X_c}$$

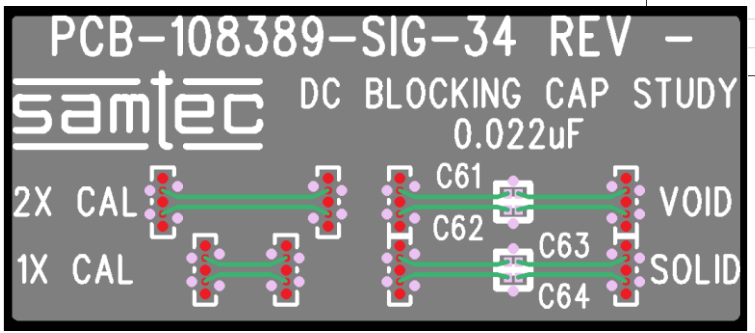


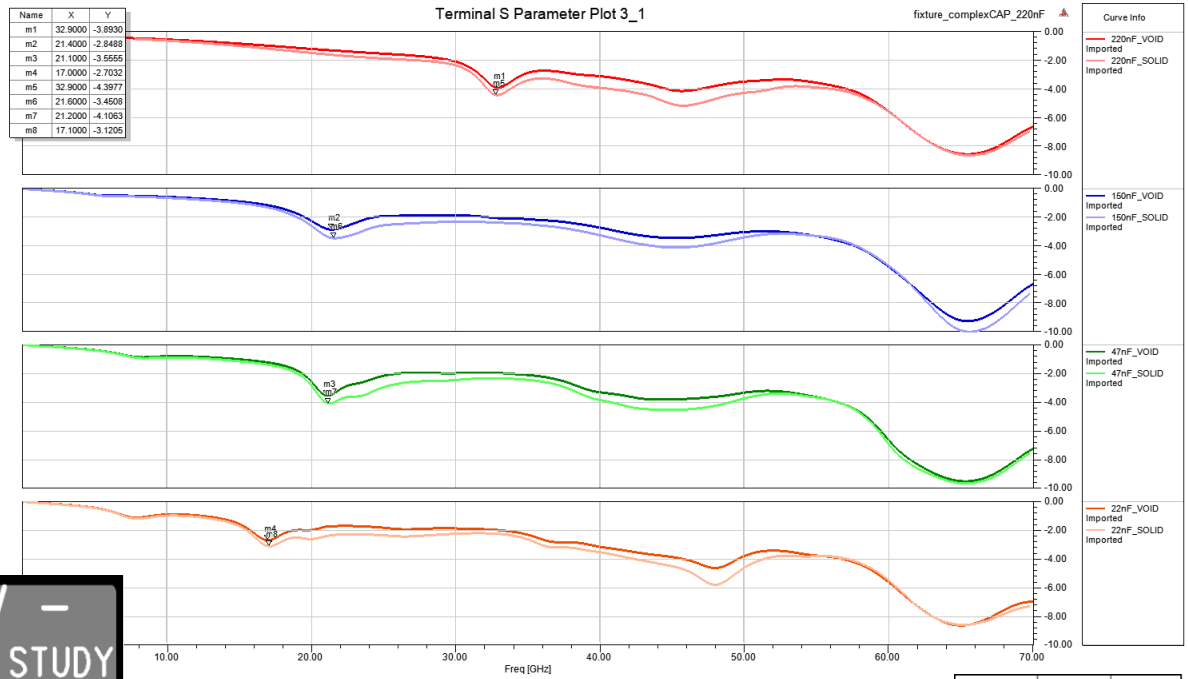


Simulated Reactance X (Ω)	Simulated Capacitance C (nF)	Capacitance Target C (nF)	Difference from Nominal (%)
0.3282	242.47	220	9.3%
0.4451	178.79	150	16.1%
1.4920	53.34	47	11.9%
3.3543	23.72	22	7.3%

0201 PKG Family

- **Using the test vehicle with 4 different capacitor values and 2 structures (VOID & SOLID) we compare the insertion loss of each**
  - 220nF, 150nF, 47nF, 22nF





Name	X	Y
m1	32.9000	-3.8930
m2	21.4000	-2.8488
m3	21.1000	-3.5555
m4	17.0000	-2.7032
m5	32.9000	-4.3977
m6	21.6000	-3.4508
m7	21.2000	-4.1063
m8	17.1000	-3.1205

Capacitor Modeling
Sim to Measurement Comparison

Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

4 & 5

1

2

3

Compare Capacitor Models

1. **SIM 220nF** - All Model Types
2. **SIM 220nF**/**MEAS All Values** Complex Model (VOID)
3. **SIM 220nF**/**MEAS All Values** Complex Model (SOLID)

Channel Exploration

4. **SIM & MEAS 220nF**, Chip to Module Host TX Pkg Only (high loss pkg)
5. **SIM & MEAS 220nF**, Chip to Module Optimistic TX/RX (low loss pkg)

What To Pay Attention To

- How do simulation results vary between modeling structures?
- How do capacitor values for a given case size (0201) affect inductance?
- How does the transition geometry (SOLID vs VOID) impact channel performance?
- What impact does loop inductance have on these geometries?

1. SIM - 220nF Capacitor, All Model Types

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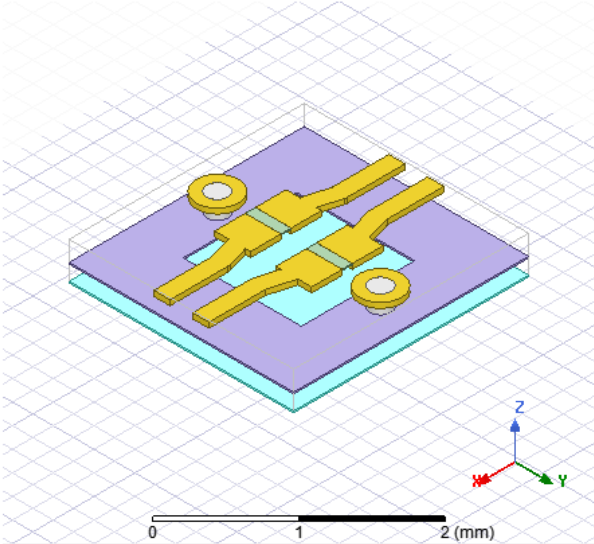
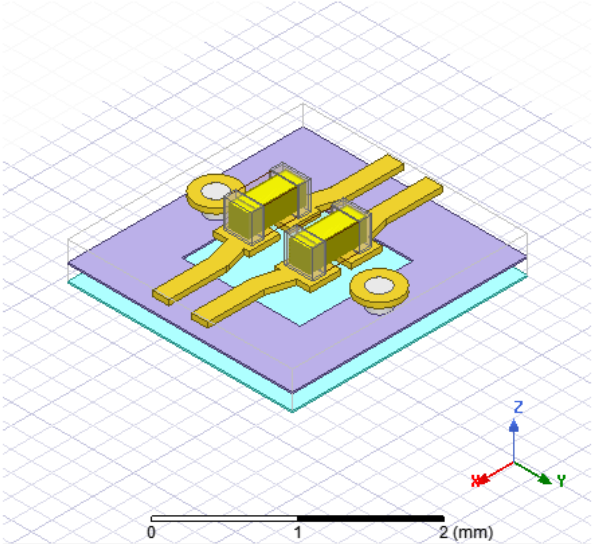
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

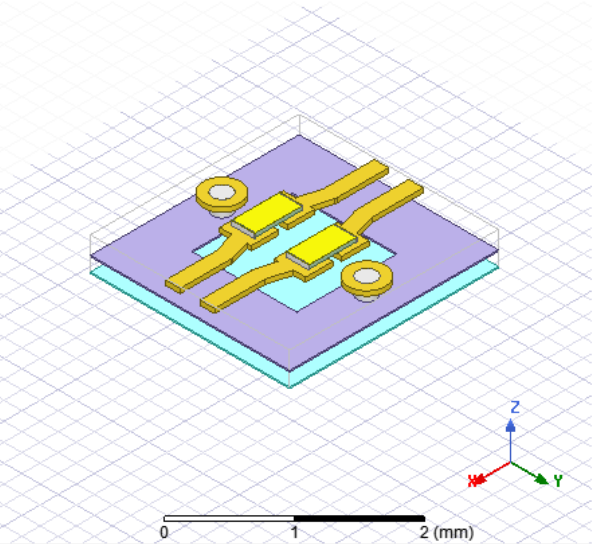
1



SHORT_VOID



COMPLEX_VOID

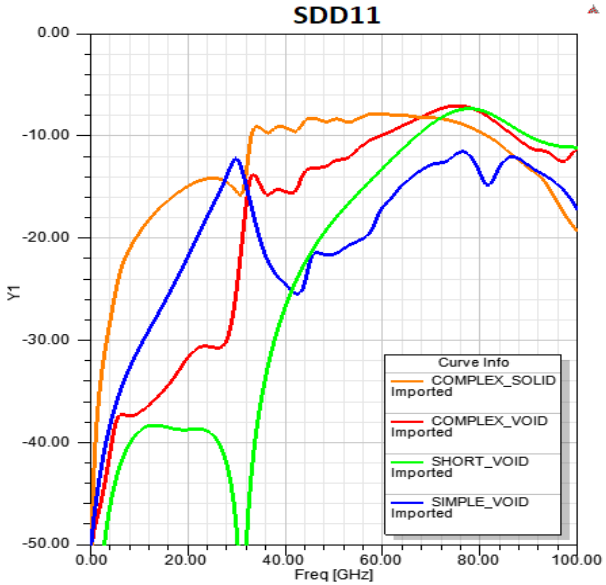


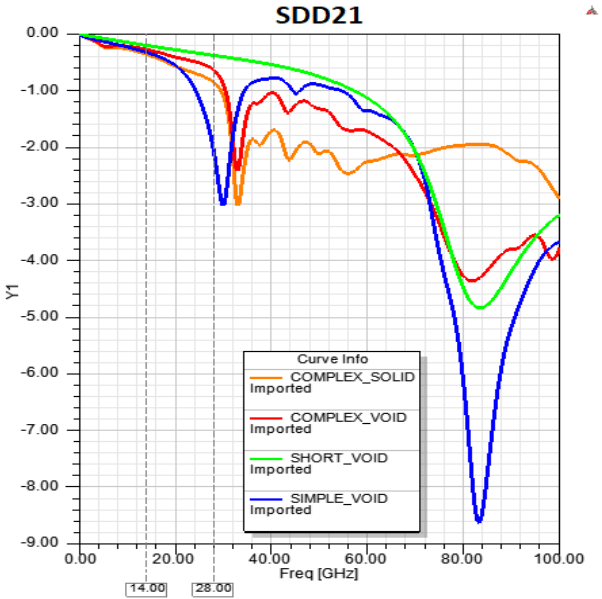
SIMPLE_VOID

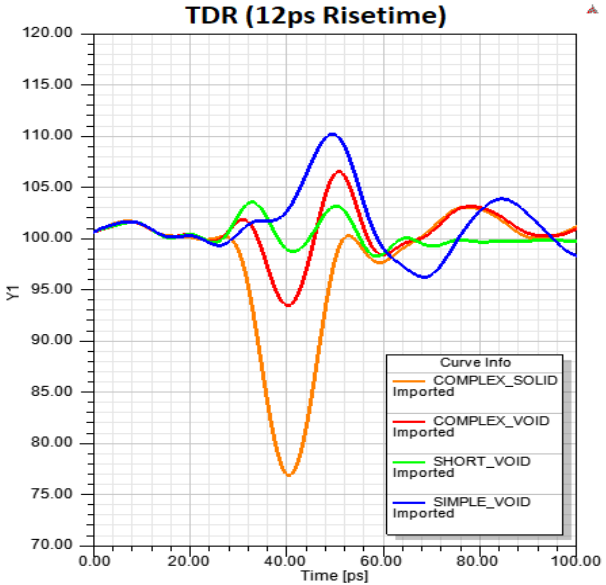
1. SIM - 220nF Capacitor, All Model Types

Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

1

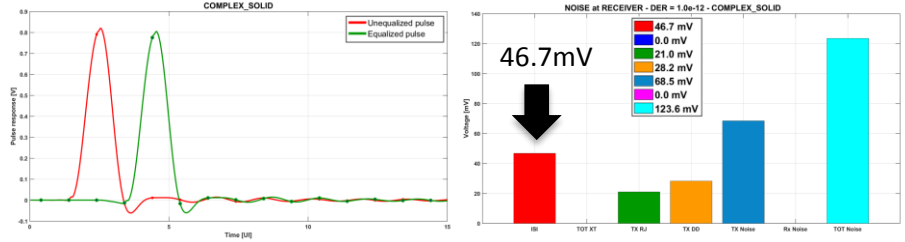




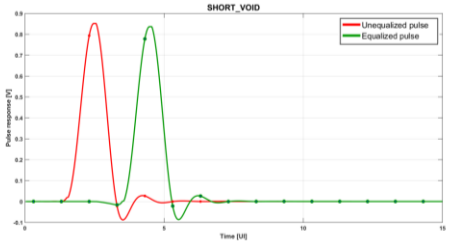


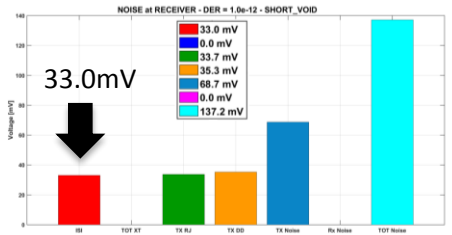
Model Comparison 56G Single Bit Response

COMPLEX_SOLID

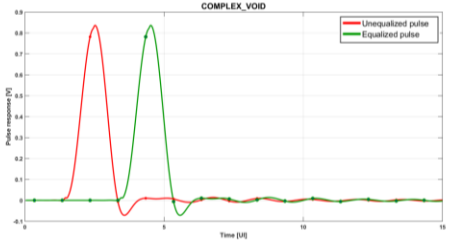


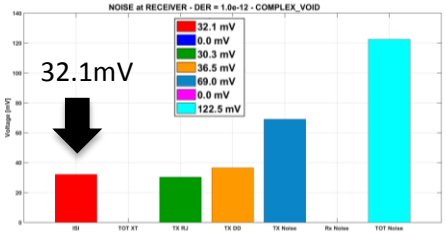
SHORT_VOID



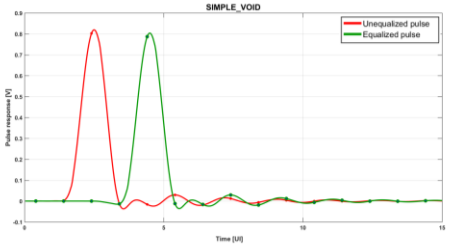


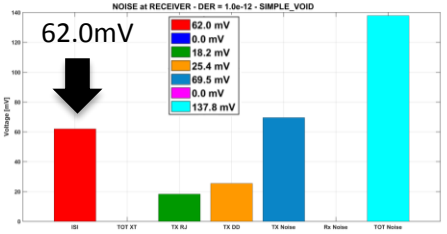
COMPLEX_VOID





SIMPLE_VOID





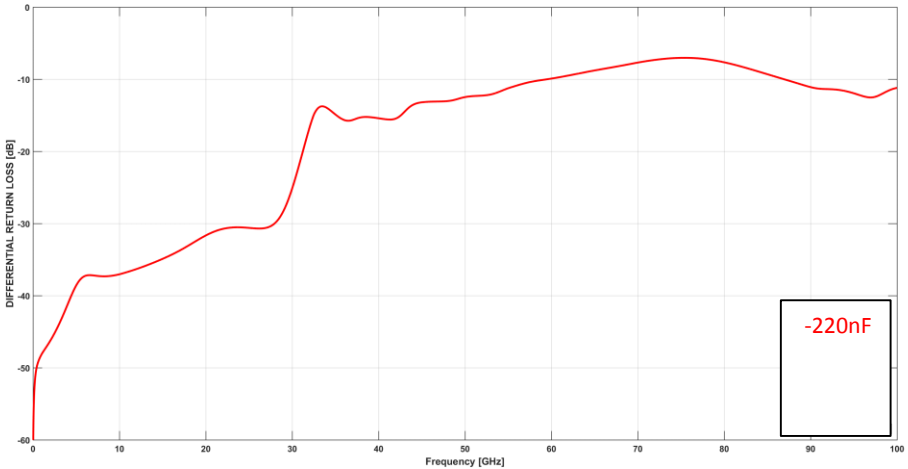
2 & 3. SIM / MEAS - All Measured Values (VOID & SOLID Configuration)

2. SIM vs MEAS – SDD11 (VOID)

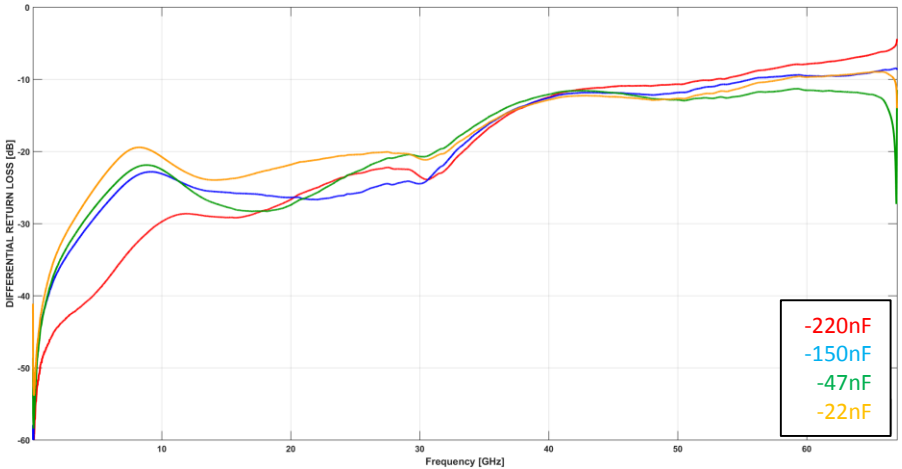
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

2

SIMULATION



MEASUREMENT

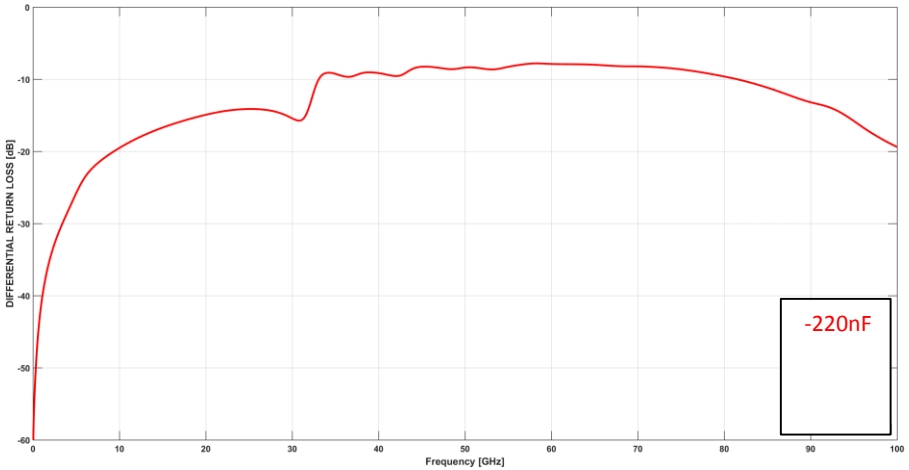


3. SIM vs MEAS – SDD11 (SOLID)

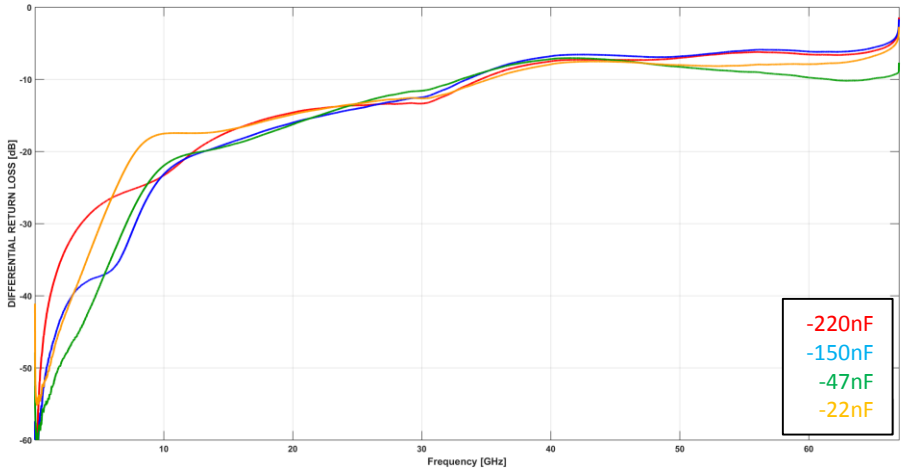
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

3

SIMULATION



MEASUREMENT

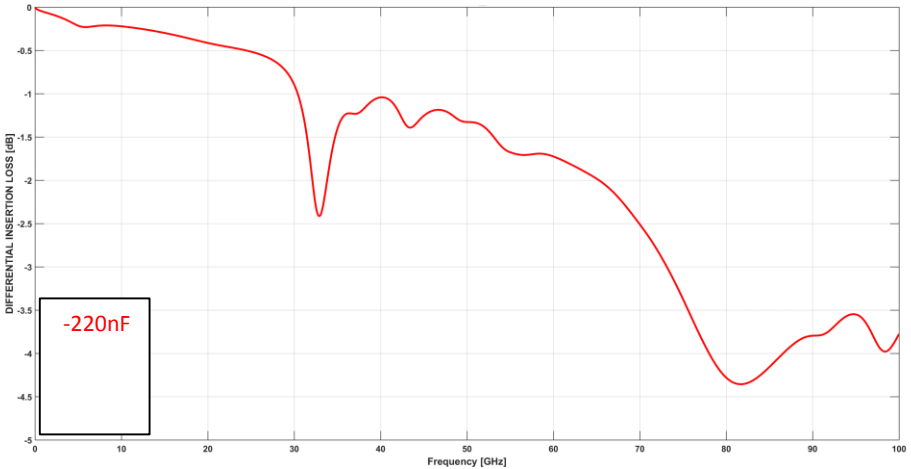


2. SIM vs MEAS – SDD21 (VOID)

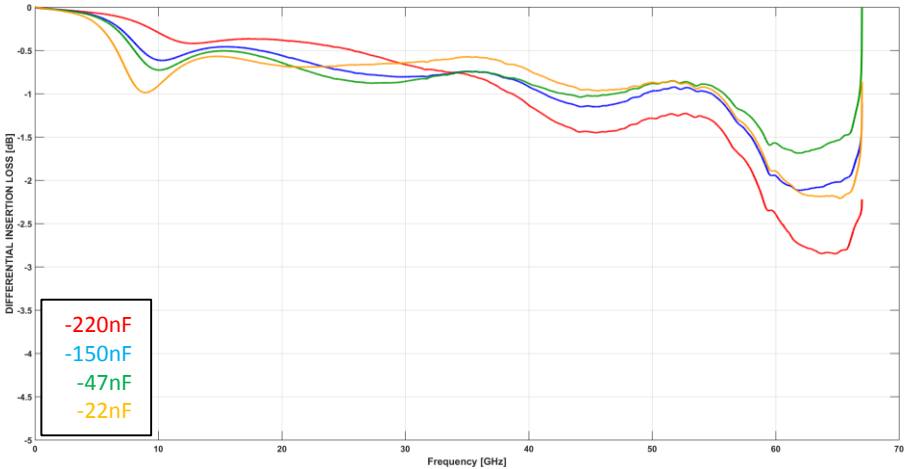
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

2

SIMULATION



MEASUREMENT

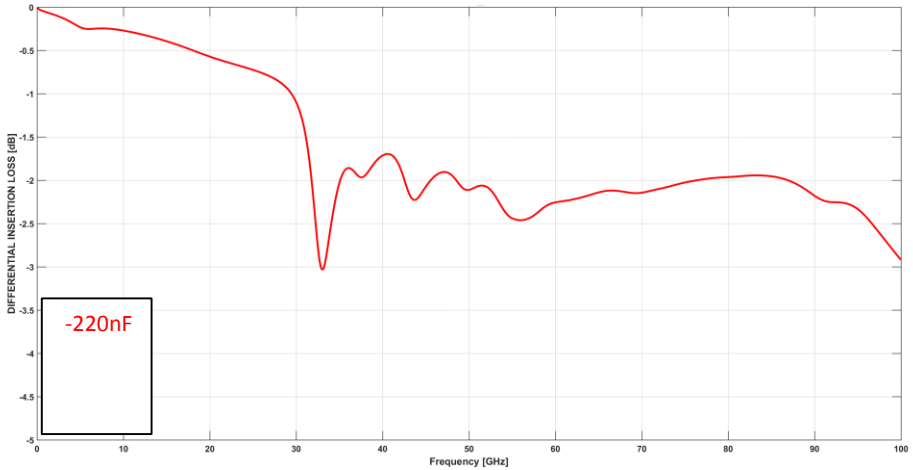


3. SIM vs MEAS – SDD21 (SOLID)

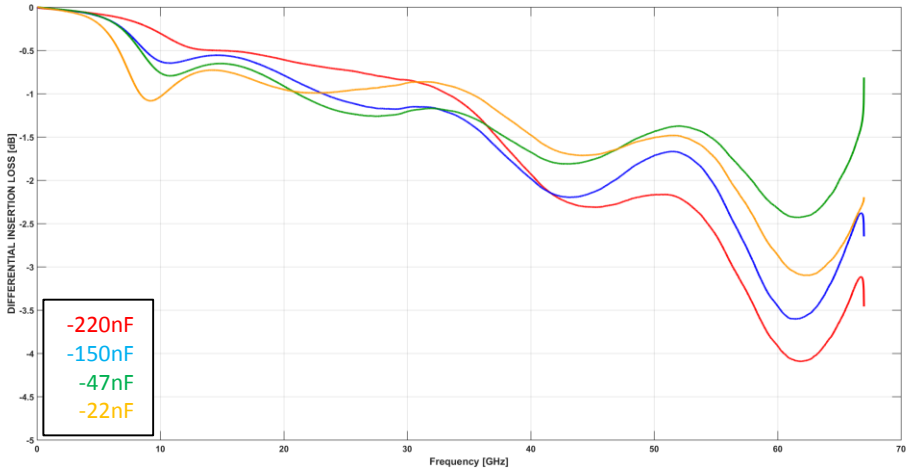
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

3

SIMULATION



MEASUREMENT

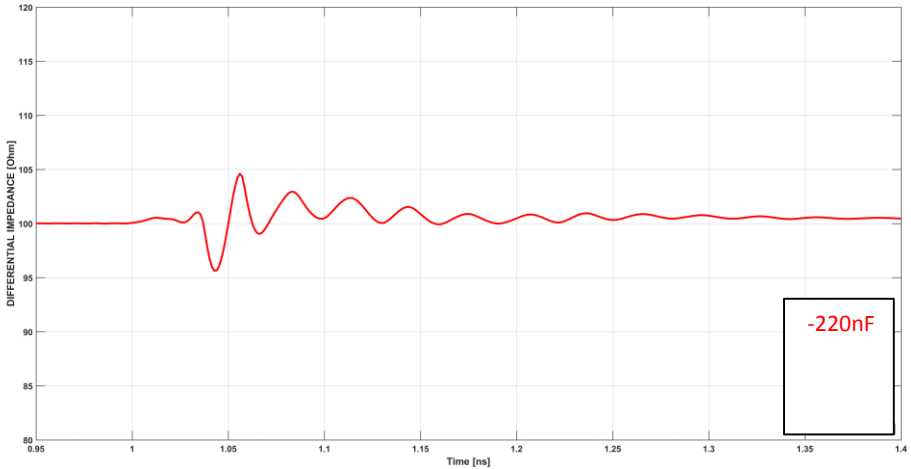


2. SIM vs MEAS – TDR, 12ps RT (VOID)

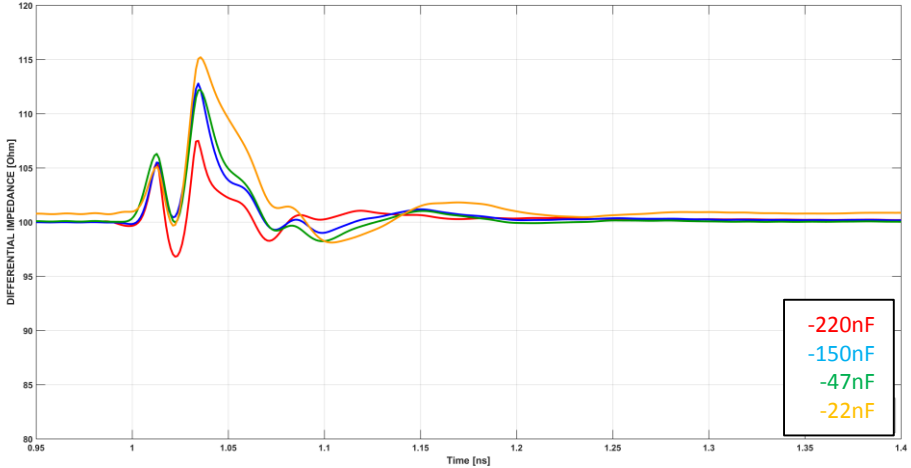
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

2

SIMULATION



MEASUREMENT

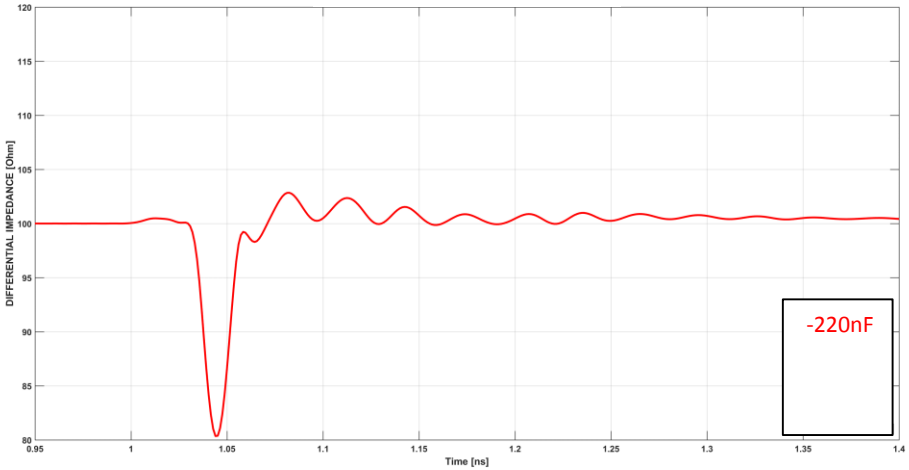


3. SIM vs MEAS – TDR, 12ps RT (SOLID)

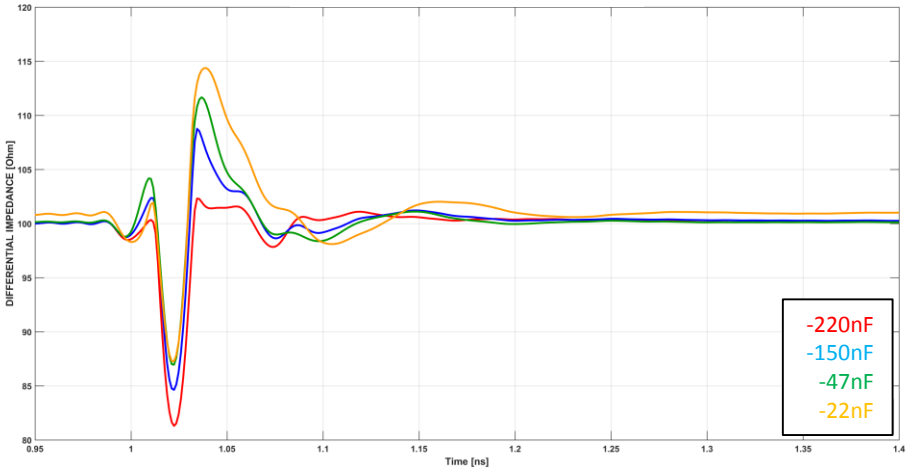
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

3

SIMULATION



MEASUREMENT



4. Chip to Module Exploration

Simulation to Measurement Comparison

220nF DC Blocking cap with Host Board package only:

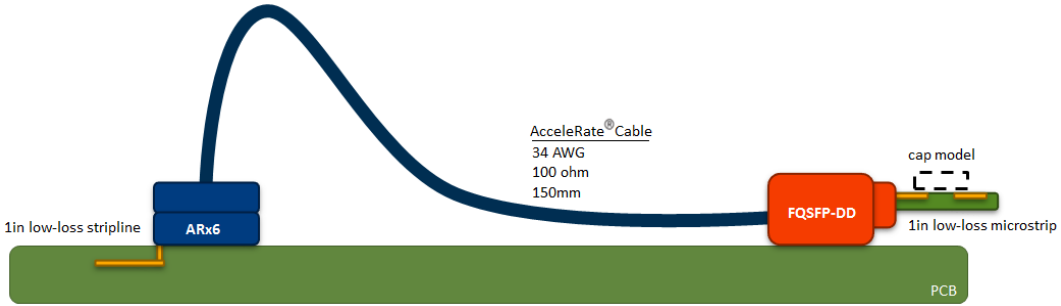
- 56G NRZ
- 112G PAM4
- 112G PAM4, 1 TAP DFE
- 112G PAM4, 3 TAP DFE
- 112G PAM4, 12 TAP DFE

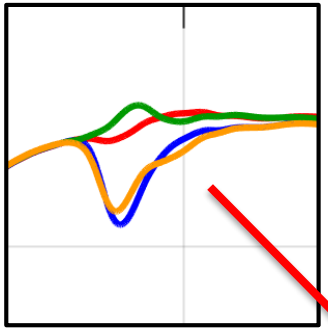
4

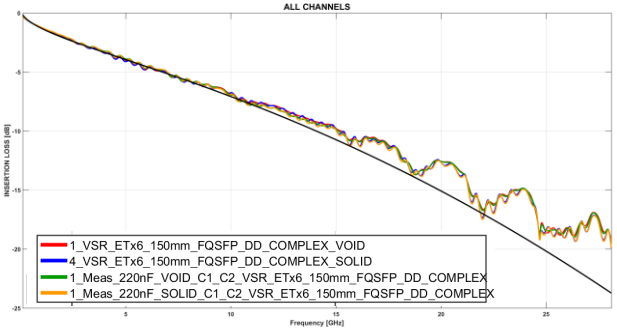
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

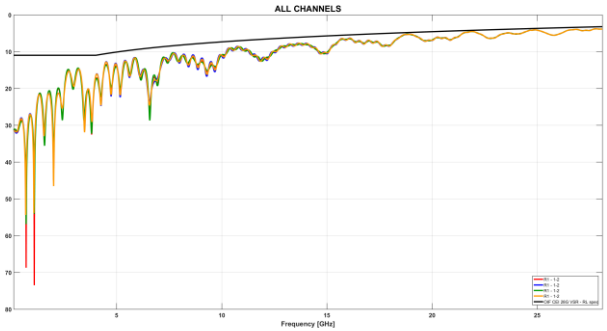
4. Host Package Only Study

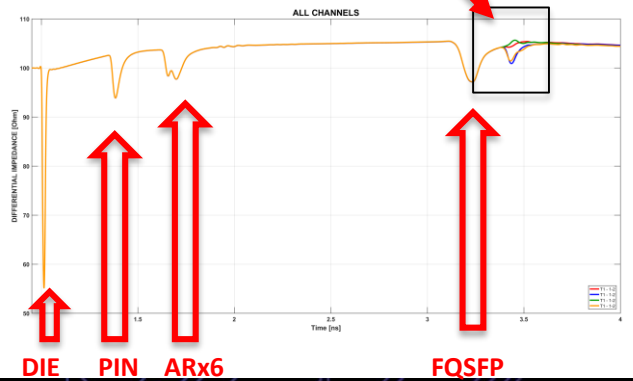
Includes TX Package & 220nF Cap





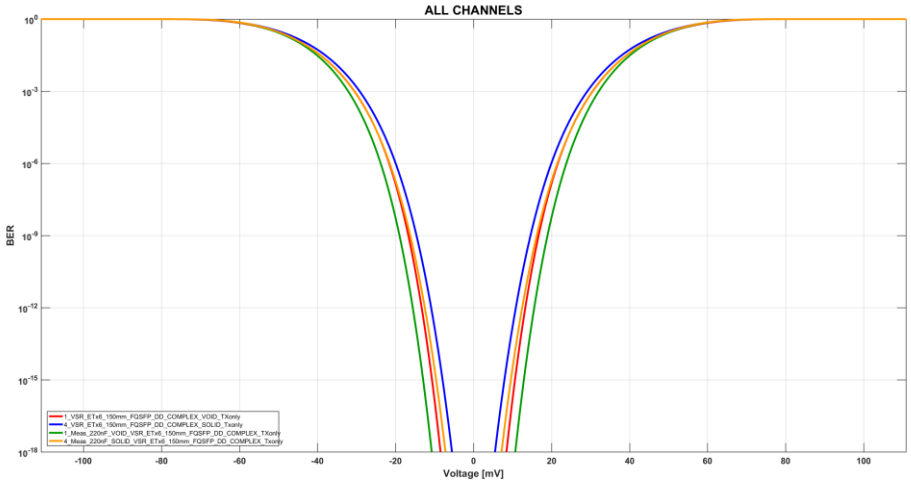






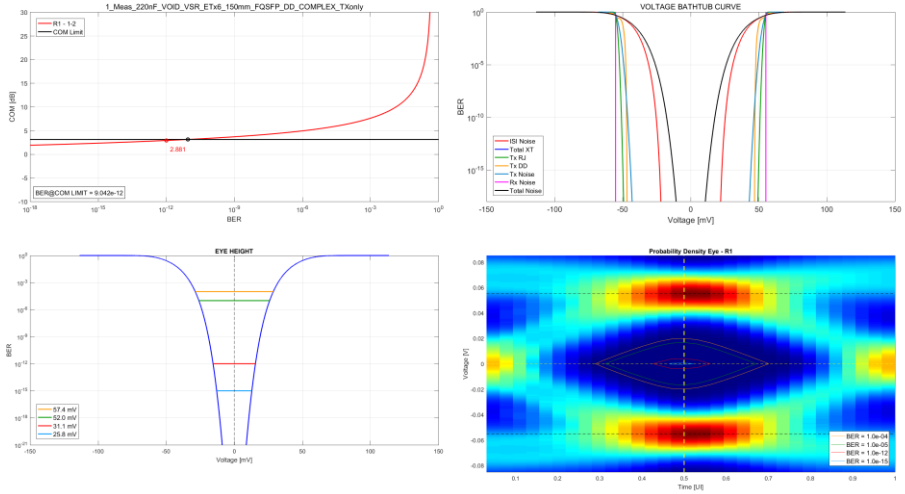
56G NRZ

Voltage Bathtub - All Cases



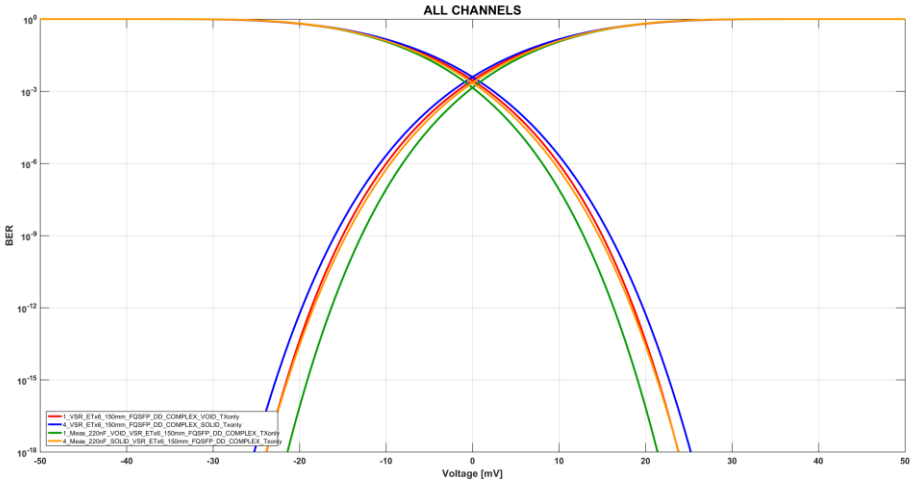
1_VSR_ETx6_150mm_FQSFP_DD_COMPLEX_VOID
4_VSR_ETx6_150mm_FQSFP_DD_COMPLEX_SOLID
1_Meas_220nF_VOID_C1_C2_VSR_ETx6_150mm_FQSFP_DD_COMPLEX
1_Meas_220nF_SOLID_C1_C2_VSR_ETx6_150mm_FQSFP_DD_COMPLEX

Measured VOID



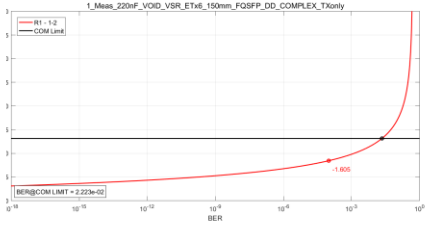
112G PAM4

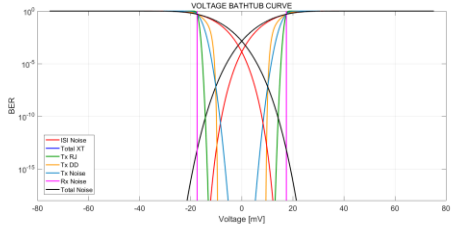
Voltage Bathtub - All Cases

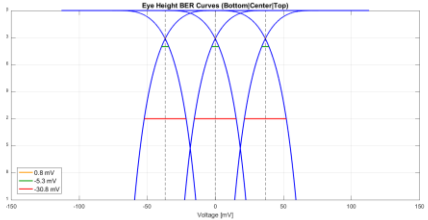


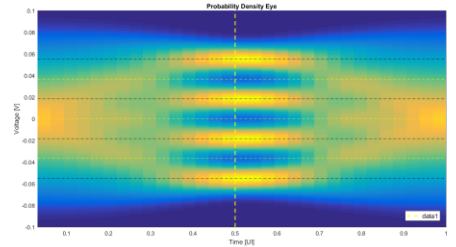
1_VSR_ETx6_150mm_FQSFP_DD_COMPLEX_VOID
4_VSR_ETx6_150mm_FQSFP_DD_COMPLEX_SOLID
1_Meas_220nF_VOID_C1_C2_VSR_ETx6_150mm_FQSFP_DD_COMPLEX
1_Meas_220nF_SOLID_C1_C2_VSR_ETx6_150mm_FQSFP_DD_COMPLEX

Measured VOID



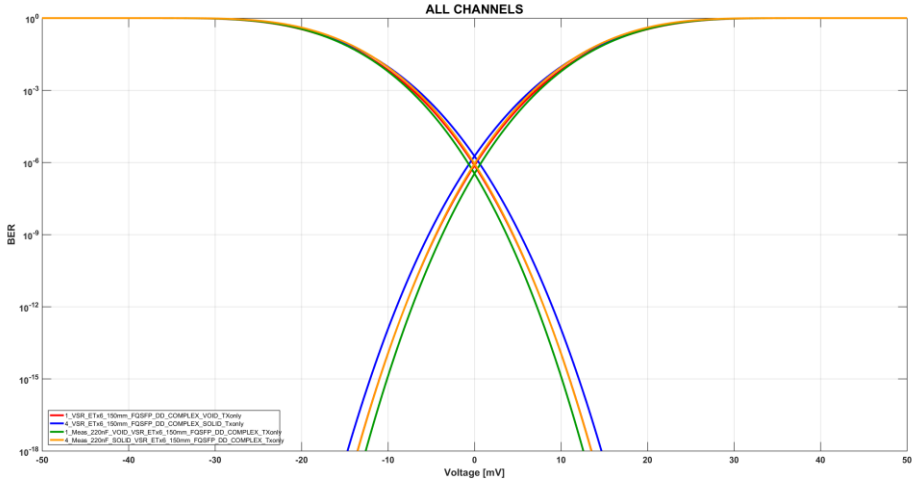






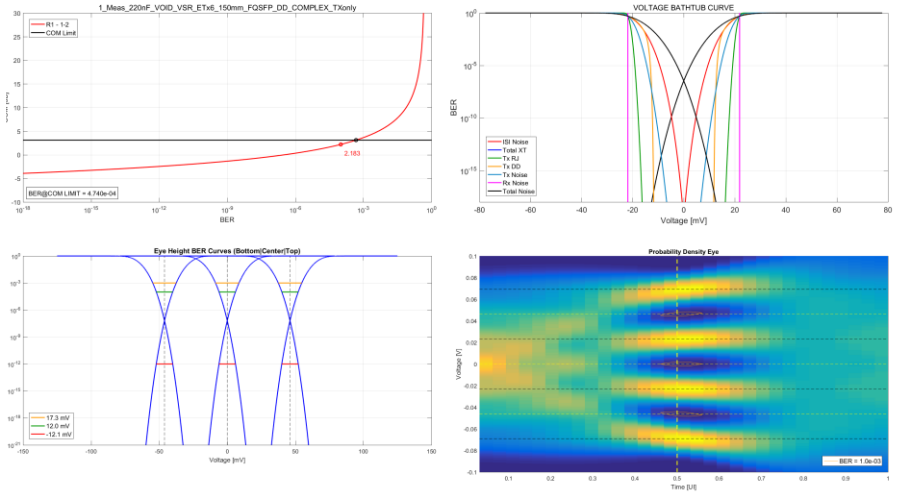
112G PAM4 3 TAP DFE

Voltage Bathtub - All Cases



1_VSR_ETx6_150mm_FQSFP_DD_COMPLEX_VOID
4_VSR_ETx6_150mm_FQSFP_DD_COMPLEX_SOLID
1_Meas_220nF_VOID_C1_C2_VSR_ETx6_150mm_FQSFP_DD_COMPLEX
1_Meas_220nF_SOLID_C1_C2_VSR_ETx6_150mm_FQSFP_DD_COMPLEX

Measured VOID



5. Chip to Module Exploration

Simulation to Measurement Comparison

220nF DC Blocking cap with optimistic TX/RX package:

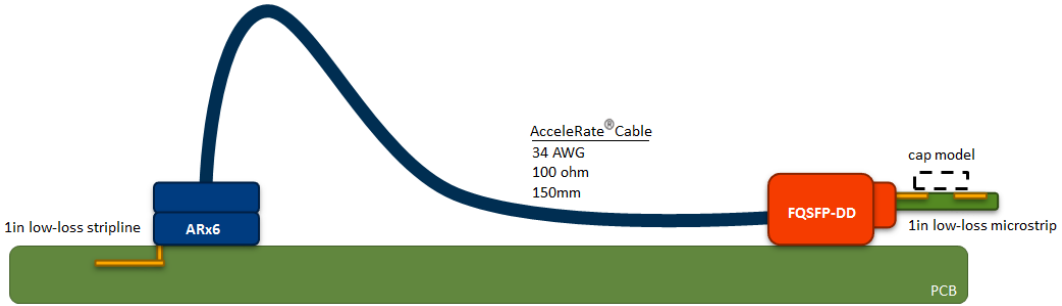
- 56G NRZ
- 112G PAM4
- 112G PAM4, 1 TAP DFE
- 112G PAM4, 3 TAP DFE
- 112G PAM4, 12 TAP DFE

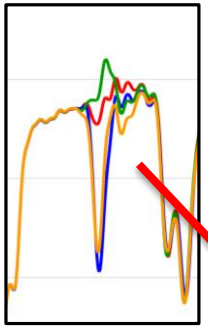
5

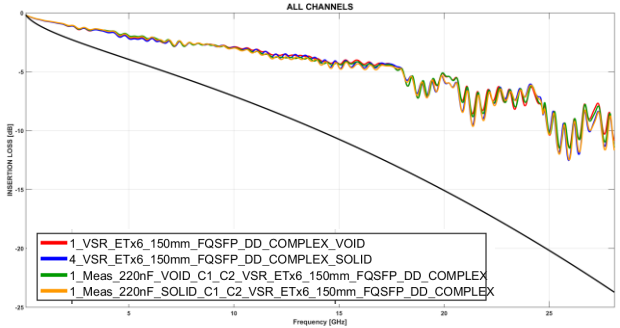
Simulated Measured Both	Capacitor Models			
Value	Complex VOID	Complex SOLID	Shorted VOID	Simple VOID
220nF	X	X	X	X
150nF	X	X		
47nF	X	X		
22nF	X	X		

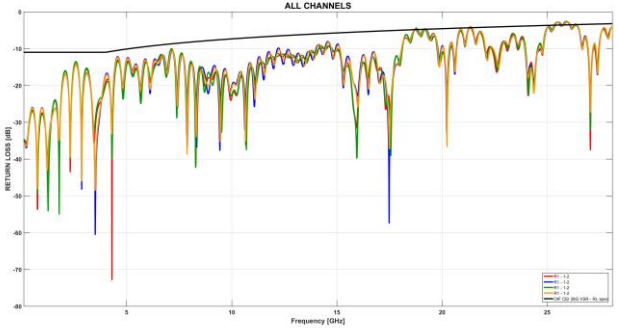
5. Optimistic Host/Module Package Study

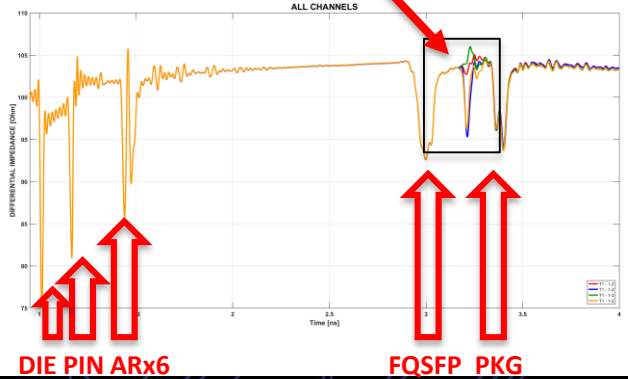
Includes TX/RX Package & 220nF Cap





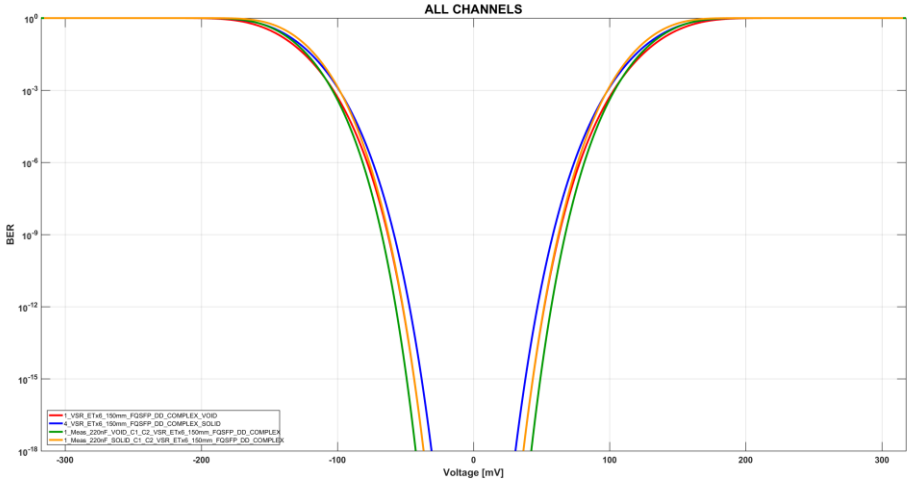




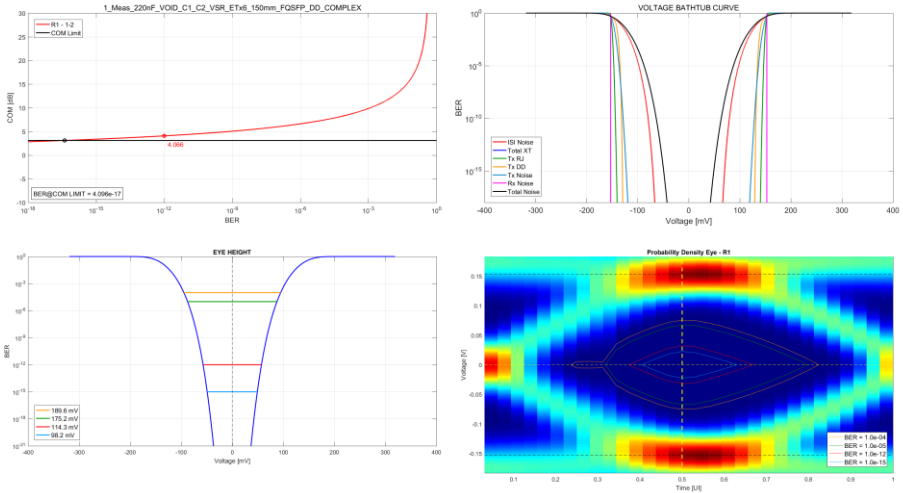


56G NRZ

Voltage Bathtub - All Cases

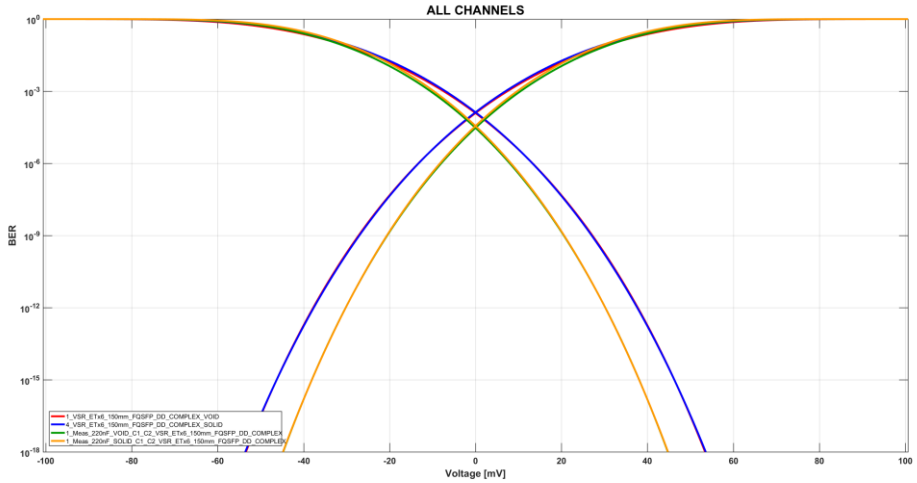


Measured VOID

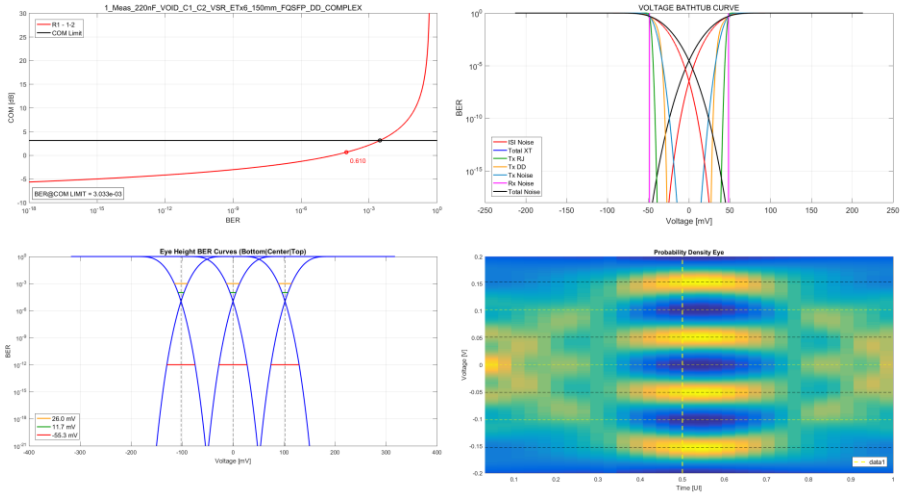


112G PAM4

Voltage Bathtub - All Cases

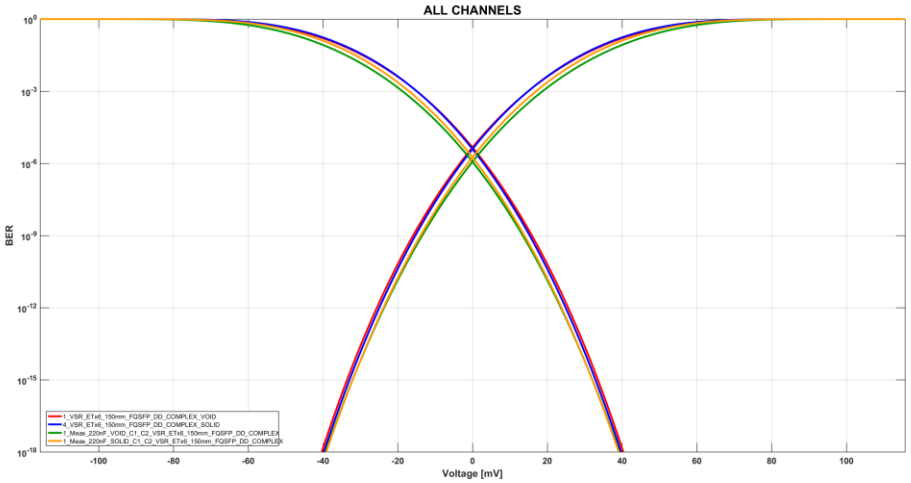


Measured VOID

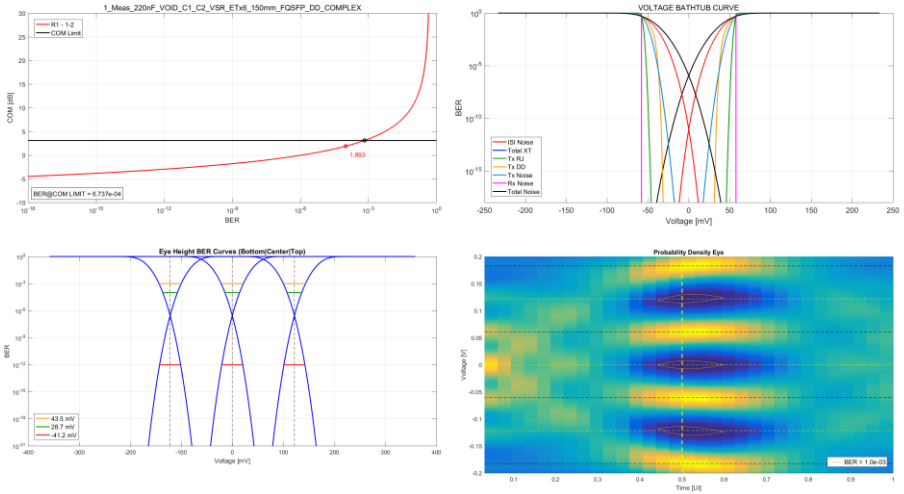


112G PAM4 3 TAP DFE

Voltage Bathtub - All Cases

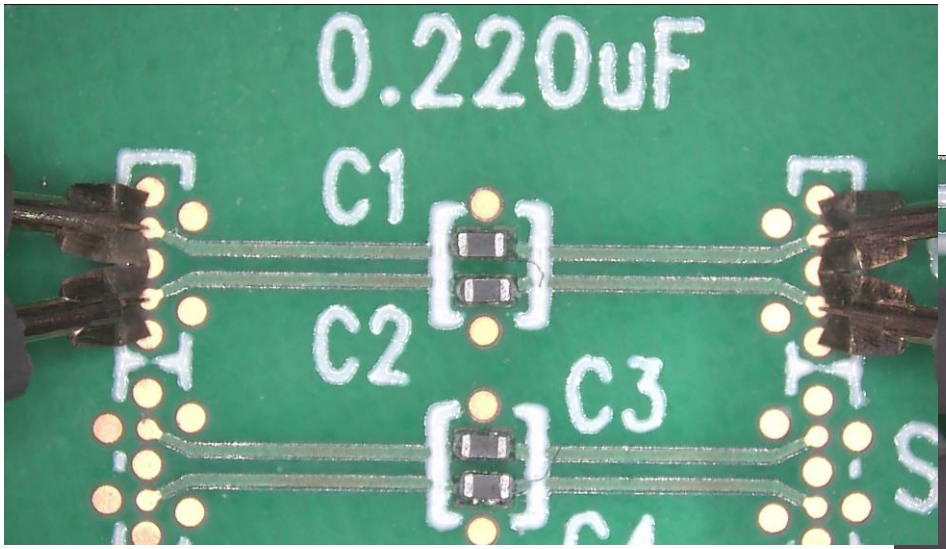


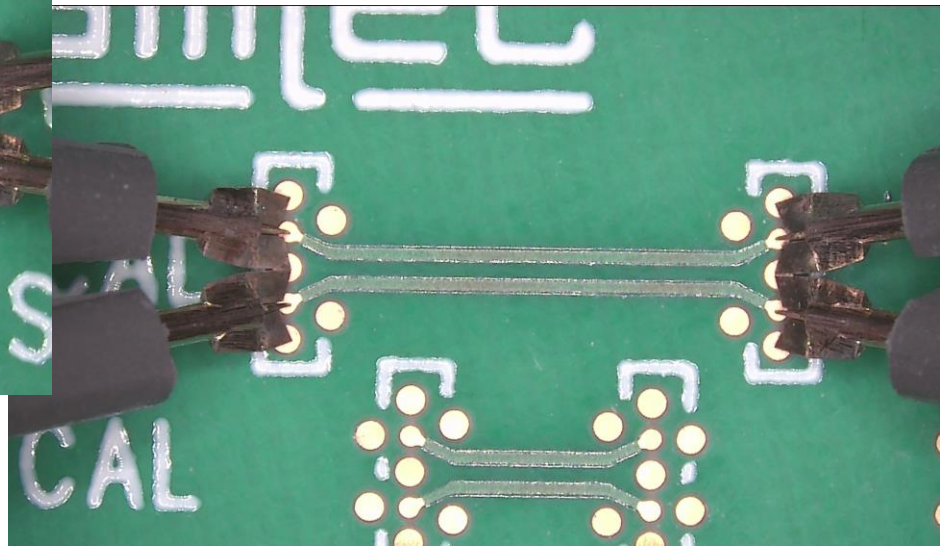
Measured VOID



Test Vehicle Correlation Work

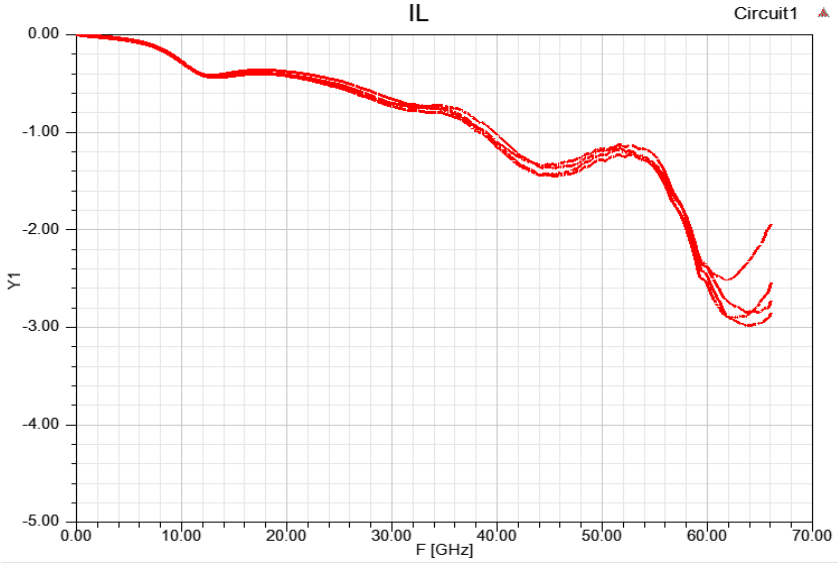
VOID, SOLID, & CAL Layouts

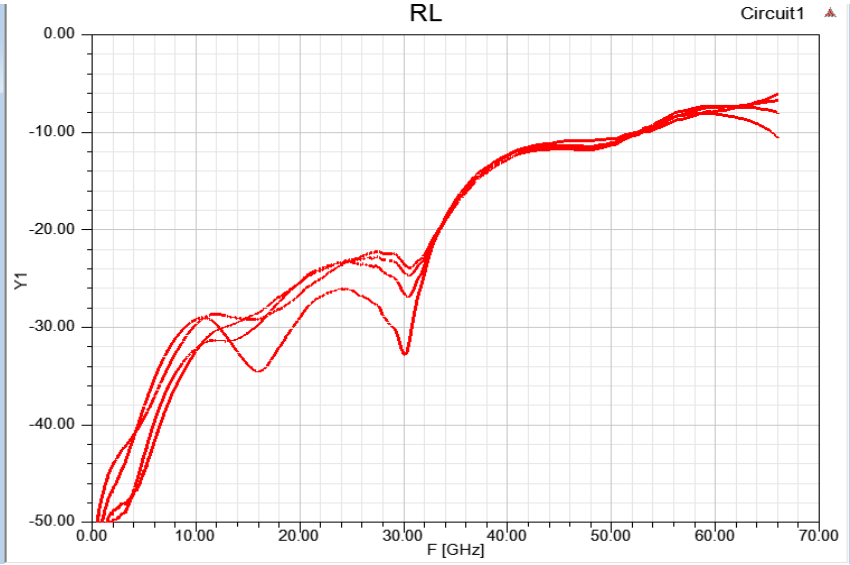




Test Vehicle Correlation Work

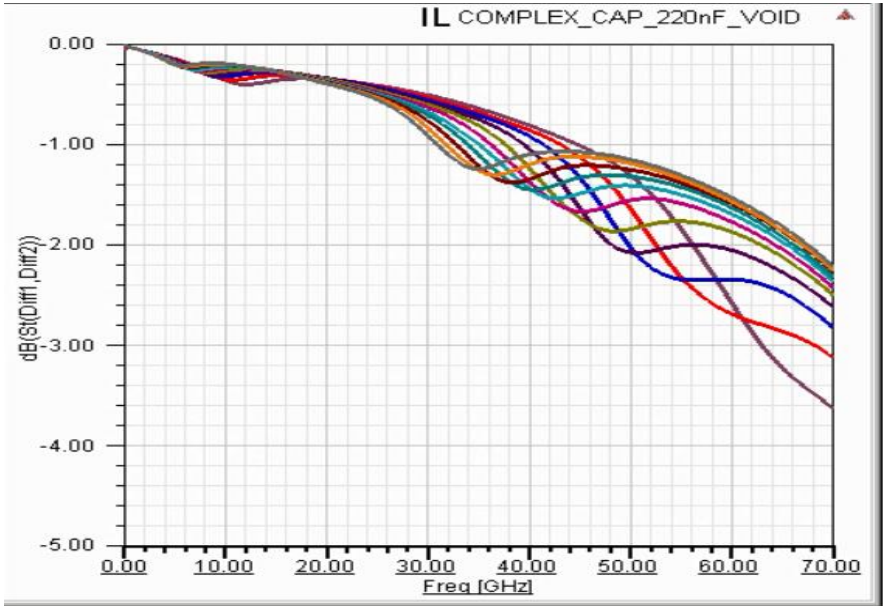
220nF VOID Measurements

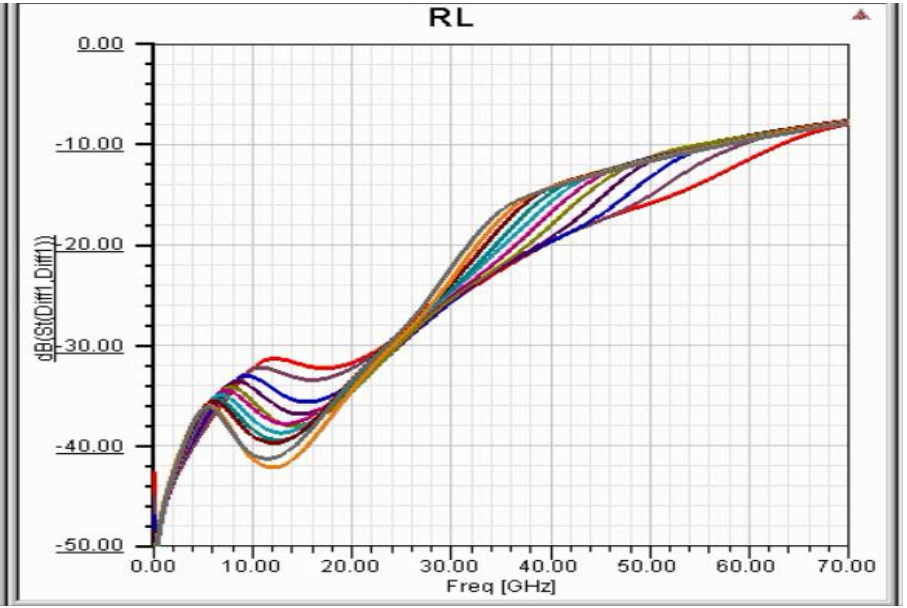




Test Vehicle Correlation Work

220nF VOID Simulation v2.0





Thank you!

QUESTIONS?