

Connecting ADS8410/13 With Long Cable

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ABSTRACT

Many applications require that the analog-to-digital converter (ADC) be located near the field sensor; however, the digital processing often occurs at a distance. Therefore, the input and output signals need to travel through a long cable from the field sensor to the site where digital processing occurs. This application report is a guide for using a 1-meter cable, the Samtec EQCD Series high data rate cable assembly, to transmit and receive the digital signals of the TI ADS8410/13 ADCs. The high-speed coaxial cable, the Samtec EQCD-020-40.00-TBL-SBR-1, is used as the ADS8410/13 offer a high-speed (200 Mbps) LVDS interface.

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1 Introduction

The Texas Instruments ADS8410/13 are 16-bit, 2-MSPS analog-to-digital converters (ADC) with a 4-V internal reference. These devices include a capacitor-based SAR ADC with inherent sample and hold. The ADS8410/13 also has a 200-Mbps, LVDS, serial interface. This interface is designed to support daisy-chaining or cascading of multiple devices. The ADS8410 has a unipolar, single-ended input, whereas the ADS8413 has a unipolar, differential input.

The Samtec EQCD-020-40.00-TBL-SBR-1 is a 38 AWG ribbon co-axial, high data rate cable assembly with a 0,8-mm pitch. It offers 50-Ω impedance and low skew between channels. The cable is flexible in nature.

2 Block Diagram

Figure 1 shows a simple block diagram of a system consisting of field sensor, ADC, the Samtec EQCD-020-40.00-TBL-SBR-1 cable assembly, and an FPGA for processing the digital outputs and sending them to a personal computer. The sensor and ADC are located on the Sensor Board. The LVDS receiver/ FPGA are located on the Receiver Board. The Samtec EQCD Series cable assembly connects these two boards. Note that no buffer is between the ADS8410/13 and the FPGA/ Receiver. The ADC directly drives the connectors, cable, and the receiver.

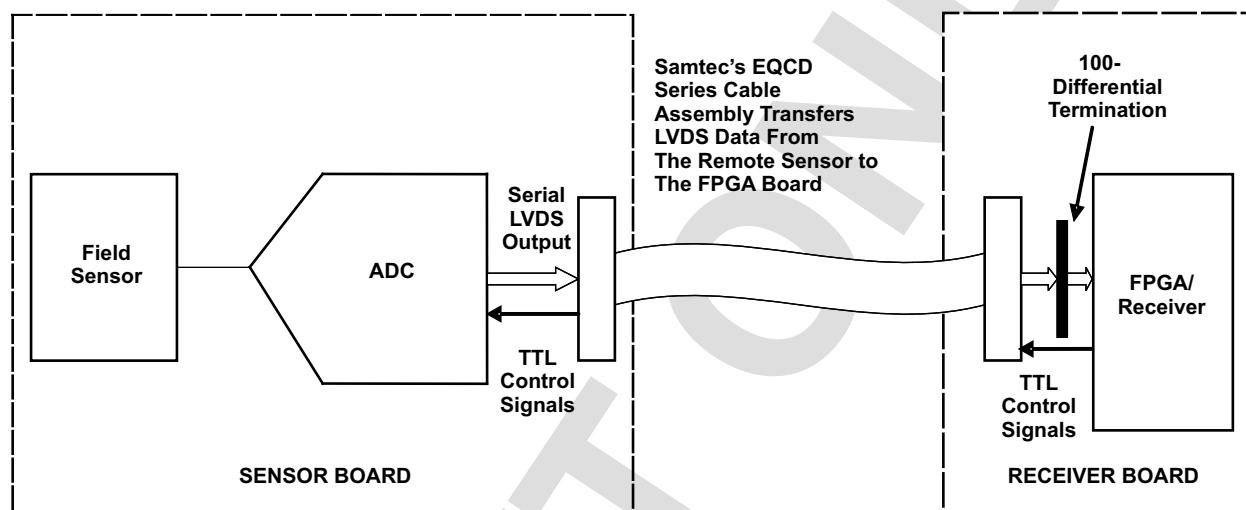


Figure 1. Block Diagram

3 High-Speed LVDS Interface

The high-speed (200 Mbps) LVDS interface offered by ADS8410/13 is useful for the following reasons.

1. LVDS, low voltage differential signaling, induces less switching noise compared to CMOS/TTL.
2. LVDS is immune to ground bounce because of its differential nature.
3. High speed supports more devices that are daisy-chained or cascaded.
4. LVDS is a differential current output which is converted to voltage by a 100-Ω termination at the receiver end.

4 Selection of Cable

The ADS8410/13 have a 200-MHz clock with a maximum rise and fall time of 950 ps. The cable should offer 100-Ω differential impedance matching because LVDS is terminated with a 100-Ω resistor at the receiver end. This ensures that no reflection occurs. The receiver at the far end latches SDO and SYNC_O signals at the falling edge of CLK_O. Therefore, the skew, introduced by the cable among these signals (SDO, SYNC_O and CLK_O), should be low (<100 ps), so that no setup and hold time violation occur.

The Samtec EQCD-020-40.00-TBL-SBR-1 cable assembly has a bandwidth of 500 MHz (period of 2 ns) for a 1-meter length. This supports a 1-ns rise and fall time, offering a good 50-Ω matching for individual signal lines. Every alternate third line is connected to ground to make a 100-Ω differential pair. This is

shown in [Figure 2 \(www.samtec.com/ftppub/prodspec/qse-qte.pdf\)](http://www.samtec.com/ftppub/prodspec/qse-qte.pdf). The EQCD Series cable assembly has a maximum skew of 50 ps which is within a tolerable limit. From the Samtec EQCD Series Characterization Summary Report (available at www.samtec.com/ftppub/testrpt/eqcd120903aweb.pdf), because of the resistance of 1-meter cable, the voltage drop is only 17 mV compared to a 680-mV differential swing.

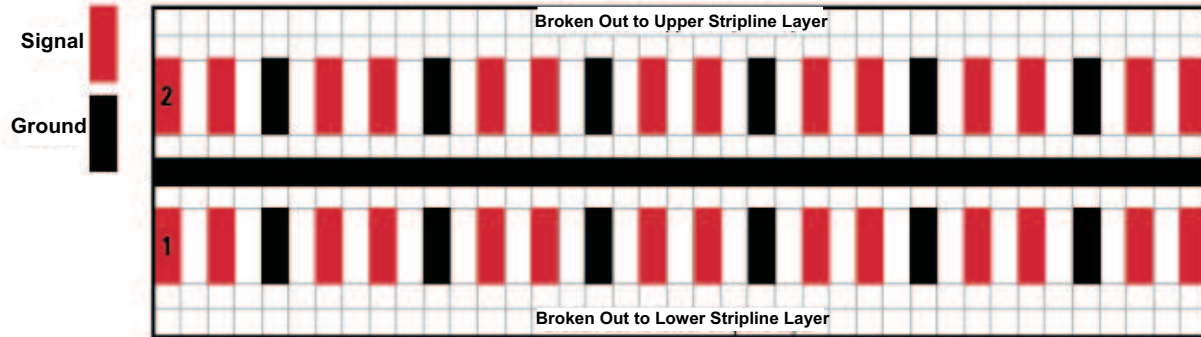


Figure 2. Connection to Make 100-Ω Differential Impedance Matching

The Samtec EQCD-020-40.00-TBL-SBR-1 cable assembly mates with the Samtec Q-Strip™ QTE-020-09-F-D-A connector (see [Figure 3](#)) on one end and the Samtec QSE-020-01-F-D-A connector (see [Figure 3](#)) on the other end. These high-speed connectors have 40 signal input/outputs and have an apparent impedance (based on the maximum rise/fall time of the ADS8410/13 clock) of 50 Ω to ground and low insertion loss. When used with differential signaling, the connectors have an apparent differential impedance of 100 Ω between two lines providing every third line is connected to ground (as shown in [Figure 2](#)). These Samtec connectors are surface mount.

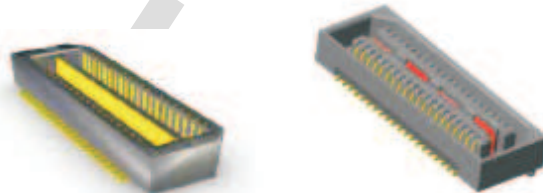


Figure 3. Samtec Q-Strip QSE Series and QTE Series High-Speed Connectors

5 Orientation of Samtec EQCD Series Cable Assembly

In the Samtec EQCD Series high data rate cable assembly, a length of coaxial ribbon cable is terminated to a transition PCB break-out region onto which the respective connectors are soldered. Three different connector styles/orientations are available for the 0,8-mm pitch Samtec Q-Strip QSE Series and QTE Series connectors (see [Figure 4](#)):

1. DV to DV (dual vertical)
2. EM to EM (edge mount)
3. DV to EM

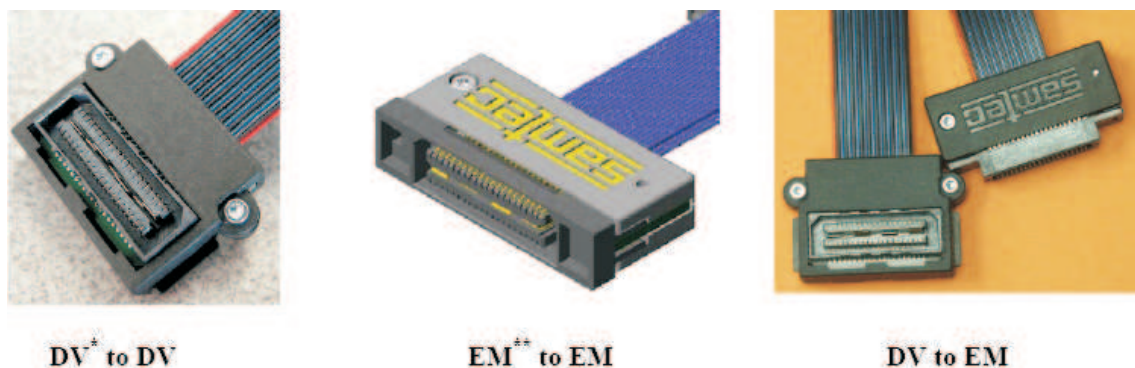


Figure 4. Different Types of Samtec EQCD Series Cable Assemblies

Two PCB variations for each of the three connector styles are:

1. Non-crossover PCB break-out — Outer rows of the connectors on both ends are connected via the transition PCB.
2. Crossover PCB break-out (designed with an X) — Outer row on end of the connector assembly is connected to the inner row on the opposite end connector via the transition PCB.

For this application report, the part number of the Samtec EQCD Series cable assembly evaluated is EQCD-020-40.00-TBL-SBR-1. This is a DV-to-DV connector orientation, with a non-crossover PCB break-out type. However, similar performance should be achieved from any of the other connector orientations and PCB break-out types offered within the Samtec EQCD Series Cable Assemblies.

6 Evaluation Setup

To evaluate the ADS8410/13 with the Samtec EQCD-020-40.00-TBL-SBR-1 cable assembly, the application EVM (ADS8413EVM or ADS8410EVM) was selected so that the ADC would be near the sensor. The application board has a Samtec Q-Strip QTE-020-09-F-D-A connector which connects to the EQCD Series cable assembly. A receiver board with SN65LVDS152 (LVDS to CMOS de-serializer) which connects to FPGA/ DSP was selected as the receiver at the far end. This board has a Samtec Q-Strip QSE-020-01-F-D-A connector which connects to the other end of the EQCD Series cable assembly. The CMOS/TTL, LVDS inputs are generated from the FPGA and travels through the EQCD Series cable assembly to the ADC. The output LVDS, CMOS/TTL signals from the ADC travel through the EQCD Series cable assembly to the de-serializer and the FPGA. [Figure 5](#), [Figure 6](#), and [Figure 7](#) show the detailed block diagrams of the evaluation setup. [Figure 5](#) shows the inputs to the ADC from the sensor. OPA drivers are used as input drivers. [Figure 6](#) shows the digital inputs and outputs, of the ADC, connection to the Samtec Q-Strip QTE Series connector. The same connection applies to the signals to the Samtec Q-Strip QSE Series connector in the receiver board. [Figure 7](#) shows how the LVDS serial outputs are de-serialized by two SN65LVDS152.

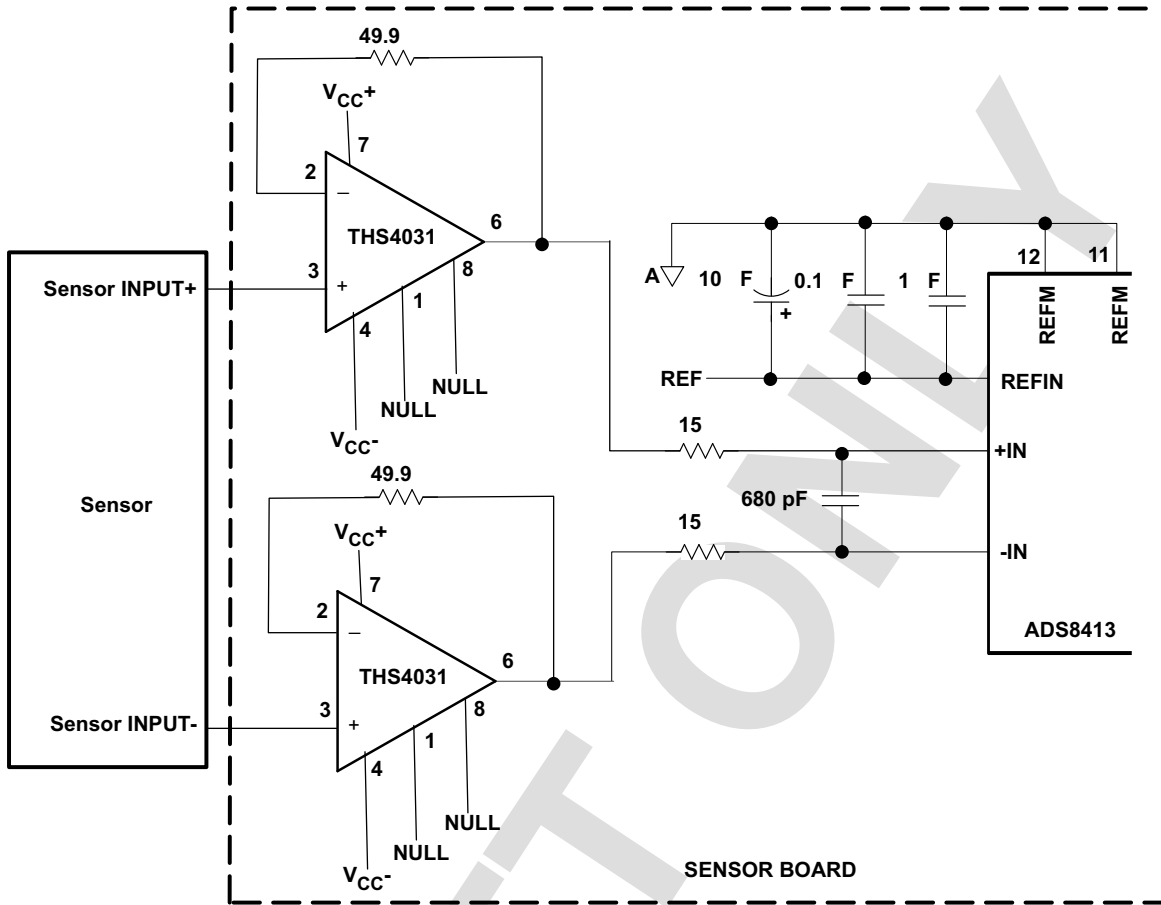


Figure 5. Sensor and the ADC (Analog Side)

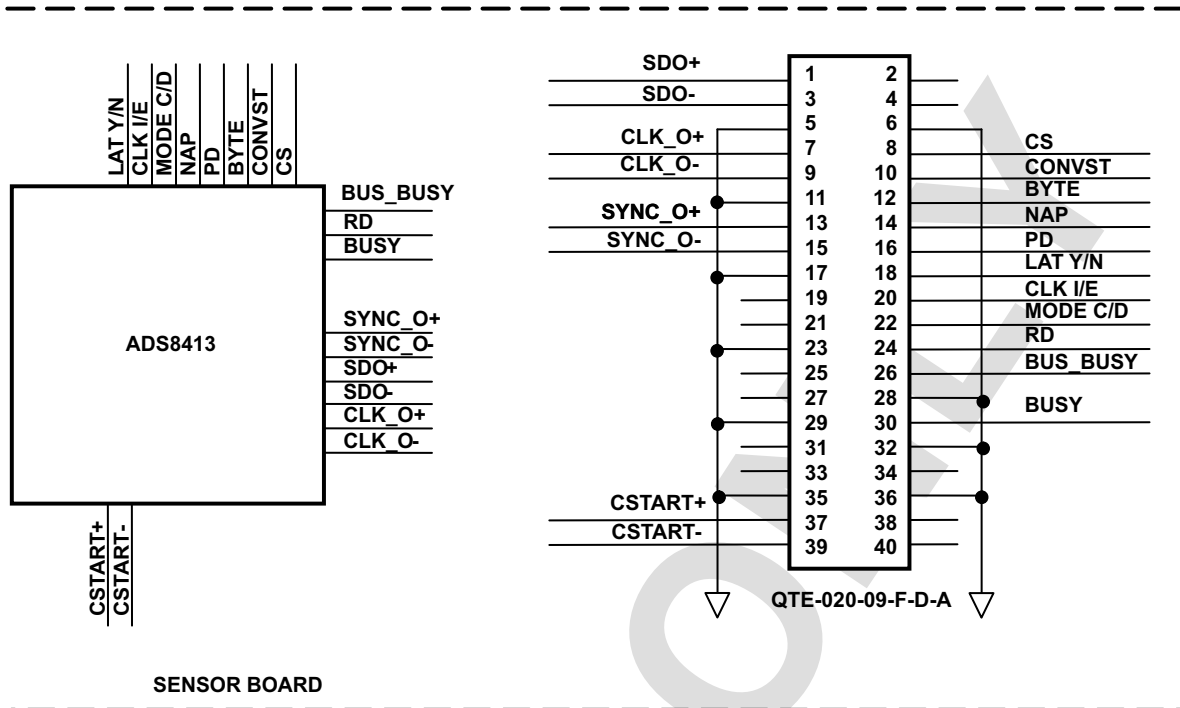


Figure 6. ADC Digital Input and Output Connection to PCB-Mounted Samtec Q-Strip QTE Series Connector

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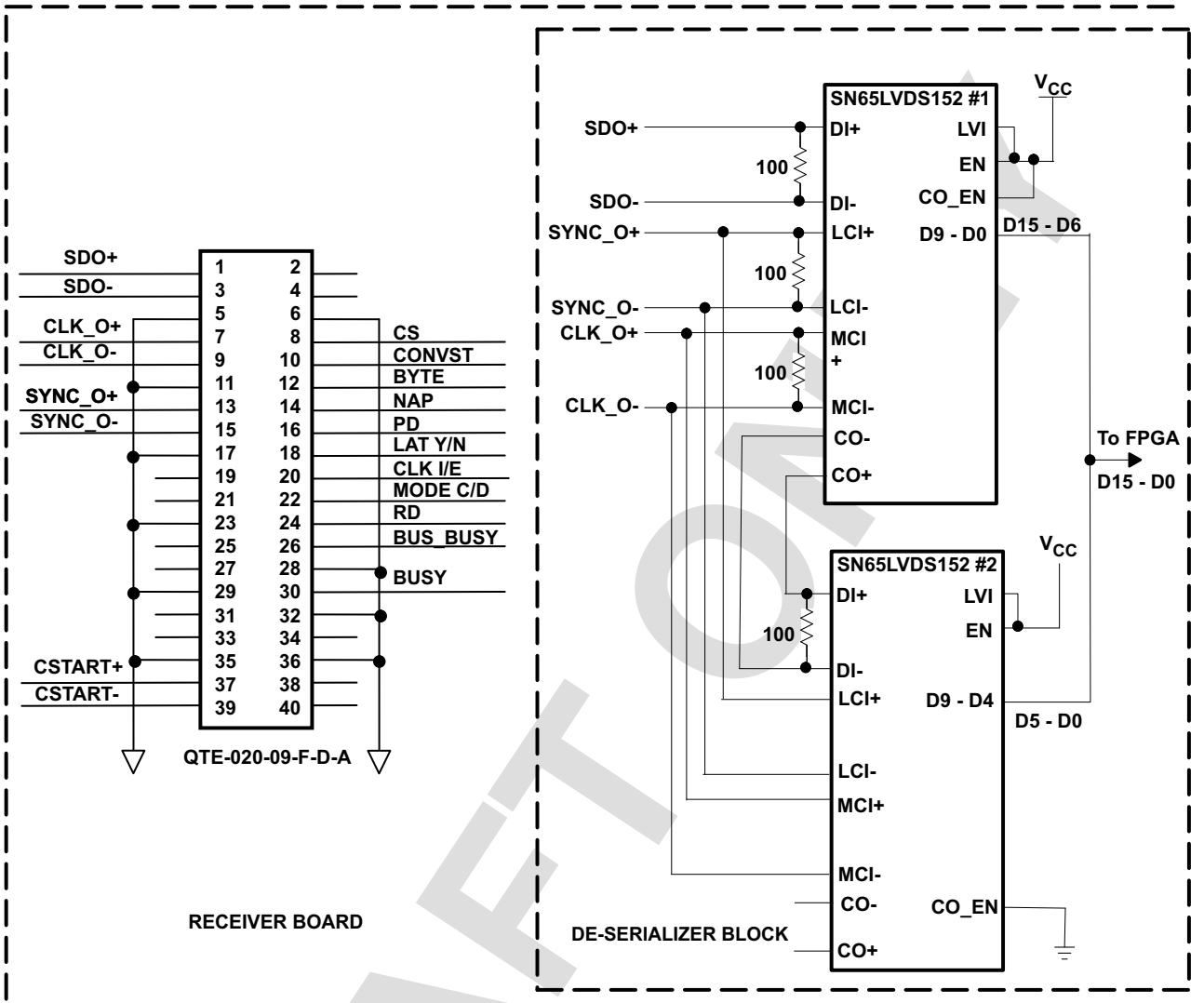


Figure 7. LVDS to 16-Bit Parallel De-Serialization

7 Result

Figure 8 and Figure 9 show the 200-MHz LVDS clock with and without the cable. When the cable was not used, the sensor board and the receiver board were directly connected together with QTE and QSE connectors. A small amount of reflection occurs due to the impedance mismatch resulting from resistor tolerance. The reflection takes more time to come back when the cable is used, which makes the clock waveforms look different.

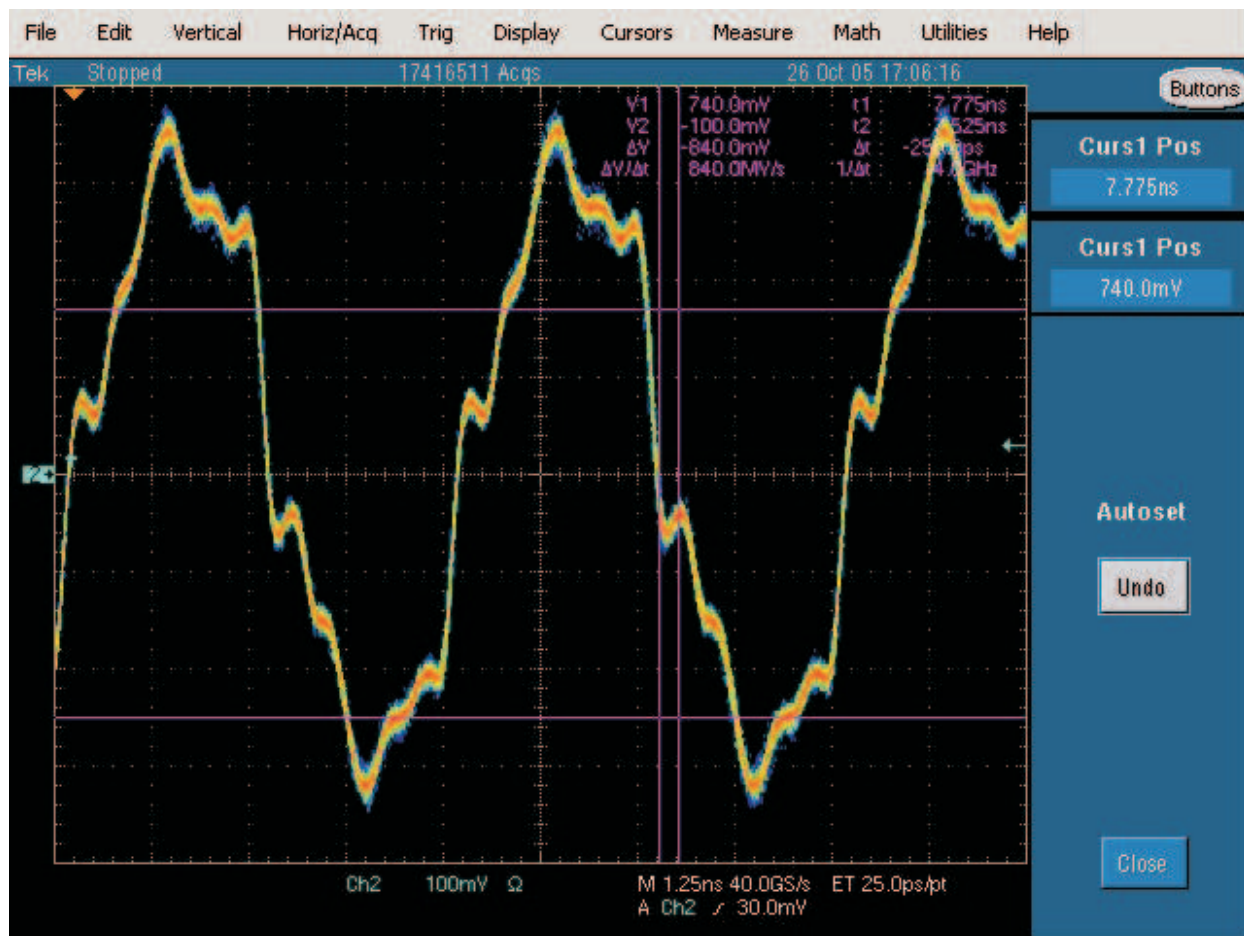


Figure 8. CLK_O at the Receiver End Without Using Cable

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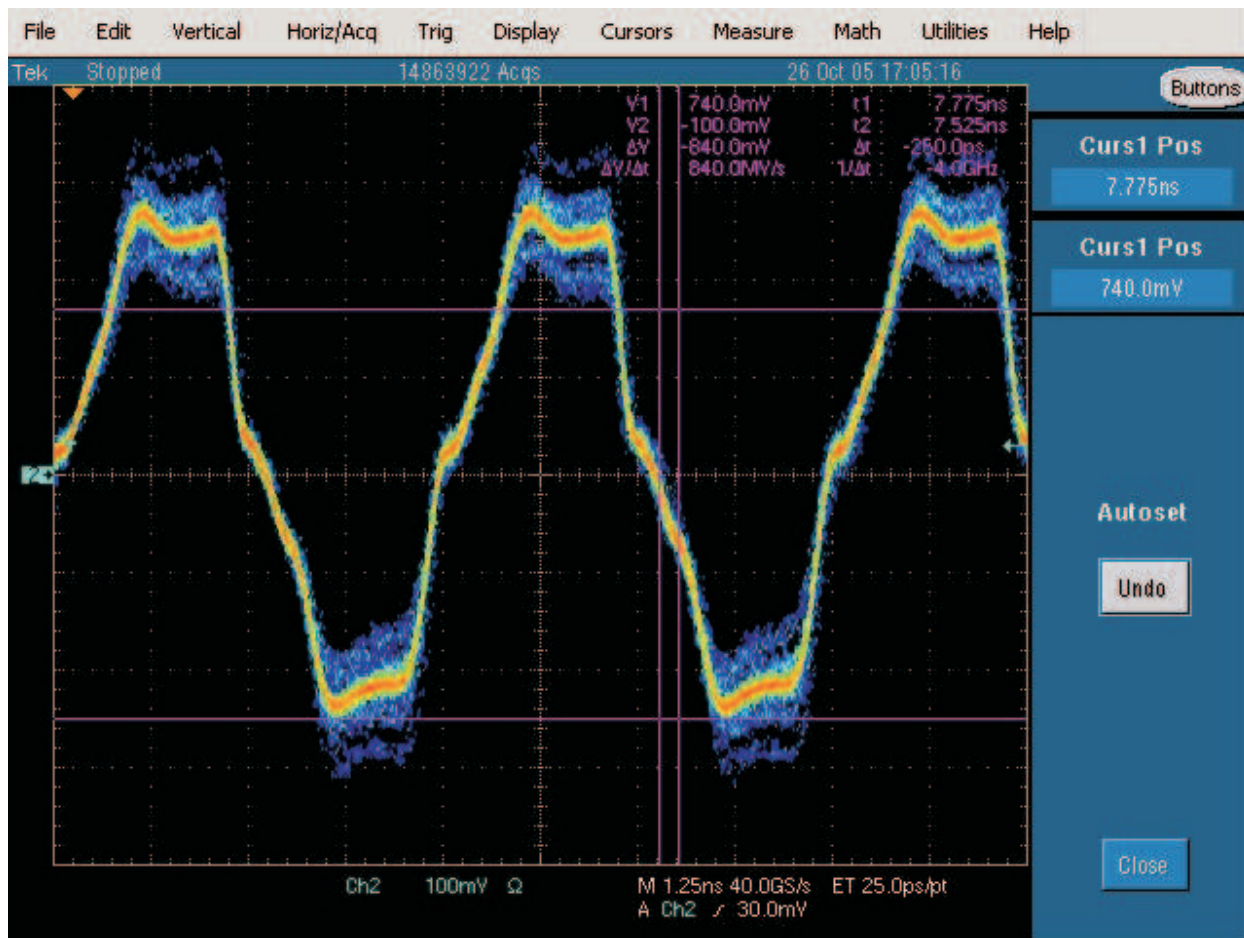


Figure 9. CLK_O at the Receiver End Using Cable

Table 1 shows AC parameters of the ADS8413 in this evaluation versus the typical specification in the data sheet. The small difference seen in the parameters of this table is primarily because of repeatability of measurement and device to device variation.

Table 1. AC Parameters of ADS8413

PARAMETER	CONDITION	EVALUATION SYSTEM WITH CABLE	EVALUATION SYSTEM WITHOUT CABLE ⁽¹⁾	DATA SHEET SPECIFICATION (TYPICAL)
SNR	20 kHz	91.67	91.98	91.5
	100 kHz	90.65	90.62	90.3
THD	20 kHz	-102.23	-102.25	-107.0
	100 kHz	-100.21	-100.12	-95.0
SFDR	20 kHz	-102.99	-102.99	-112.0
	100 kHz	-101.78	-102.77	-98.0
SINAD	20 kHz	91.31	91.59	91.4
	100 kHz	90.20	90.16	86.3
ENOB	20 kHz	14.87	14.92	14.89
	100 kHz	14.70	14.68	14.04

⁽¹⁾ The sensor board and the receiver board were directly connected by QTE and QSE connectors in this case.

8 Conclusion

The high-speed LVDS outputs of ADS8410 and ADS8413 do not require any buffer to drive the Samtec EQCD-020-40.00-TBL-SBR-1 high data rate cable assembly and the LVDS receiver. The high-speed (200 Mbps) LVDS signals travel through the Samtec EQCD-020-40.00-TBL-SBR-1 high data rate cable assembly without any noticeable reflection or cross-talk. Performance of the ADC is unchanged with a 1-meter cable transmitting and receiving the LVDS and CMOS/TTL digital signals.

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