

FIG 1
PCIE-LP

TABLE 1				
	"A" FULLY MATED	"A" MAX ALLOWABLE	CONTACT WIPE	
			MAX	MIN
PCIE-LP	1.15 [0.045]	3.50 [0.138]	2.73 [0.107]	0.38 [0.015]

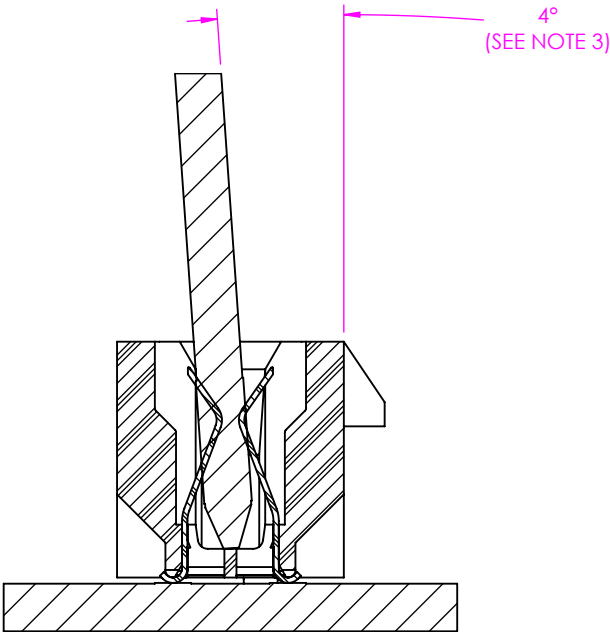


FIG 2
PCIE-LP

- NOTES:
- 1. ALL DIMENSIONS BASED ON NOMINAL VALUES FOR SAMTEC RECOMMENDED PCB LAYOUTS.
 - 2. ALTHOUGH MAXIMUM DIMENSIONS OF ALLOWABLE SEPARATION FROM FULLY MATING THE COMPONENTS ARE LISTED, SAMTEC RECOMMENDS FULL MATING.
 - 3. MAXIMUM ALLOWABLE ANGLE AT FULLY MATED NOMINAL CONDITIONS. F:\dwg\sw\exisprod\mated docs\PCIE-LP Mated Document.SLDDRW

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