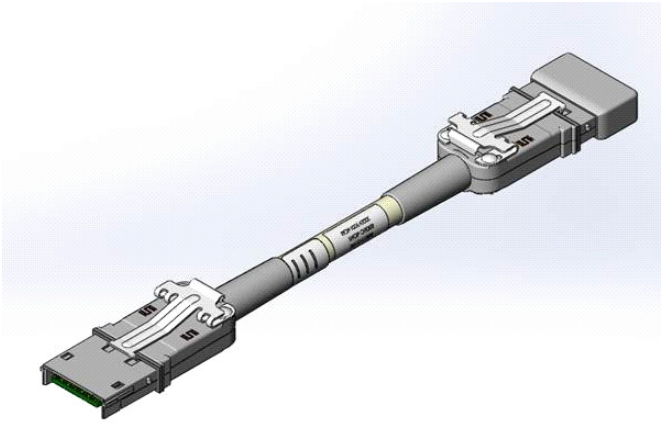
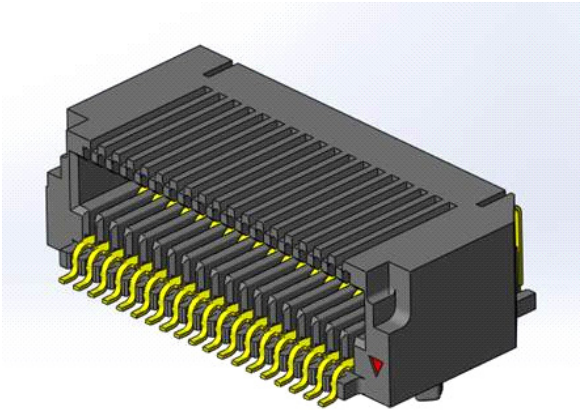
High Speed Characterization Report

EPLSP-XXX-3000



Mated with:

ERI8-XXX-X-D-RA



Description:

0.80 mm Eye Speed® 32 AWG Twinax
Rugged Latching High-Speed I/O Cable Assembly

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Report Revision: 5/7/2014

Series: EPLSP
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Cable Assembly Overview

EPLSP Cable Assembly is constructed using Samtec 32 AWG, low skew pair twinax cable. The cable is terminated at each end to a printed circuit transition board and an EPLSP plug connector with 0.80 mm (.0315") pitch. The transition boards are wired to facilitate a Pin 1 to Pin 1 mapping between the cable terminations.

EPLSP series cable assemblies support SAS, SATA, Fibre Channel, Ethernet, PCIe and Infiniband protocols. The EPLSP series cable assemblies are available in 19 positions (9 diff pairs) and 31 positions (17 diff pairs). The cable assembly length can be selected from 200 to 9999 mm. The data in this report is only applicable to 3000 mm length cable assembly.

The EPLSP cable assembly was tested by mating it to an ERI8-019-S-D-RA double row 0.80 mm Eye Speed® High Speed Right Angle Edge Rate™ Receptacle at each end. One 3 meter sample was tested. The actual part number that was tested is shown in Table 1, which also identifies End 1 and End 2. A relative sample picture is shown in Figure1. Two differential pairs, a Long Path and a Short Path were tested. The short path is identified as Pair 1 and the long path is identified as Pair 6.

Length	Part Number	End 1	End 2
3000 mm	EPLSP-019-3000	EPLSP	EPLSP

Table 1: Sample Description

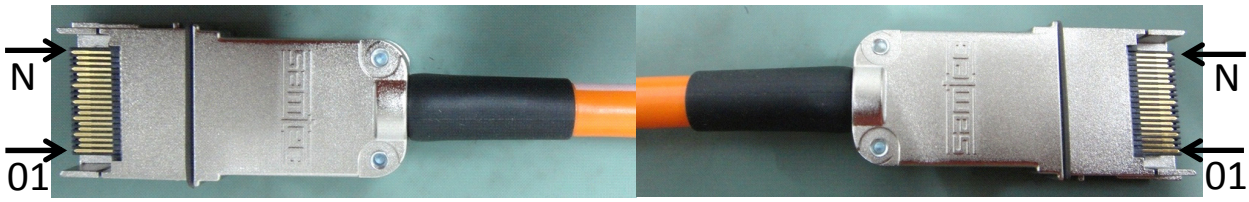

Figure 1: Test Sample

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Cable Assembly Bandwidth

The cable assembly bandwidth is based on the -7 dB insertion loss point of the mated cable assembly. The -7 dB point can be used to estimate usable system bandwidth in a typical two-level signaling environment. Modern high-speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The –7 dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

To calculate the bandwidth, the measured -7 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for any loss from the test board traces. The following table summarizes the Cable Assembly Speed Ratings for the EPLSP cable assemblies tested.

Assembly		-7 dB Frequency
EPLSP-019-3000	Pair 1 – Short Low	2.5 GHz
	Pair 6 – Long Low	2.0 GHz

Table 2: Cable Assembly Speed Rating

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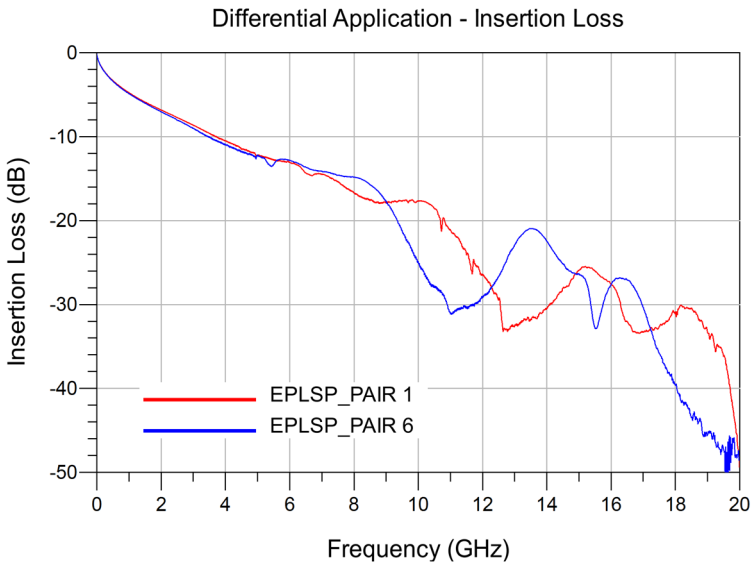
Frequency Domain Data Summary

Test Parameter	Configuration	Driver	Receiver	
Insertion Loss	Short Row	EPLSP_PAIR 1_END 1	EPLSP_PAIR 1_END 2	7dB@ 2.1 GHz
	Long Row	EPLSP_PAIR 6_END 1	EPLSP_PAIR 6_END 2	7dB@ 2.0 GHz
Return Loss	Short Row	EPLSP_PAIR 1_END 1	EPLSP_PAIR 1_END 2	>10dB to 4.4 GHz
	Long Row	EPLSP_PAIR 6_END 1	EPLSP_PAIR 6_END 2	>10dB to 3.4 GHz
Near-End Crosstalk	Across Row	EPLSP_PAIR 6_END 1	EPLSP_PAIR 1_END 1	<-20dB to 20 GHz
	In Row: Long Row	EPLSP_PAIR 6_END 1	EPLSP_PAIR 7_END 1	<-20dB to 17.6 GHz
Far-End Crosstalk	Across Row	EPLSP_PAIR 6_END 1	EPLSP_PAIR 1_END 2	<-20dB to 20 GHz
	In Row: Long Row	EPLSP_PAIR 6_END 1	EPLSP_PAIR 7_END 2	<-20dB to 20 GHz

Bandwidth Chart – Differential Insertion Loss



Series: EPLSP
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Time Domain Data Summary

Differential Application _ Impedance

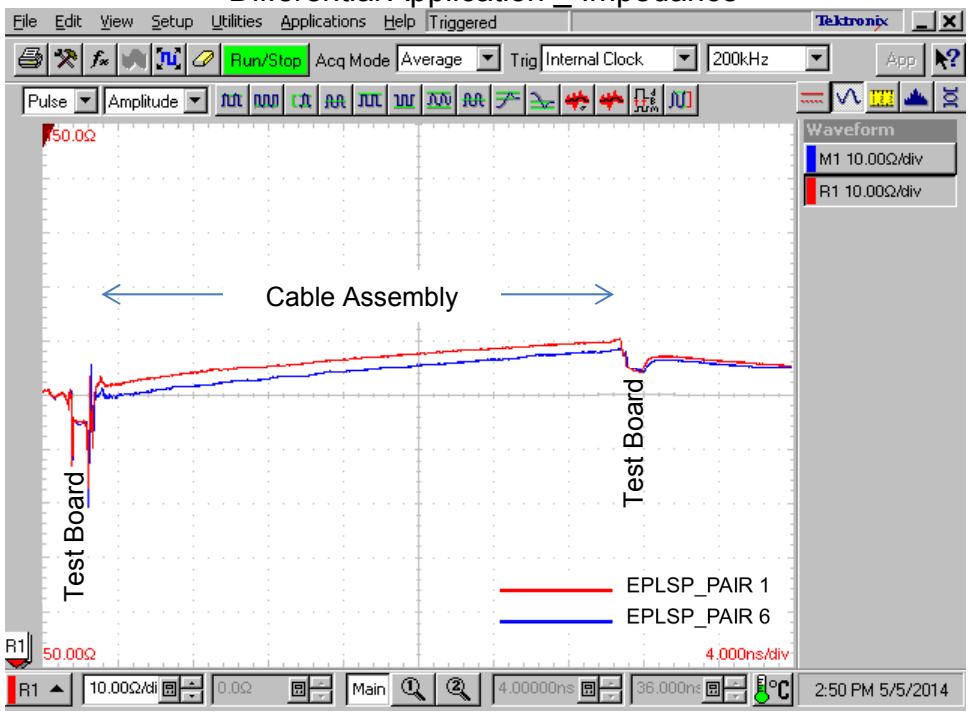

Table 4 - Propagation Delay (Cable Assembly)		
Cable Assembly	**Path**	**Propagation Delay (ns)**
EPLSP-019-3000	Pair 1 - Short Row	14.41
	Pair 6 - Long Row	14.45

Series: EPLSP
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Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GSSG" differential drive configuration only.

Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this cable assembly, the following array configurations are evaluated:

Differential Impedance**:**

- Long Row (upper terminals, furthest from test fixture)
- Short Row (bottom terminals, closest to test fixture)

Differential Crosstalk**:**

- In Row: Long Row (adjacent terminals in the long row)
- Across Row: “Xrow”: (from one row of terminals to the other row)

See Appendix D – Product and Test System Descriptions for details

Only one differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

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Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, signal propagation time and crosstalk in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix E of this report.

The measured S-Parameters from the network analyzer are post-processed using Agilent Advanced Design System to obtain the time domain response for signal propagation time and crosstalk. The Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 18 mils of PCB trace on each connector side. Delay is measured at 30 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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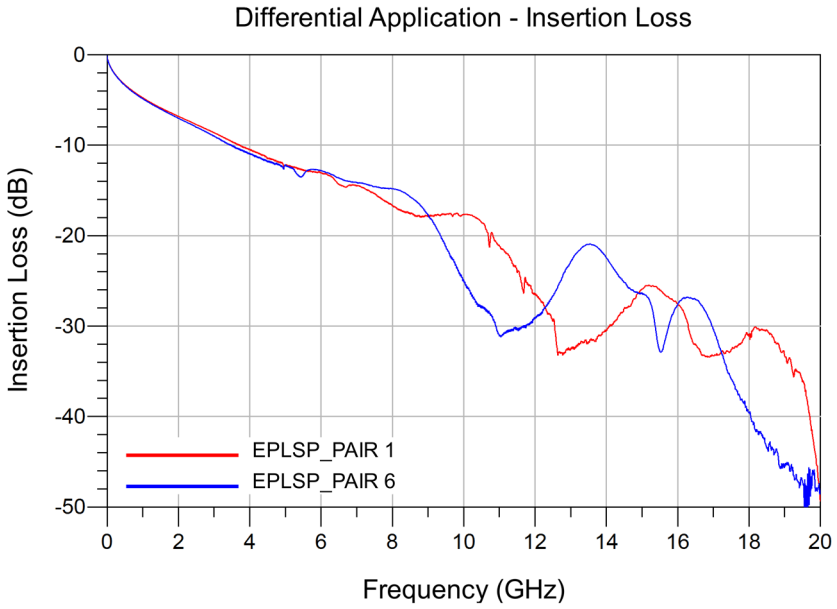
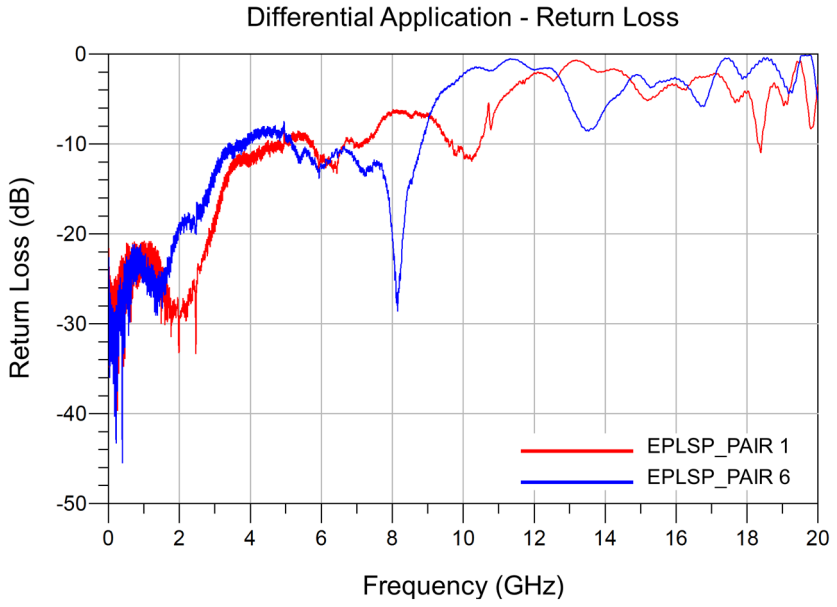
Appendix A – Frequency Domain Response Graphs

Differential Application – Insertion Loss



Differential Application – Return Loss



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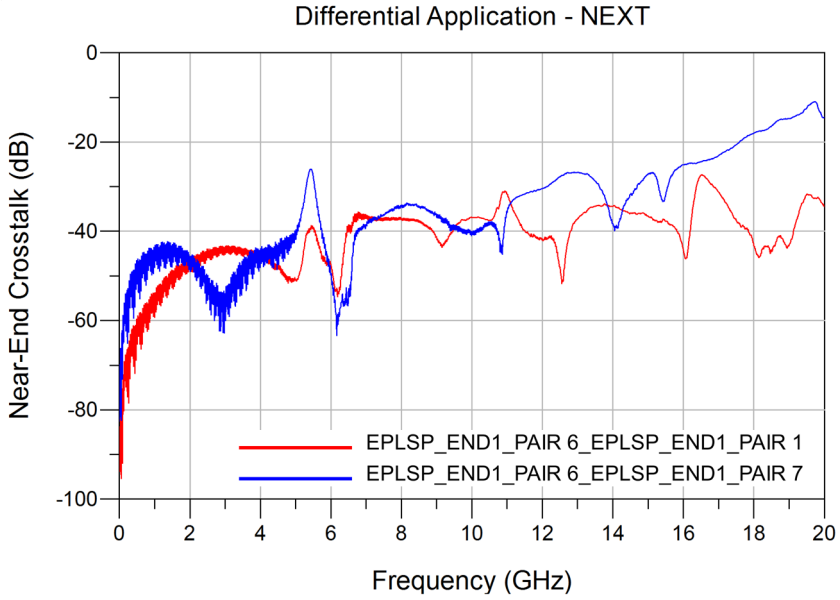
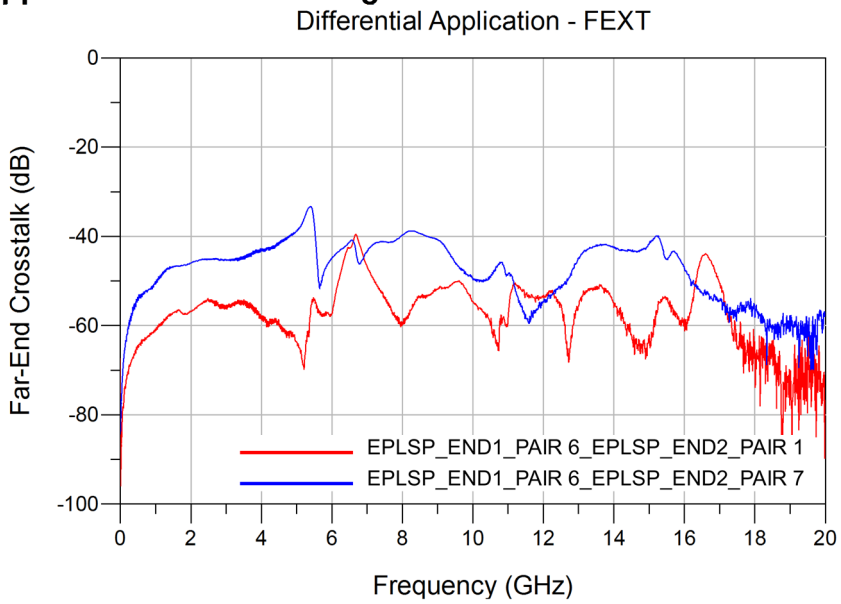
Differential Application – NEXT Configurations



Differential Application – FEXT Configurations



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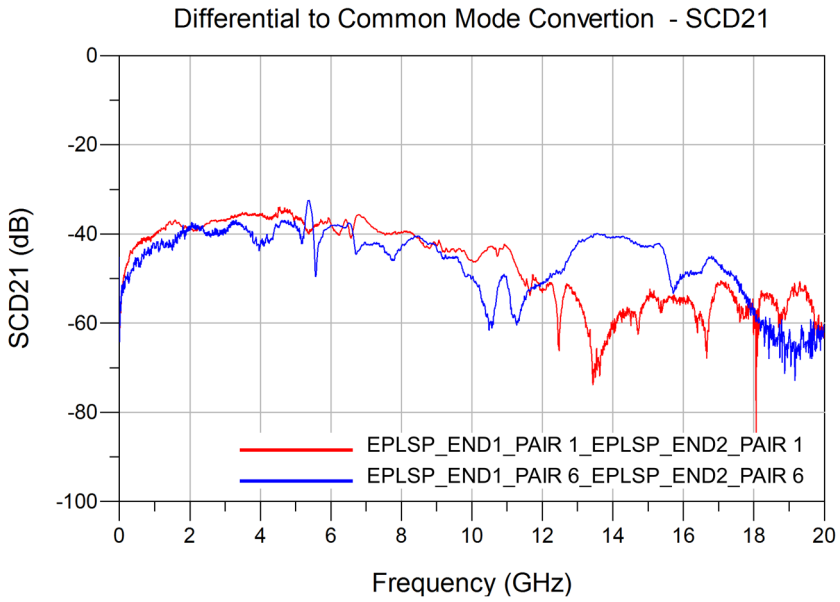
Differential Application – Differential to Common Mode Conversion



Series: EPLSP
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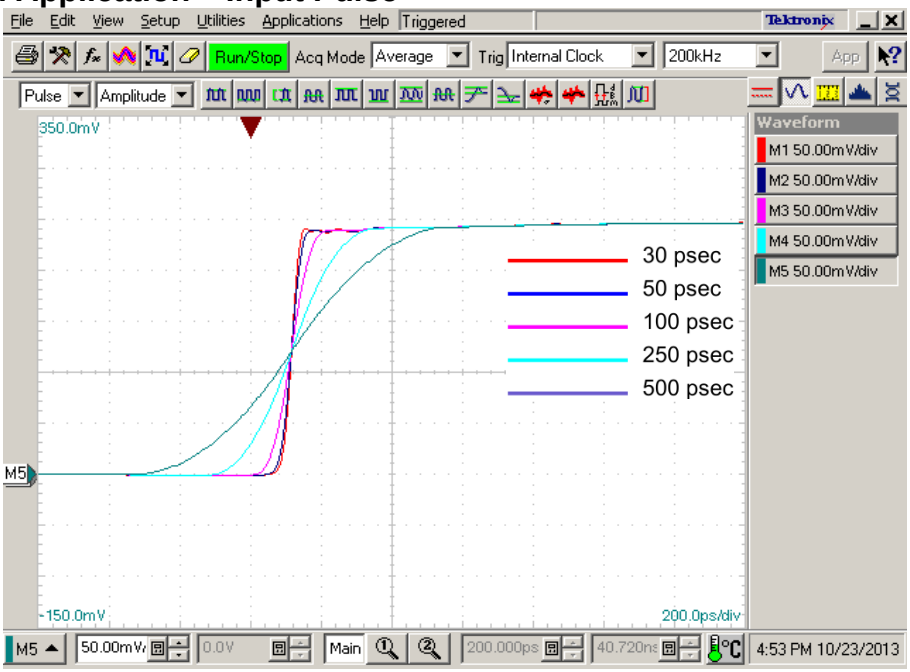
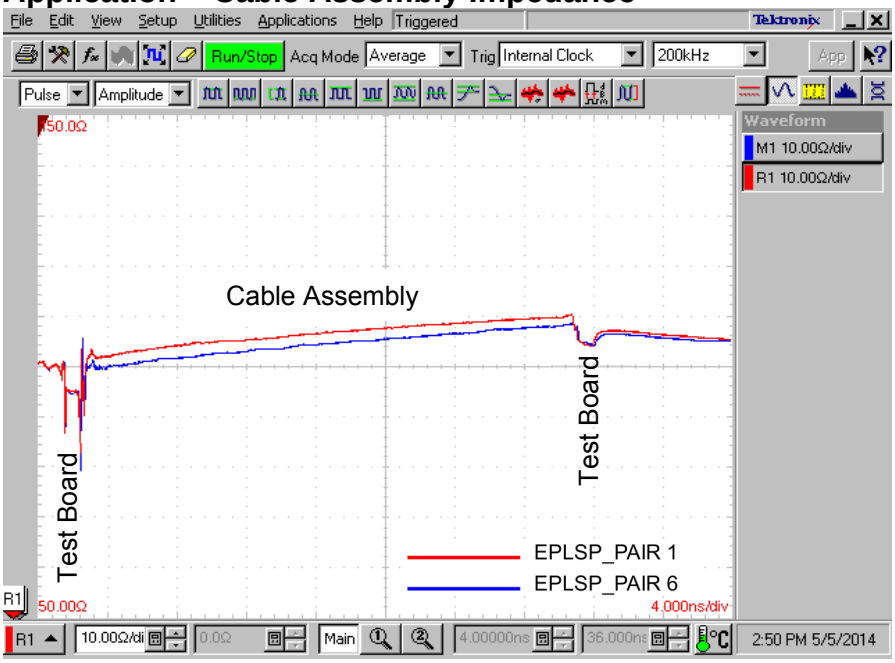
Appendix B – Time Domain Response Graphs

Differential Application – Input Pulse



Differential Application – Cable Assembly Impedance



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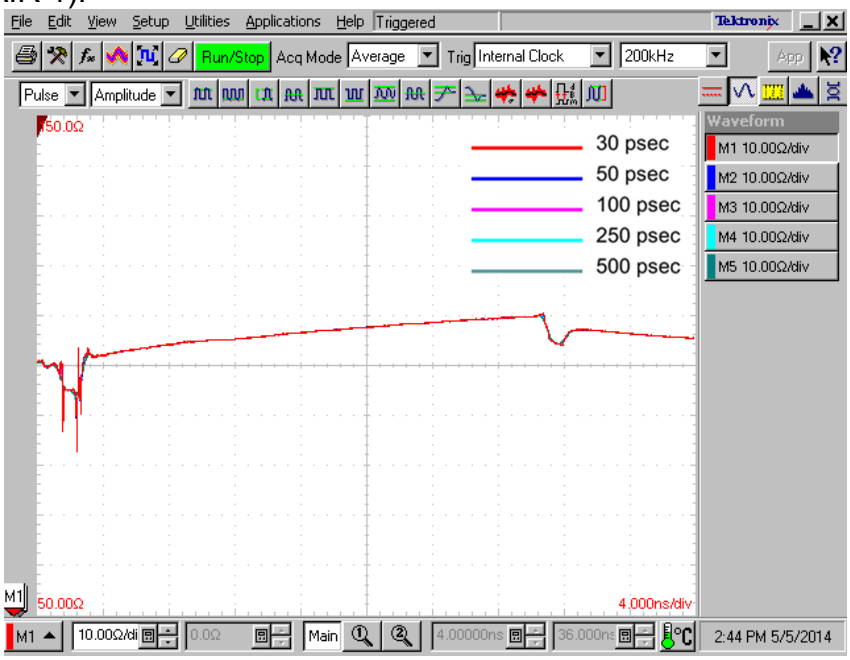
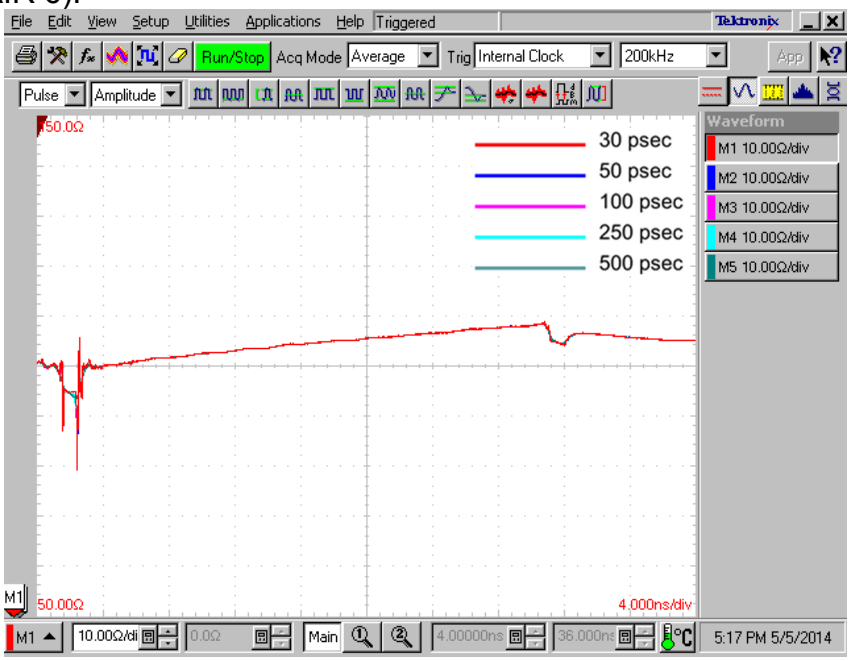
Differential Application – Cable assembly Impedance

Short Low (PAIR 1):



Long Low (PAIR 6):



Series: EPLSP
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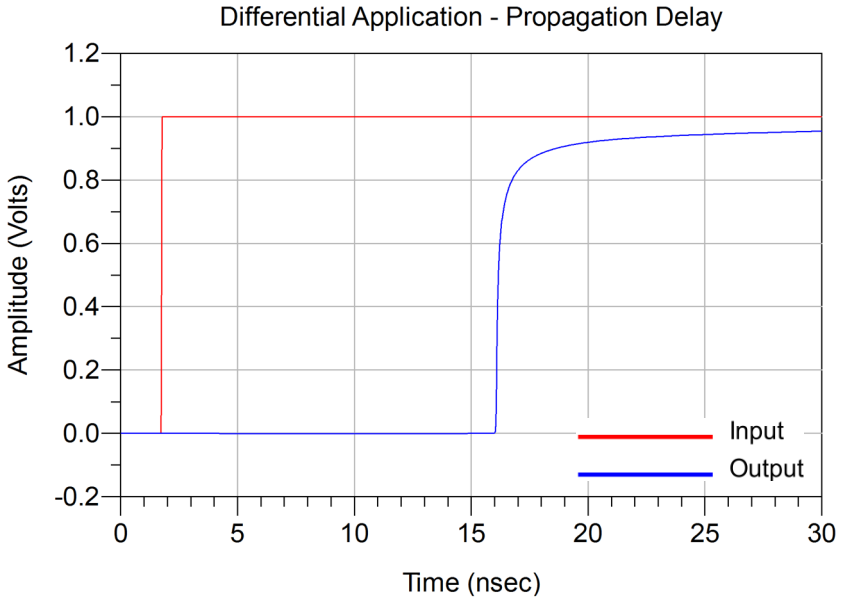
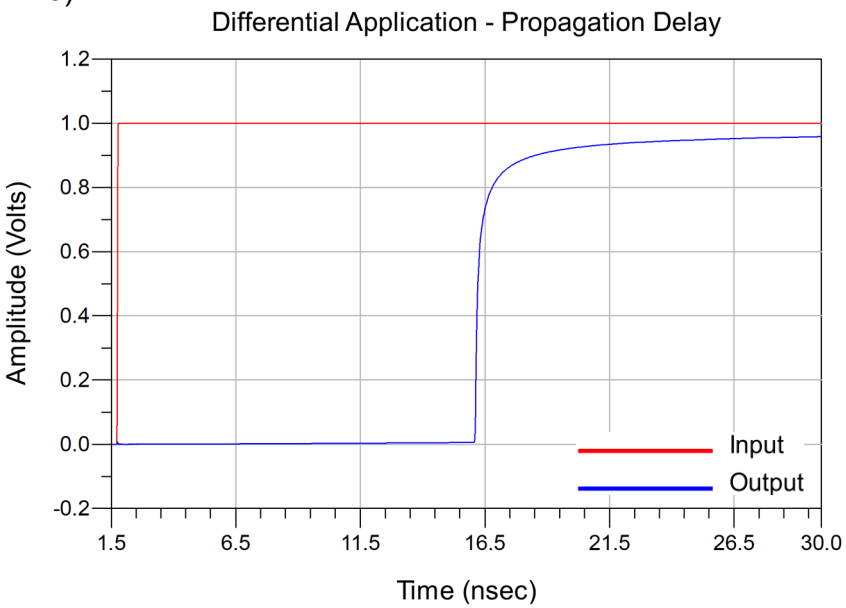
Differential Application – Propagation Delay

Short Low (PAIR 1):



Long Row (PAIR 6):



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Appendix C – Product and Test System Descriptions

Product Description

Product test sample is 0.8mm Eye Speed® Rugged Latching High Speed I/O Cable Assembly. The part number is EPLSP-019-3000, which mate with ERI8-019-S-D-RA. The cable assembly has two rows of 9 signal pairs evenly spaced on a 0.8 mm (0.0315") pitch. A photo of the mated test article mounted to SI test boards is shown below.

The cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in table below. There are a total of 19 positions per row. SMA jack numbers on the test boards correspond to the assembly line numbers. All adjacent lines are terminated where applicable.

G	**P1+**	**P1-**	G	P2+	P2-	G	P3+	P3-	G	P4+	P4-	G	CLK+	CLK-	G	PWR 1	PWR 2	G
G	**P6+**	**P6-**	G	P7+	P7-	G	P8+	P8-	G	P9+	P9-	G	PWR 3	PWR 4	G	PWR 5	PWR 6	G

Table 5: Respective signal line numbers as viewed from End 1

Test System Description

The test fixtures are composed of eight-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures.

Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Two test fixtures specific to the EPLSP series cable assembly identified by part PCB-102231-TST-01. The Auto Fixture Removal (AFR) calibration structures designed specifically for the EPLSP series are on the same test fixture. Displayed on the following pages is the information for the EPLSP/AFR calibration structure and directives for mating EPLSP fixtures.

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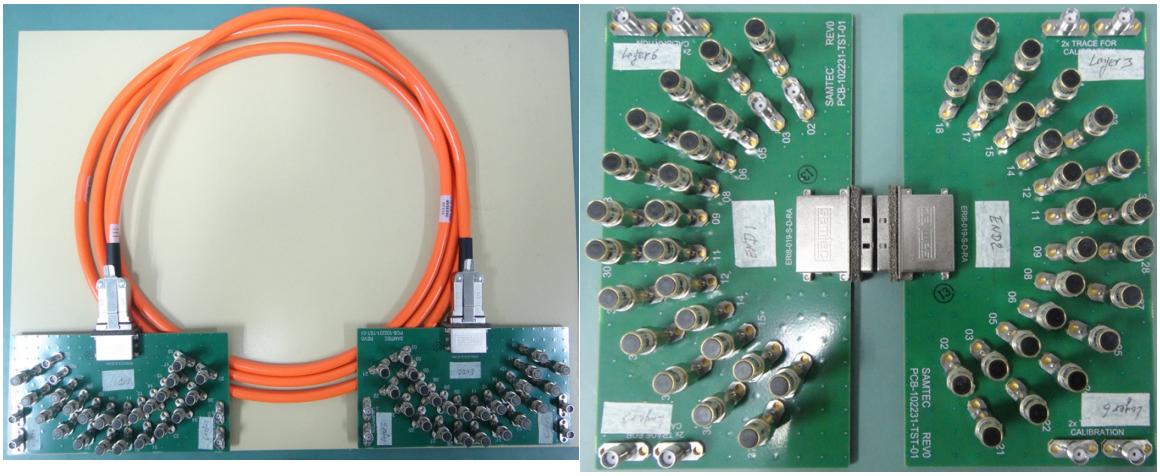
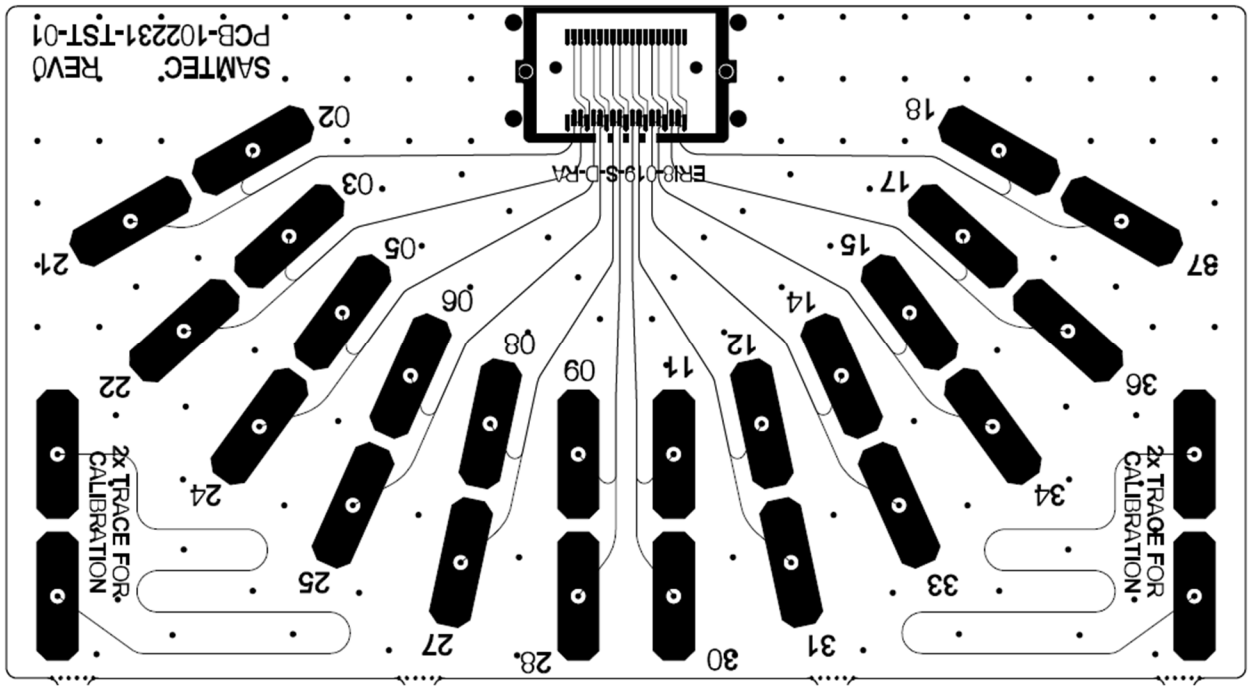
PCB-102231-TST-XX Test Fixtures



Artwork of the PCB design is shown below.



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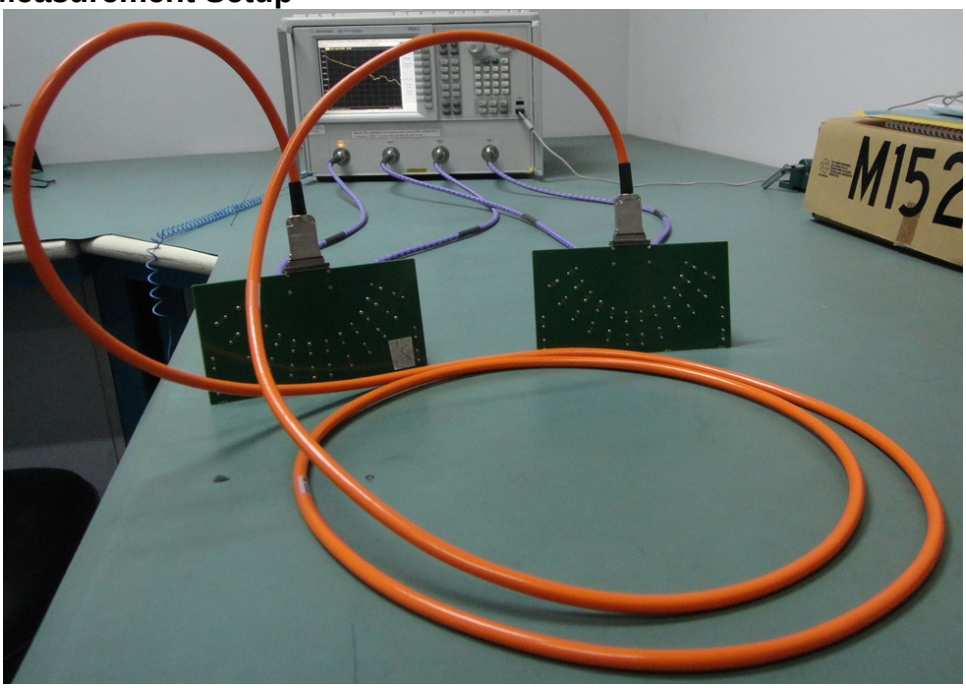
Appendix D – Test and Measurement Setup

The test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz	Number of points -1601
Stop Frequency – 20 GHz	IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

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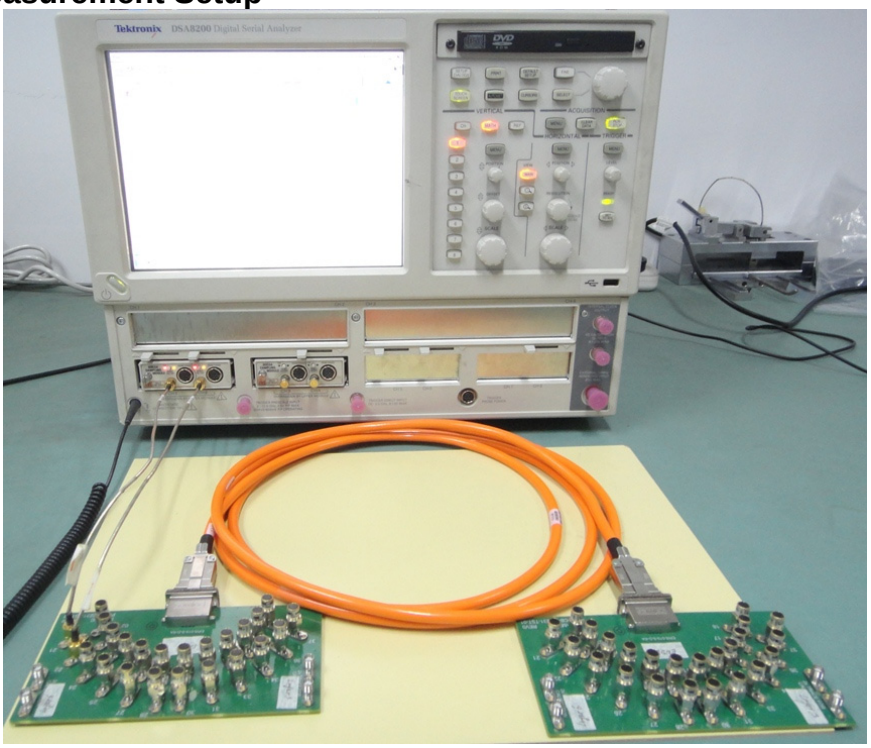
For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale: 10 ohm / Div:
Offset: Default / Scroll
Horizontal Scale: 4ns/ Div
Record Length: 4000
Averages: ≥ 16

DSA8200 Measurement Setup



Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

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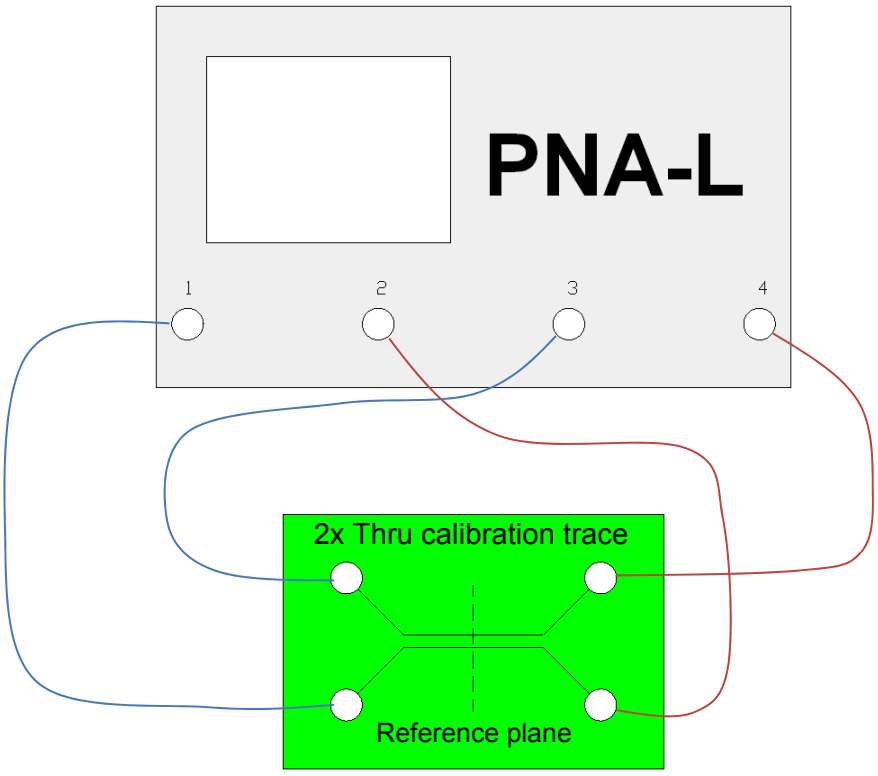
Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-cal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the EPLSP test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.



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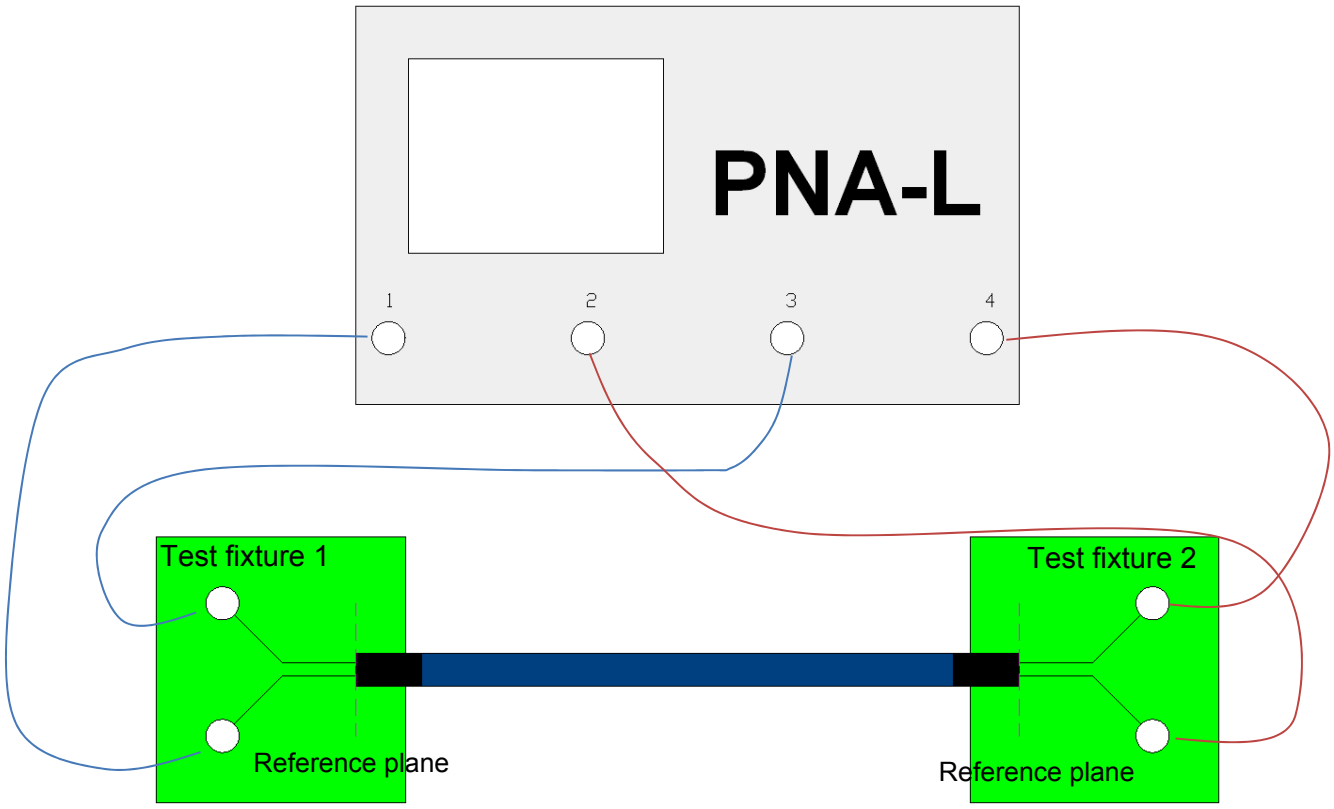
Measurements are then performed using the test boards as shown below. The test board effects are removed in post-processing via AFR in Agilent PLTS. The calibrated reference plane is located 6.5 mils from the connector footprint on each side. The S-Parameter measurements include:

A. 18 mils of 20 mil wide differential microstrip signal trace
B. Test board vias, pads (footprint effects) for the ERI8 connector
C. The ERI8 series connector at one end
D. The EPLSP test cable
E. The ERI8 series connector at another end
F. Test board vias, pads (footprint effects) for the ERI8 connector
G. 18 mils of 20 mil wide differential microstrip signal trace

The figure below shows the location of the measurement reference plane.



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Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with band-width-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Impedance (TDR)
Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

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Appendix F – Glossary of Terms

ADS – Agilent Advanced Design System
AFR – Automatic Fixture Removal
CTLE – Continuous Time Linear Analyzer
CuFireFly™ - Copper FireFly™ assembly
DUT – Device under test
FD – Frequency domain
FEXT – Far-End Crosstalk
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PLTS – Agilent Physical Layer Design System
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
UI – Unit Interval
XROW – Across Row
Z – Impedance (expressed in ohms)