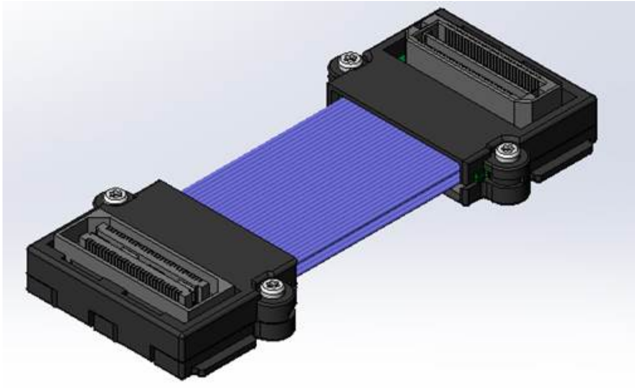
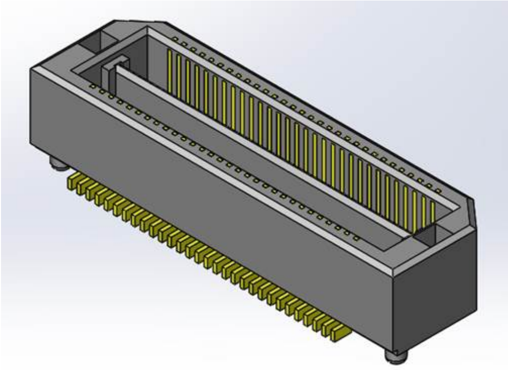
High Speed Characterization Report

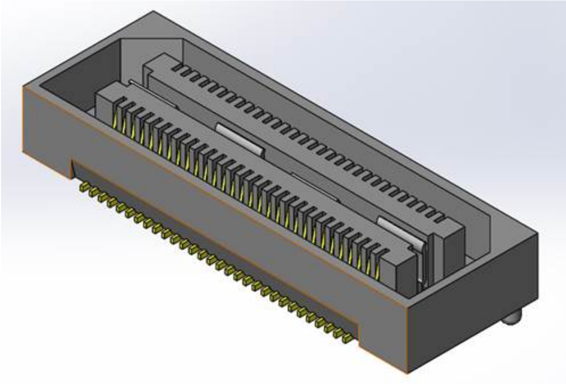
HQCD-XXX-XX.XX-STR-TTL-1



Mated with:

QTH-XXX-01-X-D-A **and** **QSH-XXX-01-X-D-A**





Description:

0.5 mm Q Strip® High Speed Coax Cable Assembly,
38 AWG Micro Ribbon Coax Cable

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Report Revision: 12/15/2015

Series: HQCD
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Series: HQCD
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Cable Assembly Overview

The 0.5 mm (.0197") HQCD Cable Assembly is constructed using 38 AWG micro ribbon coax cable with double row structure. The cable assembly connectors are of the vertical mount (DV) or edge mount (EM) type. The HQCD series cable assemblies are available in 30, 60, 90 and 120 positions per row and 43.7 mm (1.72") length minimum. The data in this report is only applicable to 250 mm and 1000 mm length cable assembly.

The test sample consists of two micro coaxial ribbon cables that contain 30 lines each. At each end of the cable there is a connector that is terminated to a small transition PCB. Each connector is soldered to its respective PCB. The connector terminals are on 0.5 mm centers. The cable assembly is wired to facilitate a Pin 1 to Pin 1 mapping between the cable terminations.

The HQCD cable assemblies were tested by mating to a QTH header at End 1 and to a QSH socket at End 2. One sample of each length assembly was tested. The actual part numbers that were tested are shown in Table 1, which also identifies End 1 and End 2 of each assembly. A relative sample picture is shown in Figure1. Two lines, the longest physical signal path (Long Path) and the shortest physical signal path (Short Path), of each assembly type were tested. The Long Path and Short Path are identified as, STR_57 to TTL_57 and the STR_30 to TTL_30, respectively.

Length	Part Number	End 1	End 2
250 mm	HQCD-030-09.80-STR-TTL-1	STR	TTL
1000 mm	HQCD-030-39.37-STR-TTL -1	STR	TTL

Table 1: Sample Description

Figure 1: Test Sample

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Cable Assembly Speed Rating

The cable assembly Speed Rating is based on the -7 dB insertion loss point of the mated cable assembly. The -7 dB point can be used to estimate usable system bandwidth in a typical two-level signaling environment.

To calculate the Speed Rating, the measured -7 dB point is rounded up to the nearest half-GHz level. The up rounding corrects for any loss from the test board traces. The following table summarizes the Cable Assembly Speed Ratings for the HQCD cable assemblies tested.

Assembly			-7 dB Frequency
HQCD-030-09.80-STR-TTL-1	Single-Ended	Short Path	5.5 GHz
		Long Path	3.5 GHz
HQCD-030-39.37-STR-TTL -1	Single-Ended	Short Path	2.0 GHz
		Long Path	1.5 GHz

Table 2: Cable Assembly Speed Rating

The Samtec Speed Rating is best considered a figure of merit for comparing relative performance between cable assemblies. The Speed Rating becomes less meaningful in systems using multi-level signaling or where crosstalk or impedance mismatch are more critical parameters. Modern high-speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The -7 dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

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Frequency Domain Data Summary

Table 3 – Single-Ended Cable System Performance

Test Parameter	Configuration	Driver	Receiver	0.25m	1m
Insertion Loss	Short Path	STR_30	TTL_30	7dB@ 5.30 GHz	7dB@ 1.75 GHz
	Long Path	STR_57	TTL_57	7dB@ 3.24 GHz	7dB@ 1.40 GHz
Return Loss	Short Path	STR_30	STR_30	>10dB to 5.81 GHz	>10dB to 6.06 GHz
	Long Path	STR_57	STR_57	>10dB to 4.88 GHz	>10dB to 5.63 GHz
Near-End Crosstalk	In Row: Short Path	STR_30	STR_32	<-20dB to 0.34 GHz	<-20dB to 0.40 GHz
	Across Row	STR_30	STR_29	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Long Path	STR_57	STR_55	<-20dB to 0.29 GHz	<-20dB to 0.29 GHz
	Across Row	STR_57	STR_58	<-20dB to 20 GHz	<-20dB to 20 GHz
Far-End Crosstalk	In Row: Short Path	STR_30	TTL_32	<-20dB to 2.99 GHz	<-20dB to 5.16 GHz
	Across Row	STR_30	TTL_29	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Long Path	STR_57	TTL_55	<-20dB to 0.95 GHz	<-20dB to 20 GHz
	Across Row	STR_57	TTL_58	<-20dB to 20 GHz	<-20dB to 20 GHz

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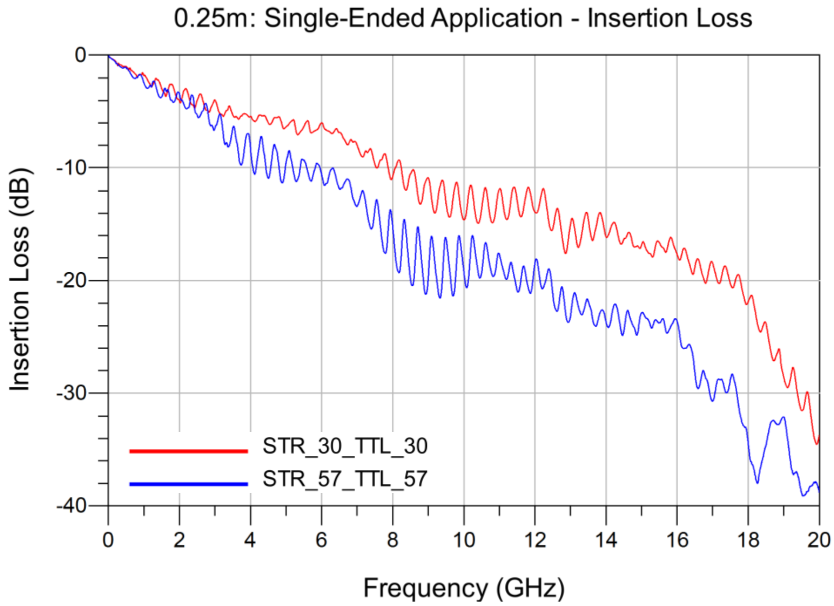
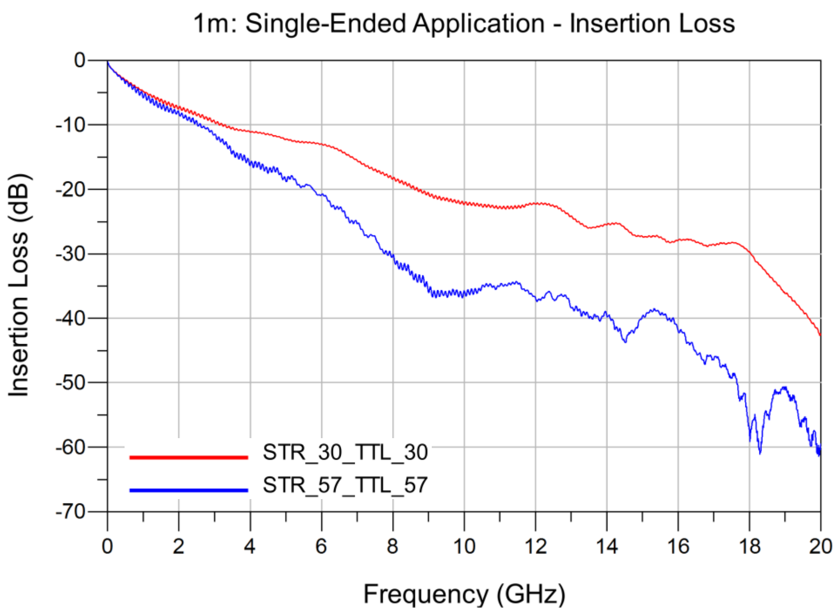
Bandwidth Chart – Single-Ended Insertion Loss





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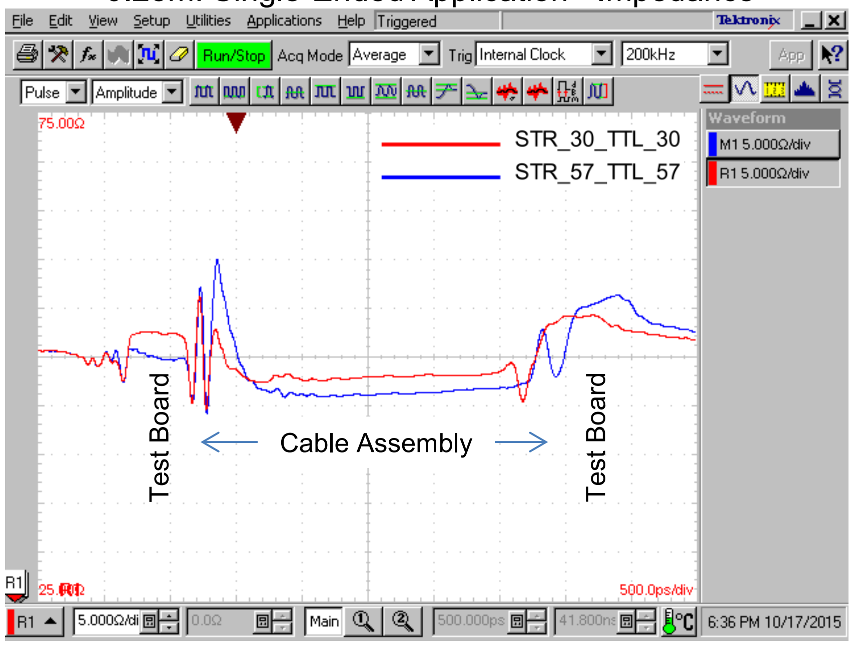
Time Domain Data Summary

0.25m: Single-Ended Application - Impedance



1m: Single-Ended Application - Impedance

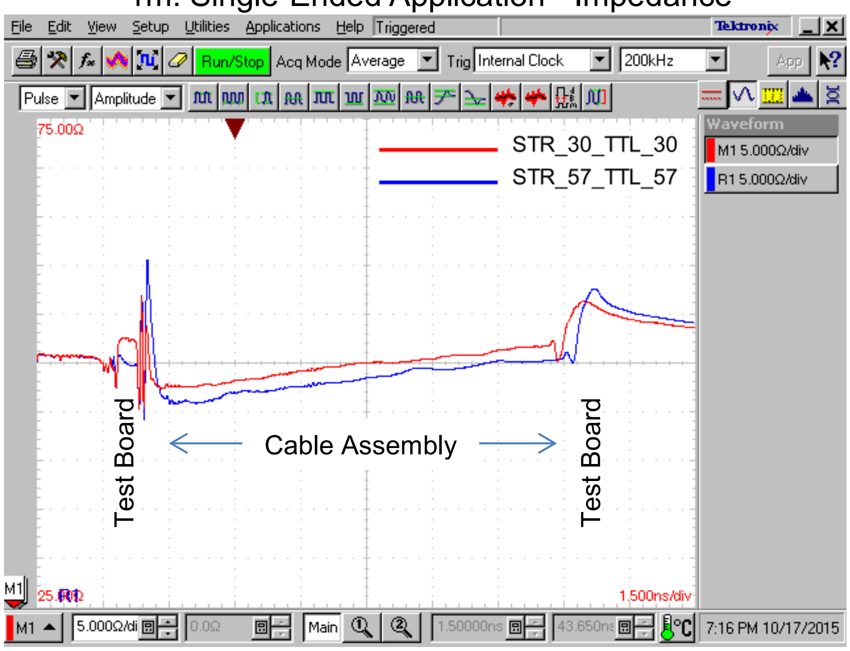


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Table 4 - Propagation Delay (Cable Assembly)

Cable length	Driver/ Receiver	Driver/ Receiver
	STR_30 / TTL_30	STR_57 / TTL_57
0.25m	1.332ns	1.463ns
1m	4.899ns	5.094ns

Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "S" single-ended drive configurations.

Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

For this cable assembly, the following array configurations are evaluated:

Single-Ended Impedance**:**
- Long Path (furthest from test fixture)
- Short Path (closest to test fixture)

Single-Ended Crosstalk**:**
- In Row: Long Path (adjacent terminals in the long row)
- In Row: Short Path (adjacent terminals in the short row)
- Across Row: “Xrow”: (from one row of terminals to the other row)

See Appendix D – Product and Test System Descriptions for details

Only one single-ended signal was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)

In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or the rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate the worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

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Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length and signal propagation time in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix C of this report.

The measured S-Parameters from the network analyzer are post-processed using Agilent ADS to obtain the time domain response for signal propagation time. The Time Domain procedure is provided in Appendix F of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 10 mils of PCB trace on each connector side. Delay is measured at 30 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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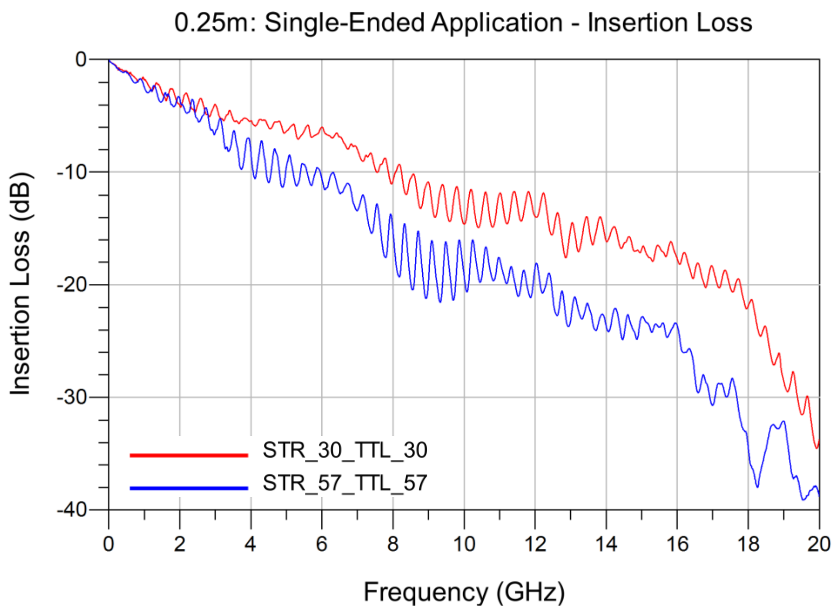
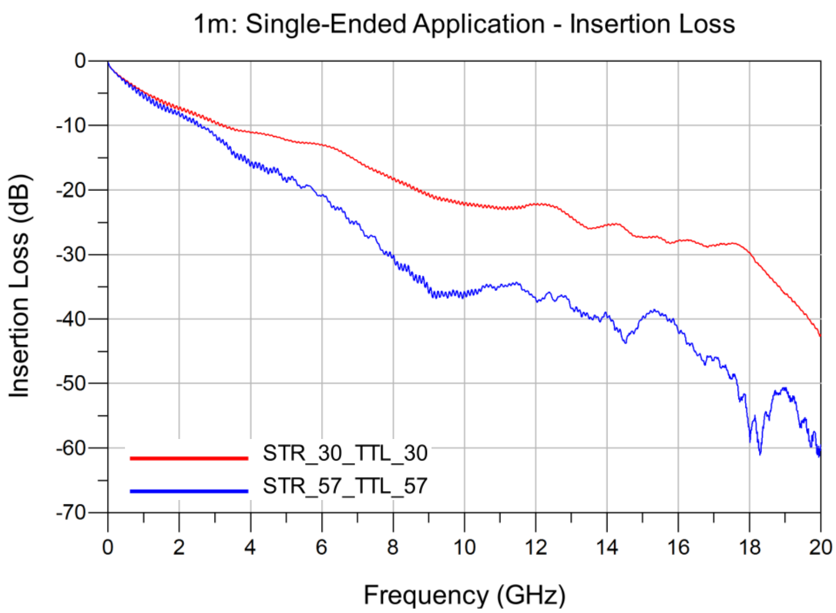
Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss





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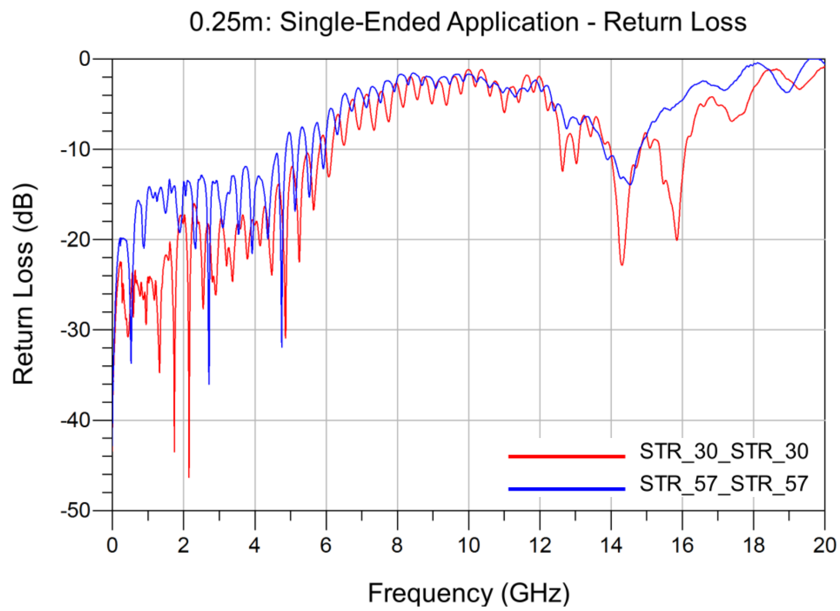
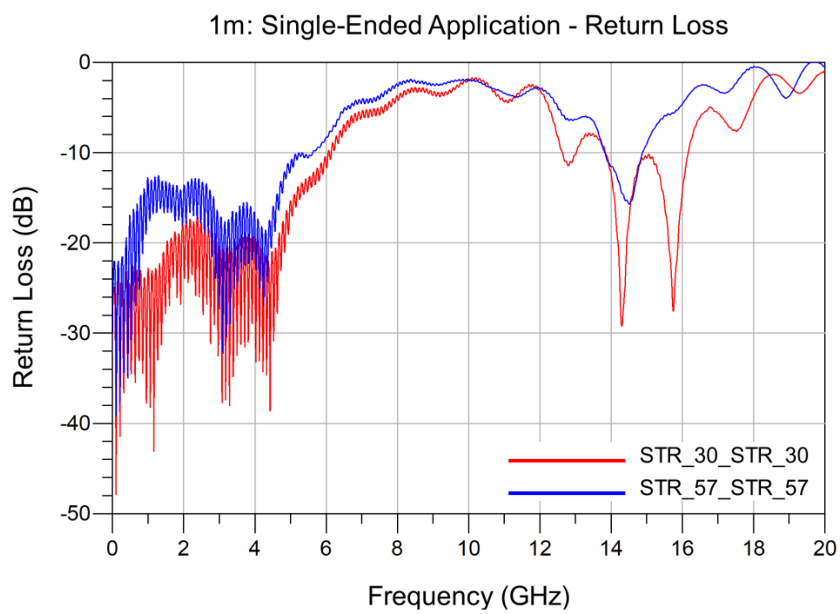
Single-Ended Application – Return Loss





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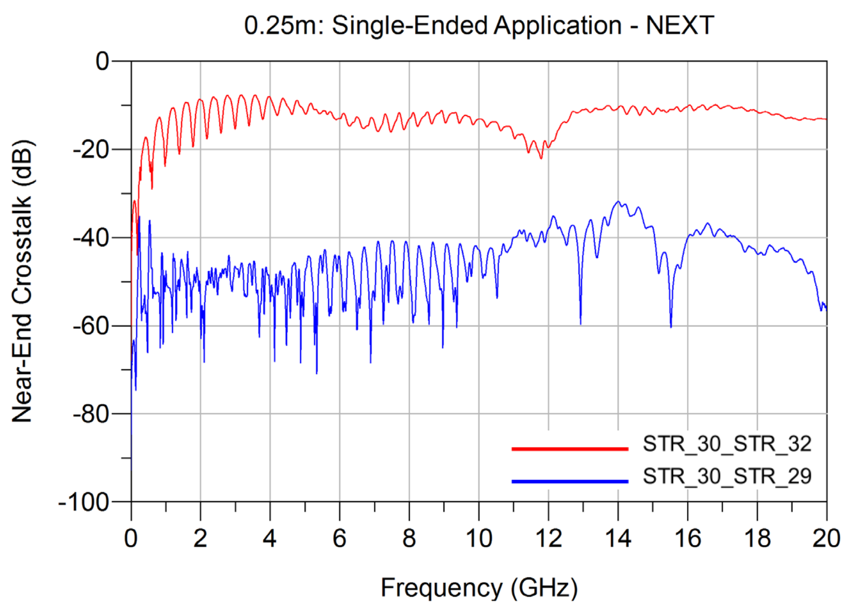
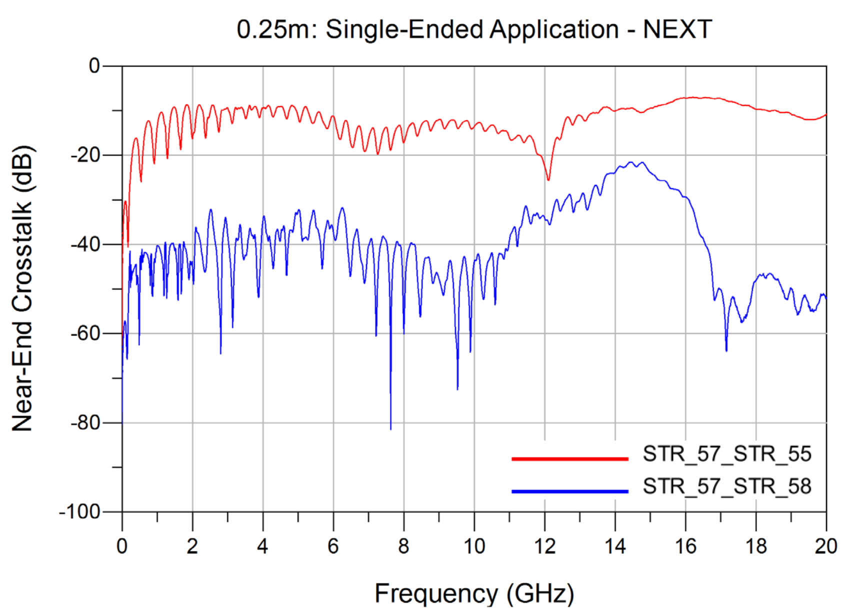
Single-Ended Application – NEXT Configurations





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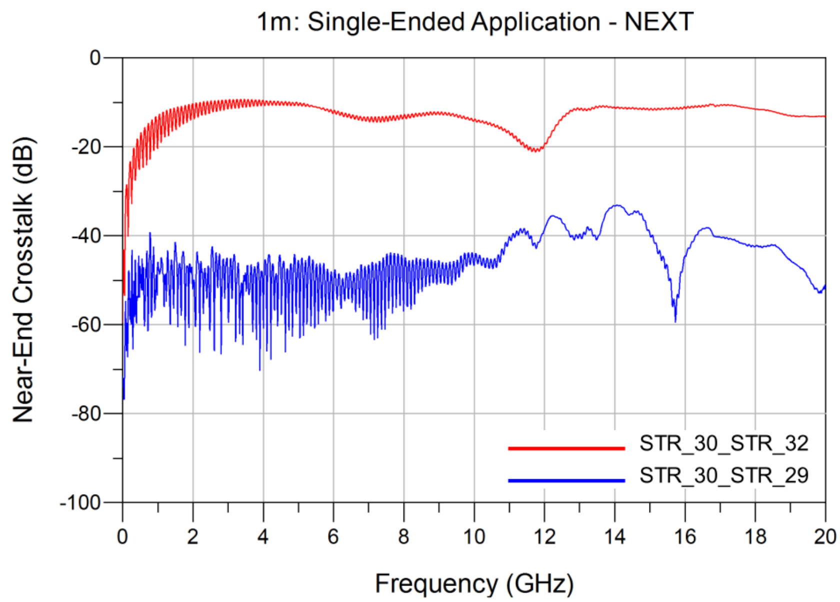
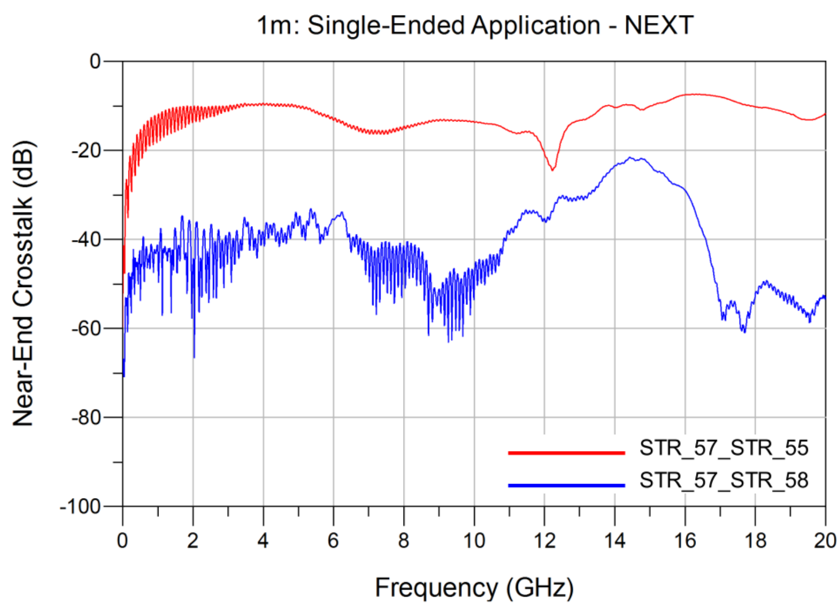
Single-Ended Application – NEXT Configurations (Continued)





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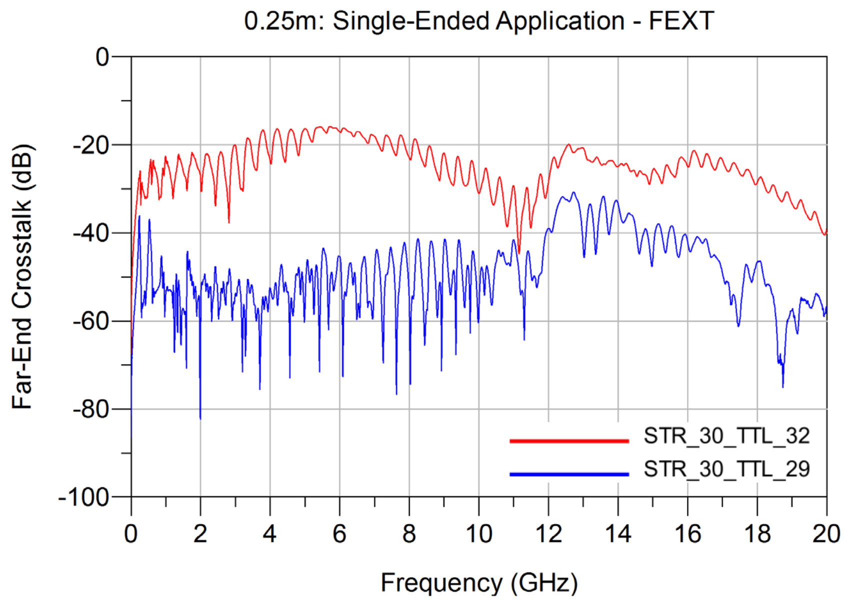
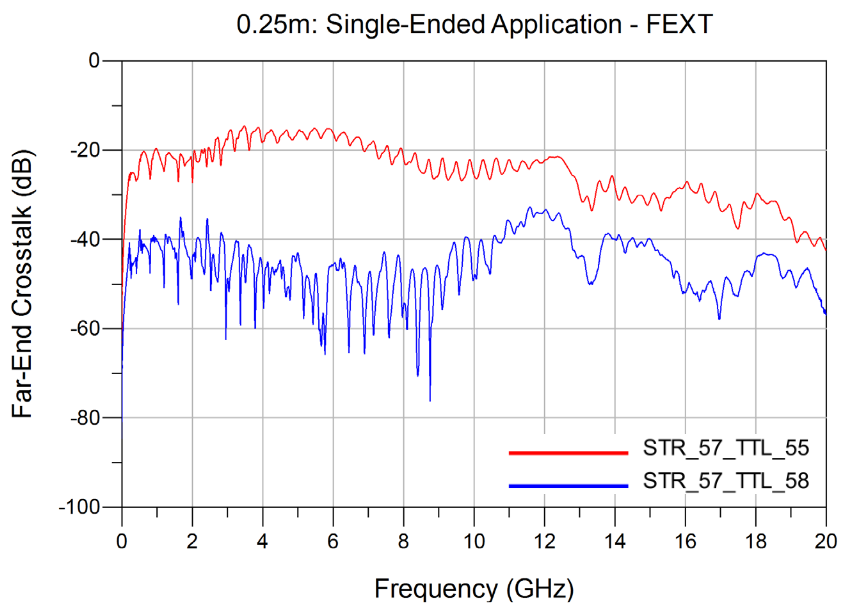
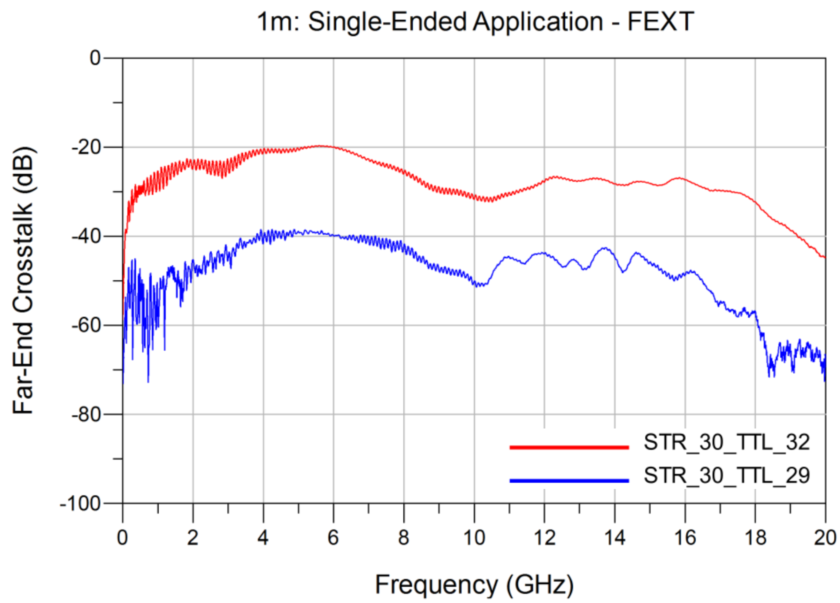
Single-Ended Application – FEXT Configurations

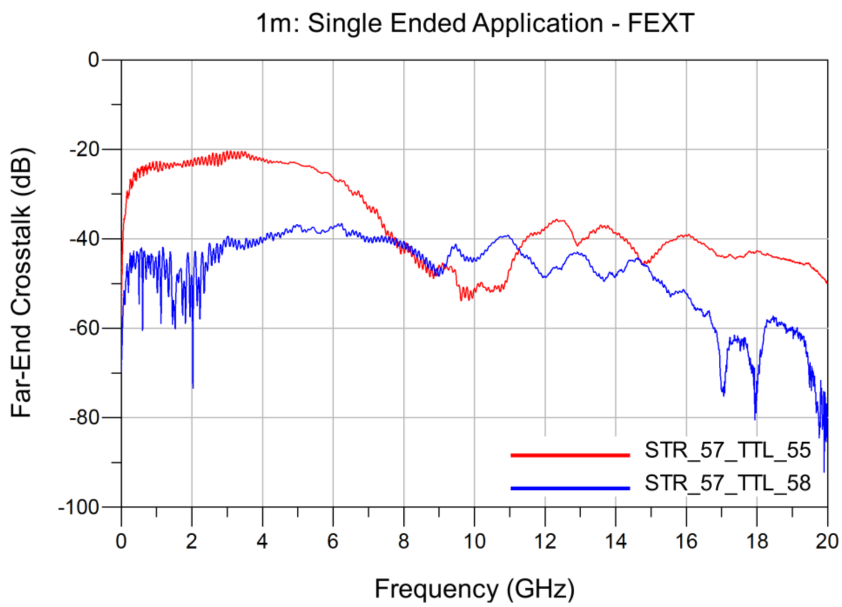




Series: HQCD
Description: 0.5 mm Q Strip® High Speed Coax Cable Assembly, 38 AWG Micro Ribbon Coax Cable

Single-Ended Application – FEXT Configurations (Continued)





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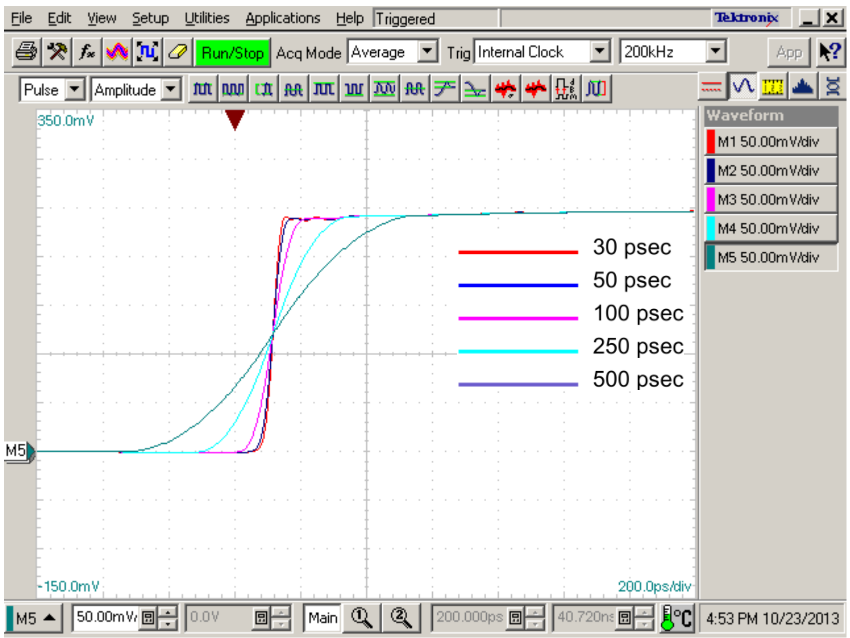
Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse



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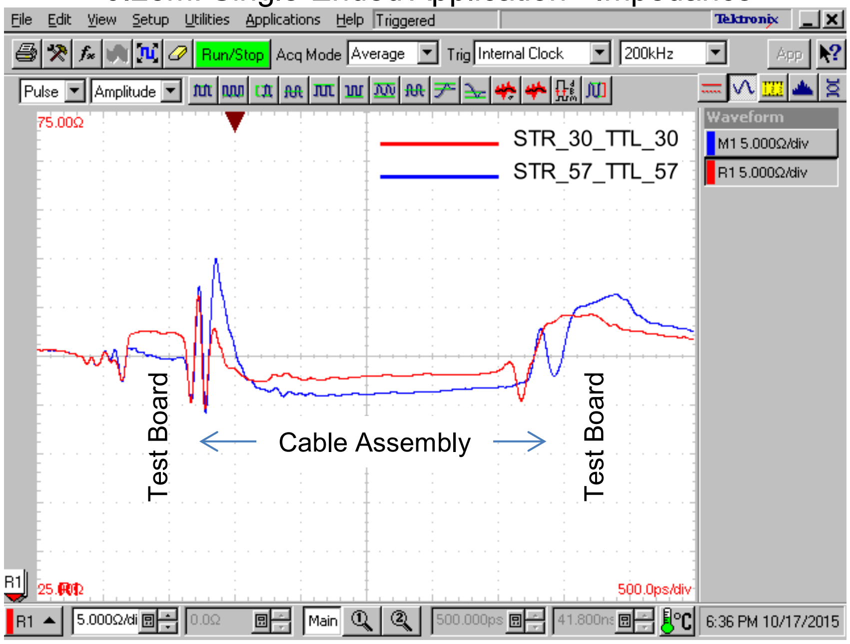
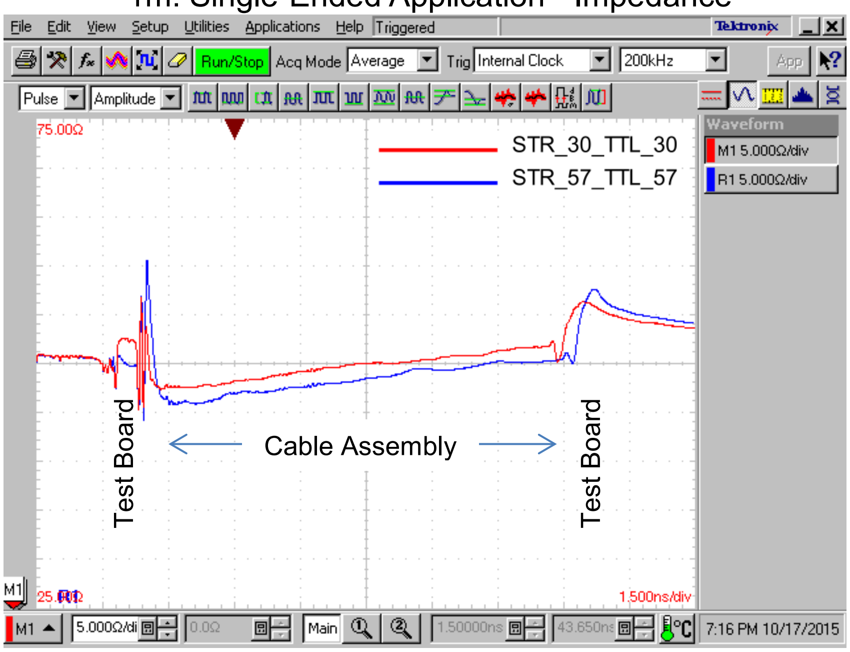
Single-Ended Application – Cable Assembly Impedance

0.25m: Single-Ended Application - Impedance



1m: Single-Ended Application - Impedance



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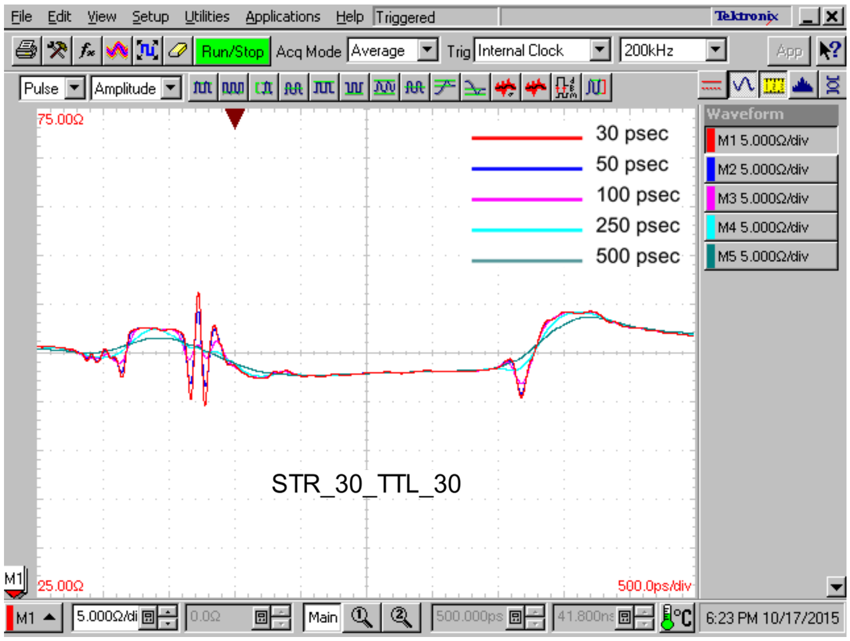
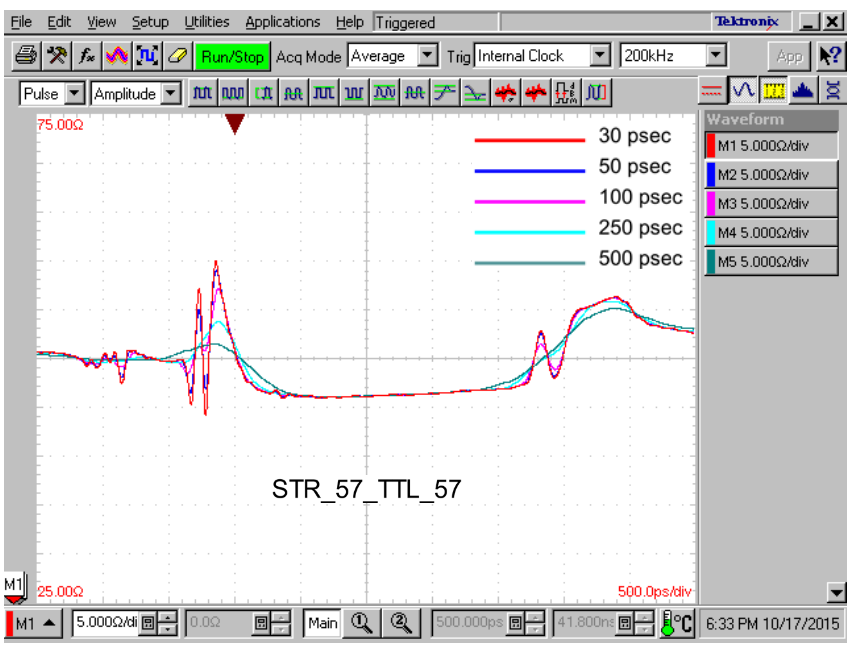
Single-Ended Application – Cable assembly Impedance

HQCD-030-09.80-STR-TTL-1





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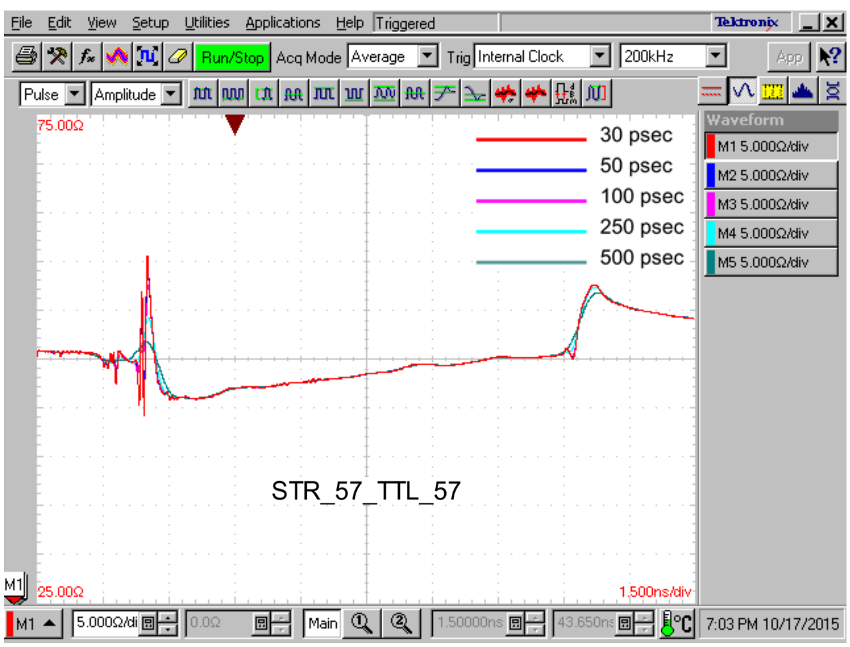
HQCD-030-39.37-STR-TTL-1



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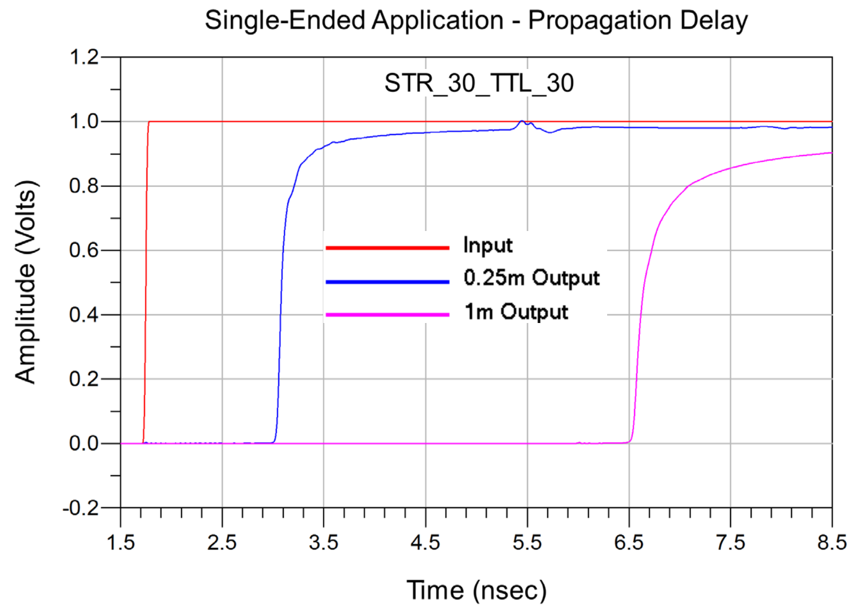
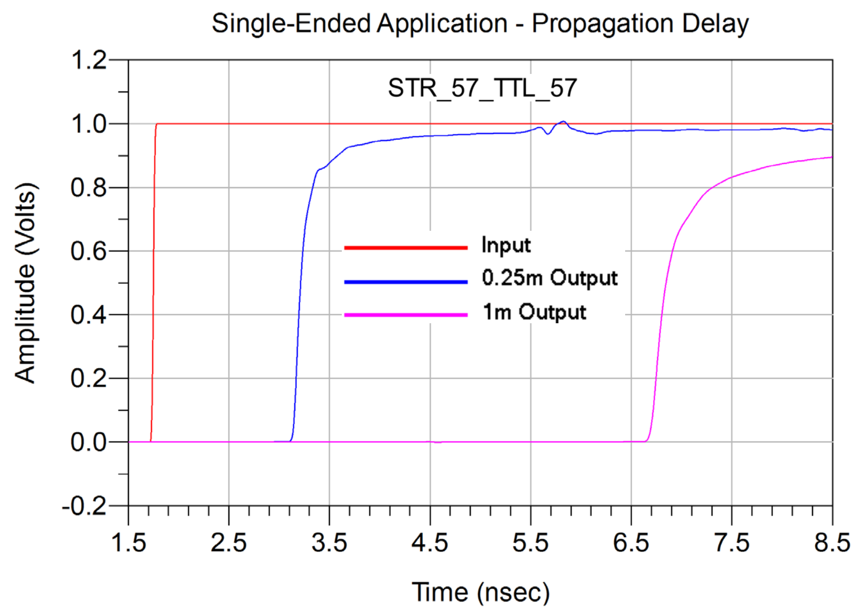
Single-Ended Application – Propagation Delay





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Appendix C – Product and Test System Descriptions

Product Description

Product test samples are 0.5 mm Q Strip® High Speed Coax Cable Assemblies. The part numbers are HQCD-030-09.80-STR-TTL-1 and HQCD-030-39.37-STR-TTL-1. They mate with QTH-030-01-F-D-A and QSH-030-01-F-D-A. A photo of the mated test article mounted to SI test boards is shown below.

The cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in Table 5 below. There are a total of 30 positions per row. All adjacent lines are terminated where applicable.

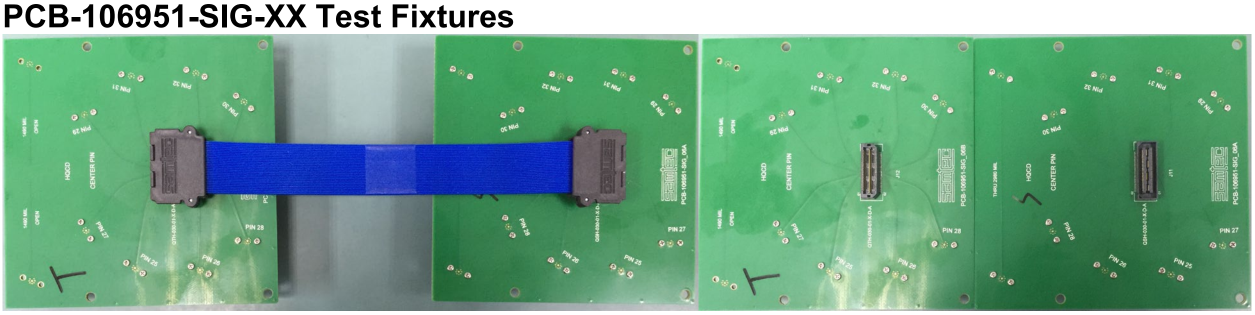
G	G	G	G	G	G	G	G	G	G	T	T	25	27	29	31	T	T	G	G	G	G	G	T	T	51	53	55	57	T
G	G	G	G	G	G	G	G	G	G	T	T	26	28	30	32	T	T	G	G	G	G	G	T	T	52	54	56	58	T

Table 5: Respective signal line numbers as viewed from End 1

Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Two test fixtures are specific to HQCD series cable assemblies and identified by part numbers PCB-106951-SIG-06A and B to PCB-106951-SIG-07A and B. The Auto Fixture Removal (AFR) calibration structures designed specifically for the HQCD series are located on PCB-106951-SIG-06A and 07B. Displayed on the following pages is the information for the HQCD and AFR calibration structure and directives for the mating HQCD fixtures. To keep trace lengths short, two different test board sets were required to access the necessary signal pins.

PCB-106951-SIG-XX Test Fixtures



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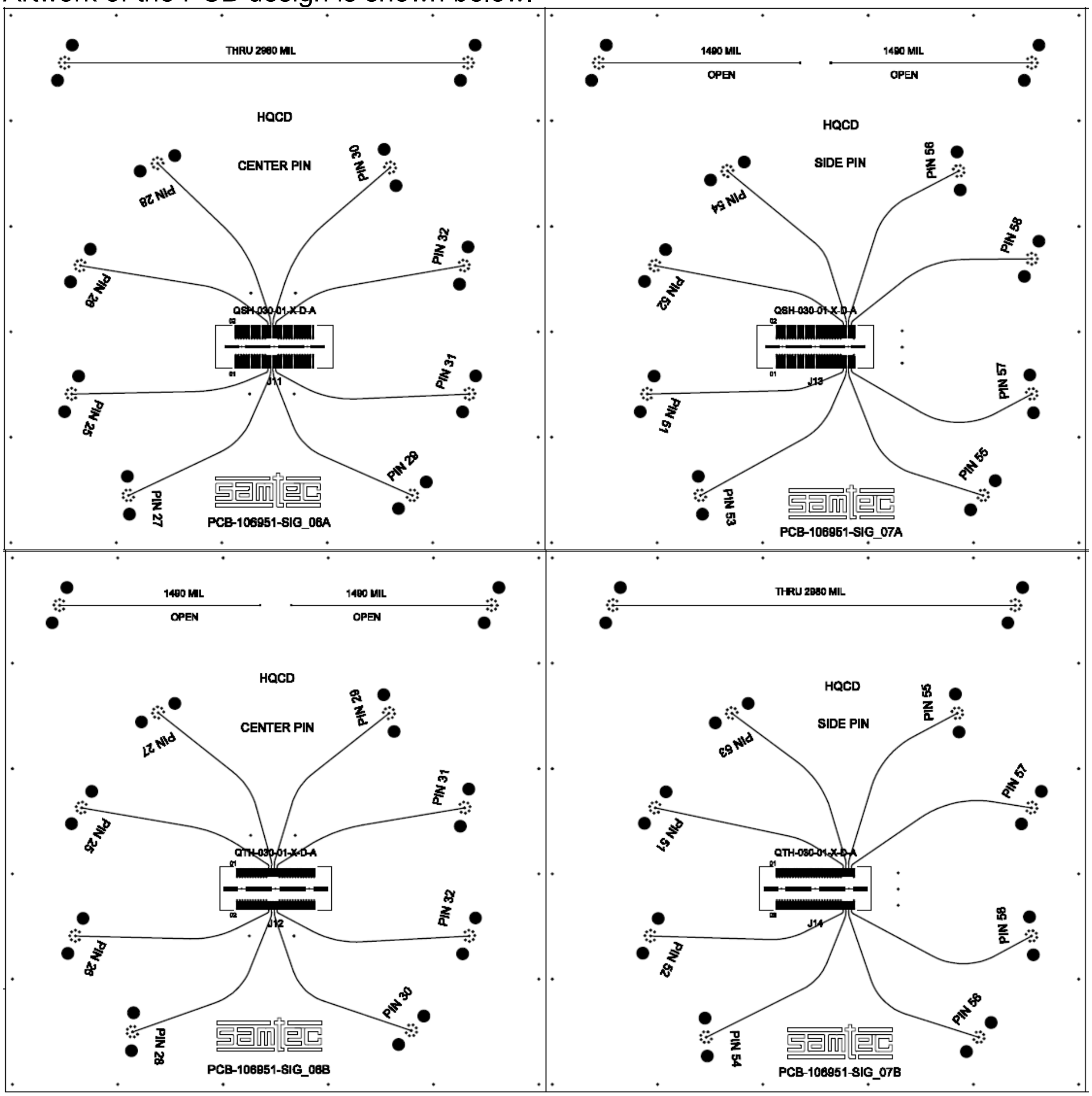
Artwork of the PCB design is shown below.



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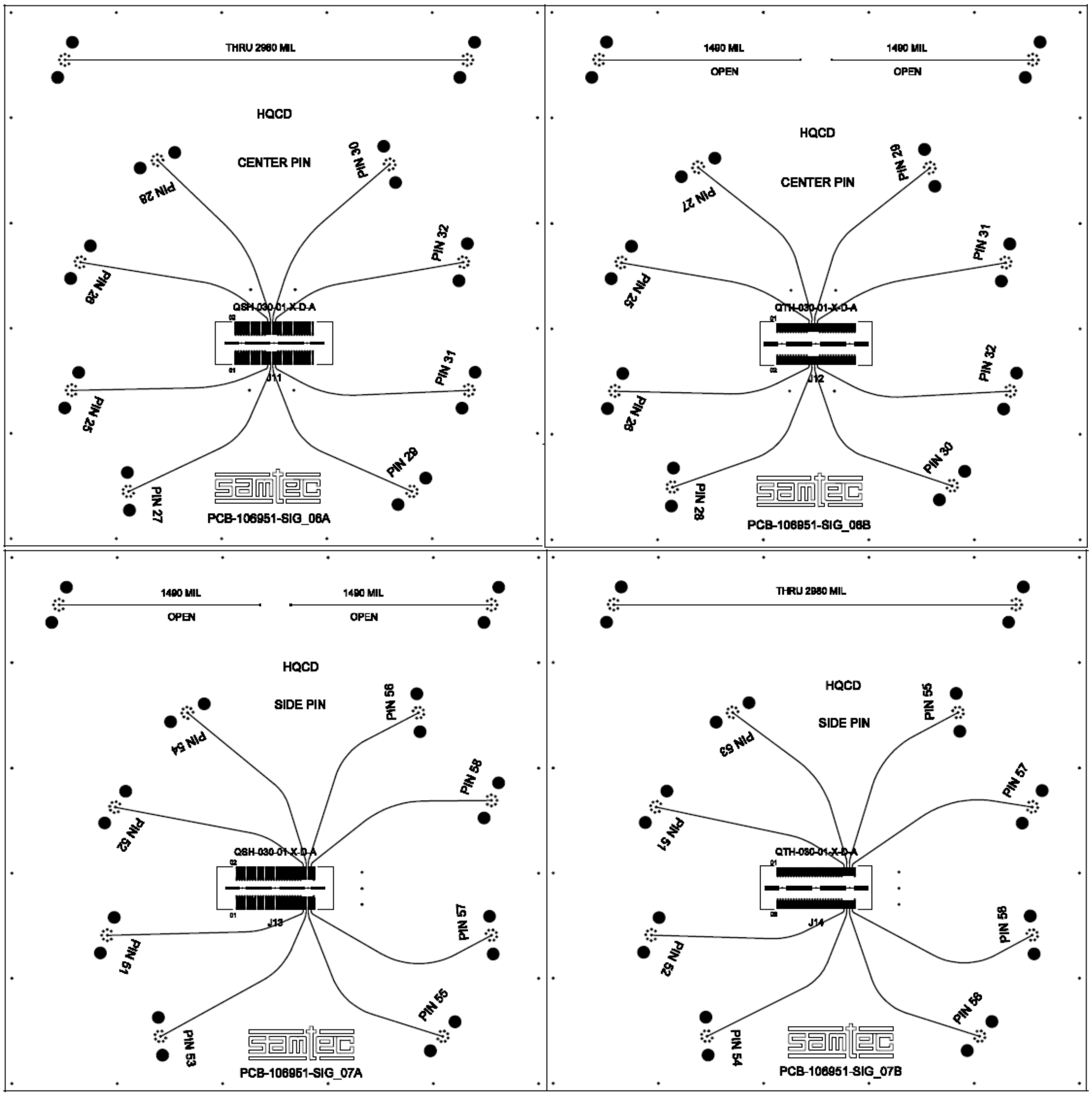
PCB Fixtures

The test fixtures used are as follows:



PCB-106951-SIG-06A– HQCD Cable Test Board 1
PCB-106951-SIG-06B– HQCD Cable Test Board 2
PCB-106951-SIG-07A– HQCD Cable Test Board 3
PCB-106951-SIG-07B– HQCD Cable Test Board 4

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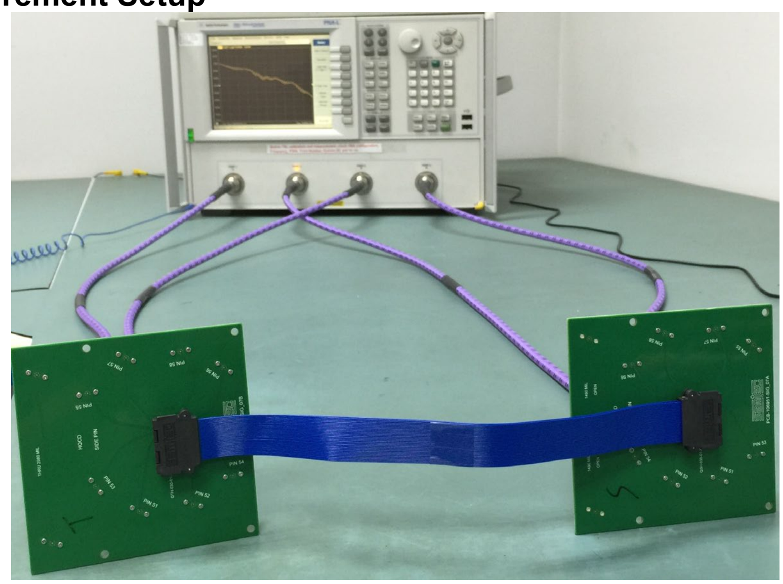
Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are extracted from the instrument by AFR application. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz	Number of points -1601
Stop Frequency – 20 GHz	IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ECAL Module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

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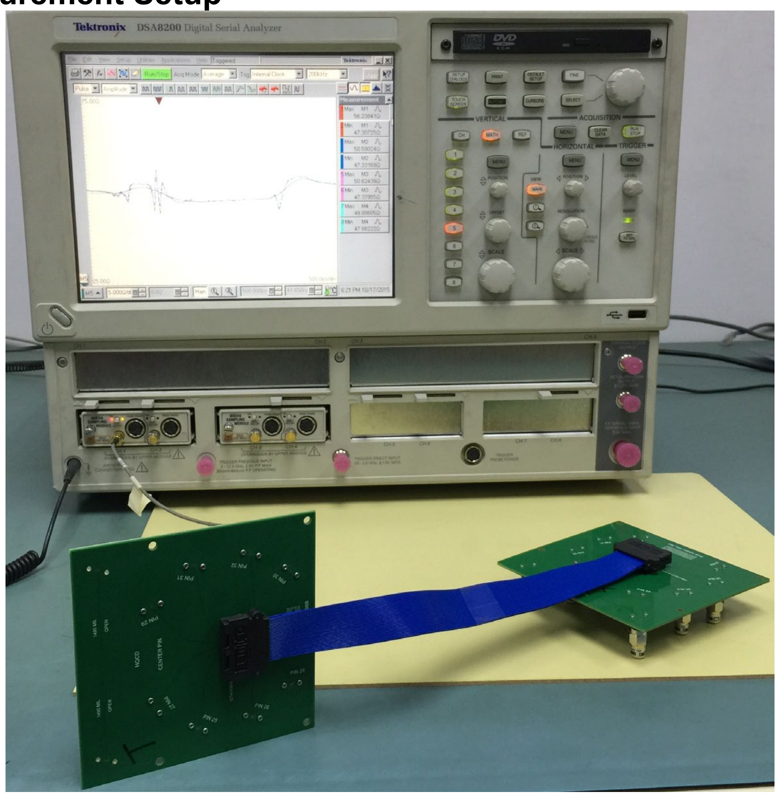
For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale:	5 ohm / Div
Offset:	Default / Scroll
Horizontal Scale:	500ps/ Div or 1.5ns/ Div
Record Length:	4000
Averages:	≥ 16

DSA8200 Measurement Setup



Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: HQCD
Description: 0.5 mm Q Strip® High Speed Coax Cable Assembly, 38 AWG Micro Ribbon Coax Cable

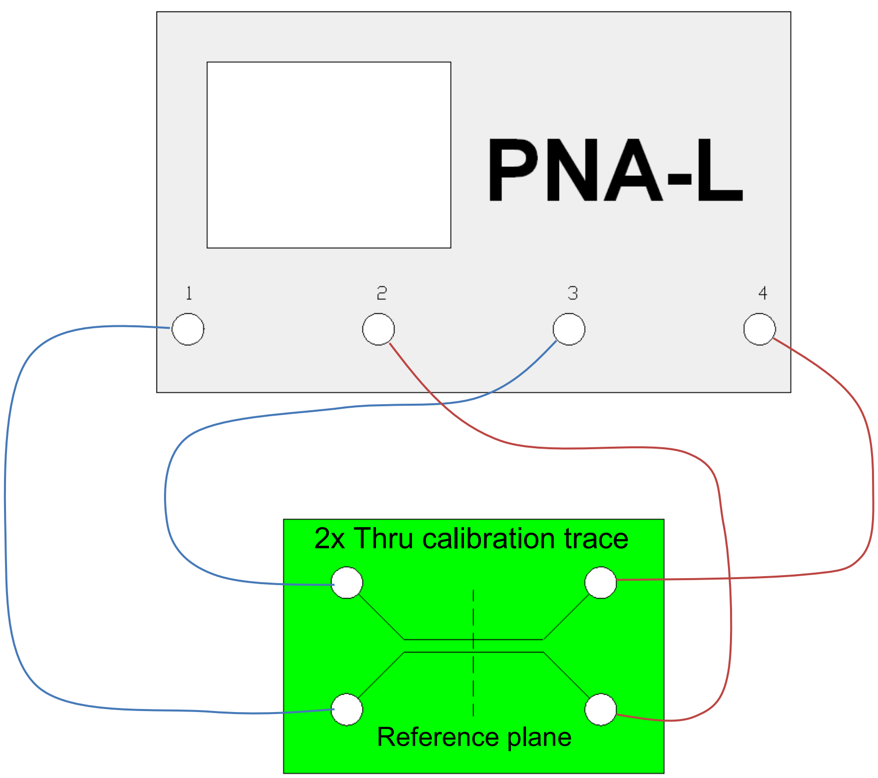
Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-CAL module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the HQCD test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.



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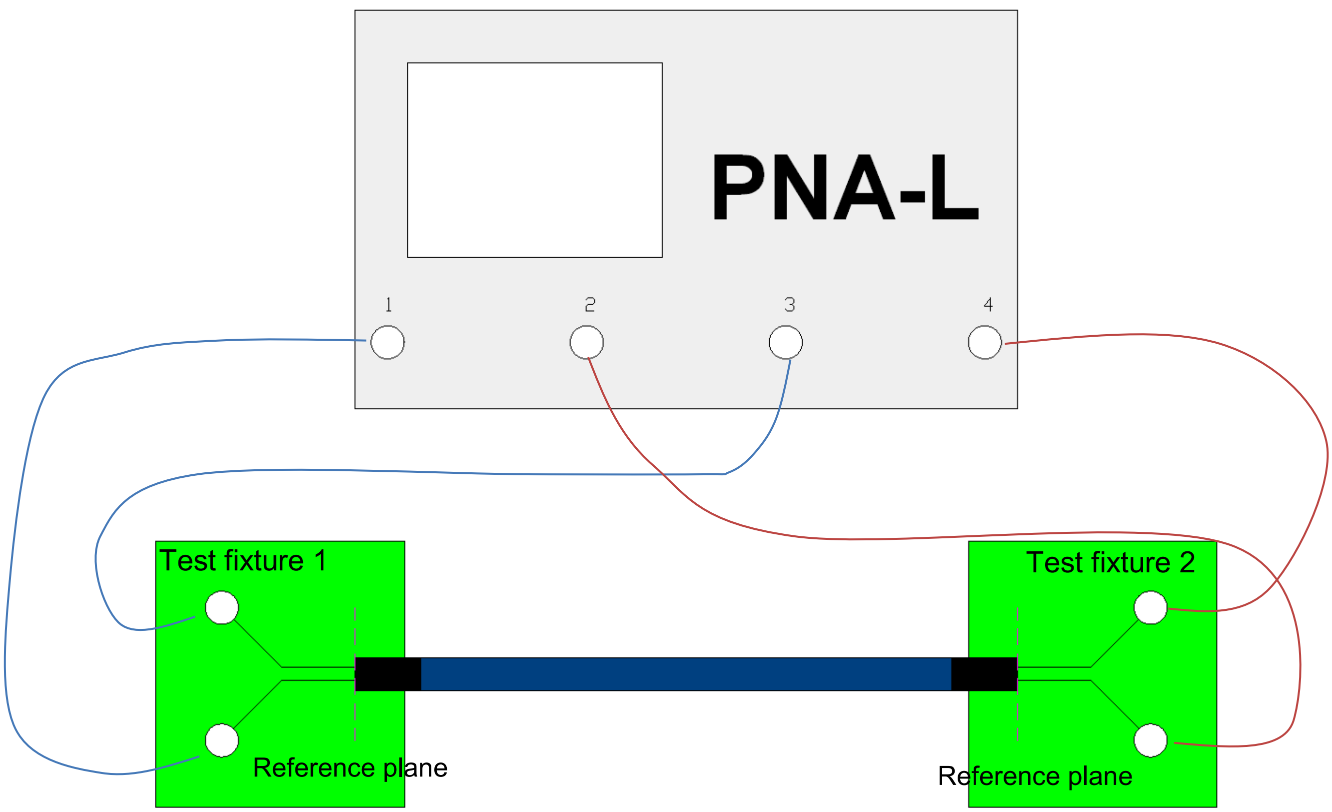
Measurements are then performed using the test boards as shown below. The test board effects are removed in post-processing via AFR in Agilent PLTS. The calibrated reference plane is located at the middle of the connector footprint on each side. The S-Parameter measurements include:

A. Test board vias, pads (footprint effects) for the QTH connector
B. The QTH series connector
C. The HQCD-030-XX.XX-STR-TTL-1 test cable
D. The QSH series connector
E. Test board vias, pads (footprint effects) for the QSH connector

The figure below shows the location of the measurement reference plane.



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Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Impedance (TDR)
Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

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Appendix F – Glossary of Terms

ADS – Agilent Advanced Design System
AFR – Automatic Fixture Removal
CTLE – Continuous Time Linear Analyzer
CuFireFly™ - Copper FireFly™ assembly
DUT – Device under test
FD – Frequency domain
FEXT – Far-End Crosstalk
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PLTS – Agilent Physical Layer Design System
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
UI – Unit Interval
XROW – Across Row
Z – Impedance (expressed in ohms)