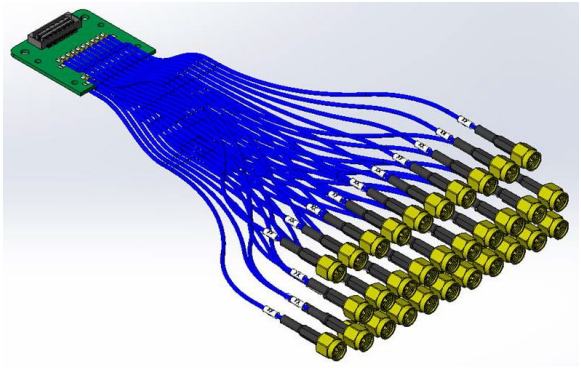
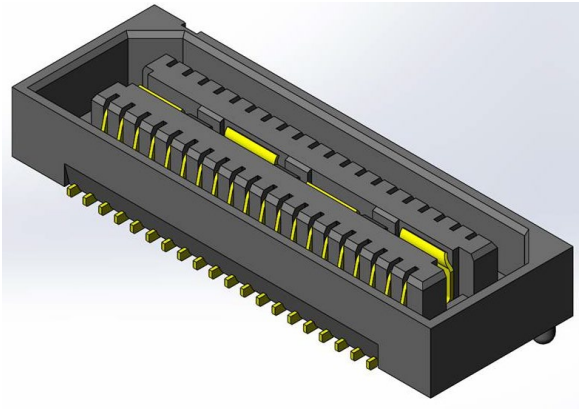
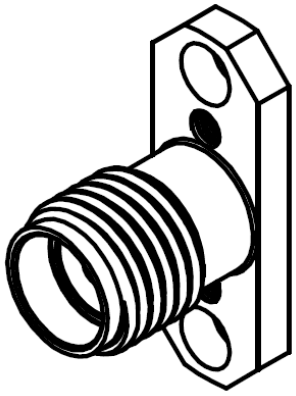
High Speed Characterization Report

EQRF-020-XX-T-L-SMA-P-1



Mated with:
QSE-020-01-X-D-A and SMA-50





Description:

0.80 mm Q Strip® High-Speed Combination RF Coax Cable Assembly

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Cable Assembly Overview

The 0.80 mm (.0315") pitch EQRF High Speed Coax Cable Assembly is available with 40, 80 signal lines. The data in this report is applicable to 250mm and 1000mm cable lengths.

The test sample consists of forty RG-316 coaxial cables. At one end of the cable assembly each cable terminated to a small transition PCB having a QTE header connector soldered to the PCB. The QTE connector contains 20 pins per row. The other ends of the cables are terminated in SMA male connectors (plugs).

There is a small label near the SMA end of each cable bearing a number that corresponds to the QXE terminal number at the other end of the assembly. Figure 1 on the following page is a picture of the termination configurations of the test sample.
One sample of each length assembly was tested. The actual sample part number that was tested is shown below in Table 1, which also identifies End 1 and End 2 of the assembly. Two lines, the longest and the shortest electrical paths, of the sample were tested. Two lines, the longest physical signal path (Long Path) and the shortest physical signal path (Short Path), of each assembly type were tested. The Long Path and Short Path are identified as, QTE_ 1 to SMA_1 and the QTE_18 to SMA_18, respectively.

Length	Part Number	End 1	End 2
250 mm	EQRF-020-0250-T-L-SMA-P-1	QTE	SMA Plug
1000 mm	EQRF-020-1000-T-L-SMA-P-1	QTE	SMA Plug

Table 1: Sample Description

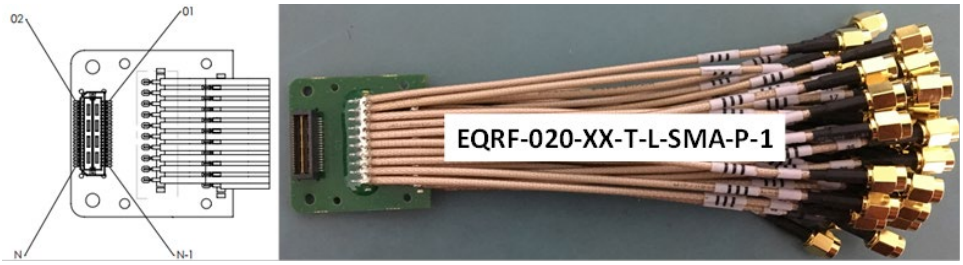

Figure 1: Test Sample

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Cable Assembly Speed Rating

The cable assembly Speed Rating is based on the –7 dB insertion loss point of the mated cable assembly. The –7 dB point can be used to estimate usable system bandwidth in a typical two-level signaling environment. The following table summarizes the Cable Assembly Speed Ratings for the EQRF cable assemblies tested.

Assembly			-7 dB Frequency
EQRF-020-0250-T-L-SMA-P-1	Single Ended	Long Path	4.8 GHz
		Short Path	4.3 GHz
EQRF-020-1000-T-L-SMA-P-1	Single Ended	Long Path	4.5 GHz
		Short Path	4.2 GHz

Table 2: Cable Assembly Speed Rating

The Samtec Speed Rating is best considered a figure of merit for comparing relative performance between cable assemblies. The Speed Rating becomes less meaningful in systems using multi-level signaling or where crosstalk or impedance mismatch are more critical parameters. Modern high-speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The –7 dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

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Frequency Domain Data Summary

Table 3 – Cable Assembly System Performance					
Test Parameter	**Configuration**	**Driver**	**Receiver**	**0.25m**	**1m**
Insertion Loss	Long Path	QTE_1	SMA_1	7dB@ 4.8 GHz	7dB@ 4.5 GHz
	Short Path	QTE_18	SMA_18	7dB@ 4.3 GHz	7dB@ 4.2 GHz
Return Loss	Long Path	QTE_1	QTE_1	>10dB to 2.7 GHz	>10dB to 2.8 GHz
	Short Path	QTE_18	QTE_18	>10dB to 2.3 GHz	>10dB to 2.7 GHz
Near-End Crosstalk	In Row: Long Path	QTE_1	QTE_3	<-20dB to 0.7 GHz	<-20dB to 0.7 GHz
	Across Row	QTE_1	QTE_2	<-20dB to 11.7 GHz	<-20dB to 11.7 GHz
	In Row: Short Path	QTE_18	QTE_20	<-20dB to 0.7 GHz	<-20dB to 0.7 GHz
	Across Row	QTE_18	QTE_17	<-20dB to 20 GHz	<-20dB to 13.6 GHz
Far- End Crosstalk	In Row: Long Path	QTE_1	SMA_3	<-20dB to 2.1 GHz	<-20dB to 2.2 GHz
	Across Row	QTE_1	SMA_2	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Short Path	QTE_18	SMA_20	<-20dB to 2.1 GHz	<-20dB to 2.7 GHz
	Across Row	QTE_18	SMA_17	<-20dB to 20 GHz	<-20dB to 20 GHz

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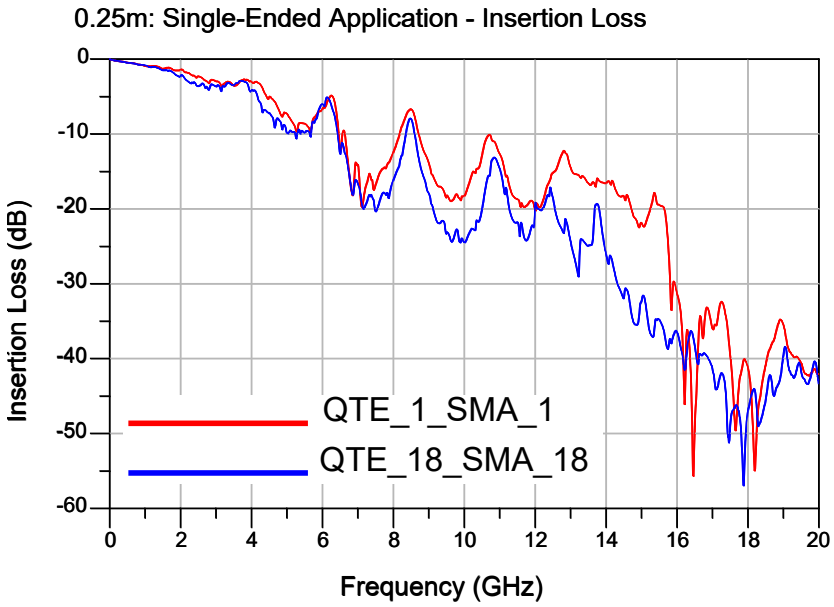
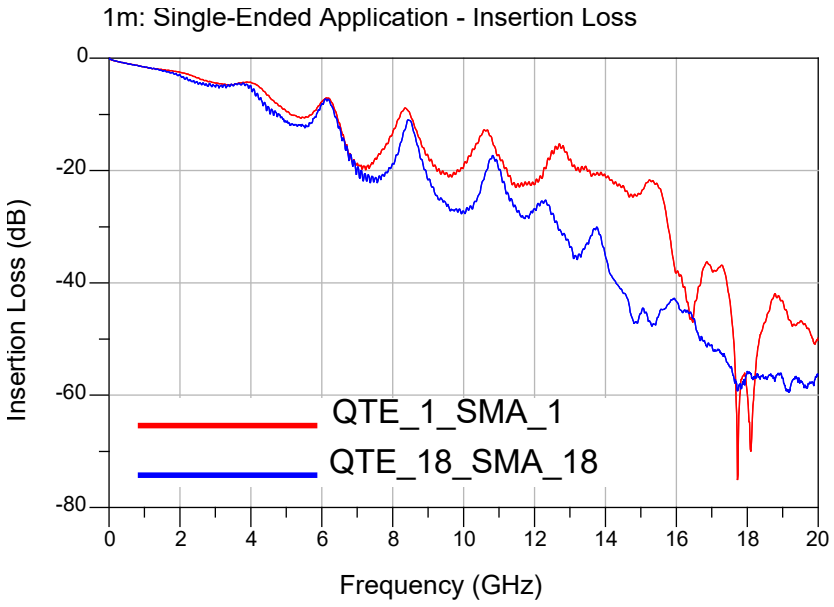
Bandwidth Chart – Single-Ended Insertion Loss





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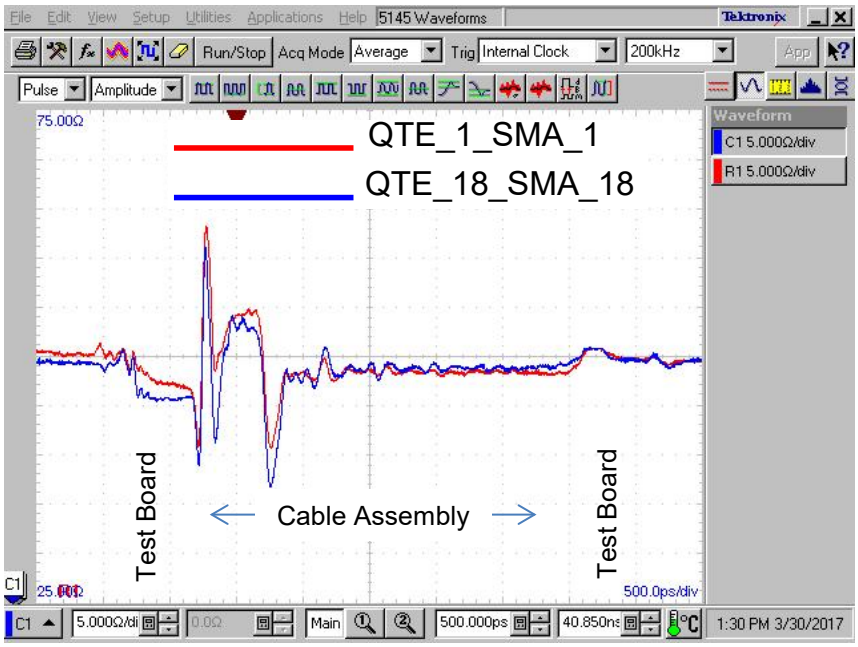
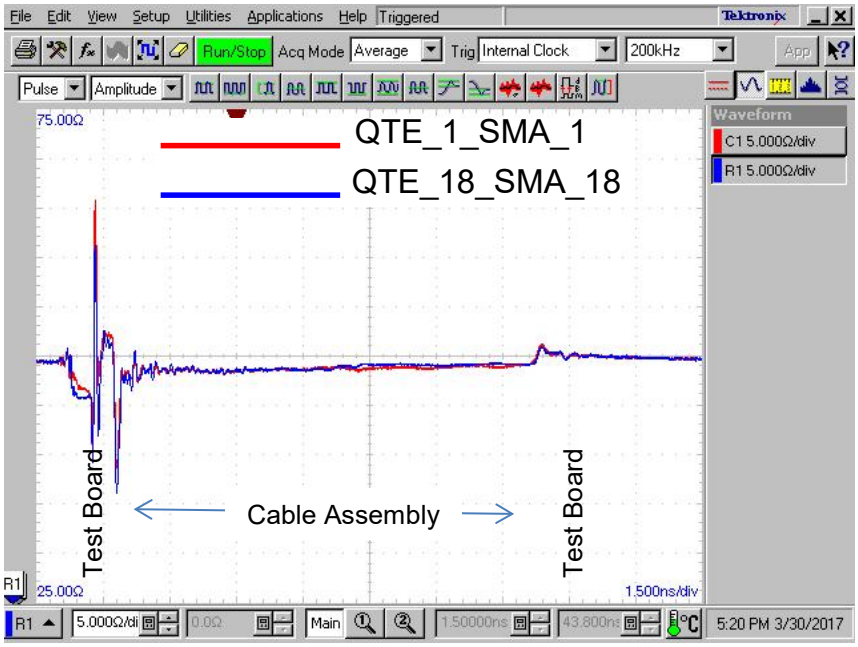
Time Domain Data Summary

0.25m: Single Ended Application _ Impedance



1m: Single Ended Application _ Impedance



Series: EQRF
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Table 4 - Propagation Delay (Cable Assembly)		
Cable length	**Driver/ Receiver**	**Driver/ Receiver**
	QTE_1/ SMA_1	QTE_18/ SMA_18
0.25m	1.508 ns	1.506 ns
1m	5.073 ns	5.095 ns

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Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "S" single-ended drive configurations.

Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this cable assembly, the following array configurations are evaluated:

Single-Ended Impedance**:**
- Long Path (furthest from test fixture)
- Short Path (closest to test fixture)

Single-Ended Crosstalk**:**
- In Row: Long Path (adjacent terminals in the long row)
- In Row: Short Path (adjacent terminals in the short row)
- Cross Row: “Xrow”: (from one row of terminals to the other row)

See Appendix C – Product and Test System Descriptions for details

Only one single-ended and one differential pair for long row and short row were driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

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Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix B of this report.

The measured S-Parameters from the network analyzer are post-processed using Agilent ADS to obtain the time domain response for signal propagation time .The Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It includes 10 mils of PCB trace on first end of the connector. Delay is measured at 30 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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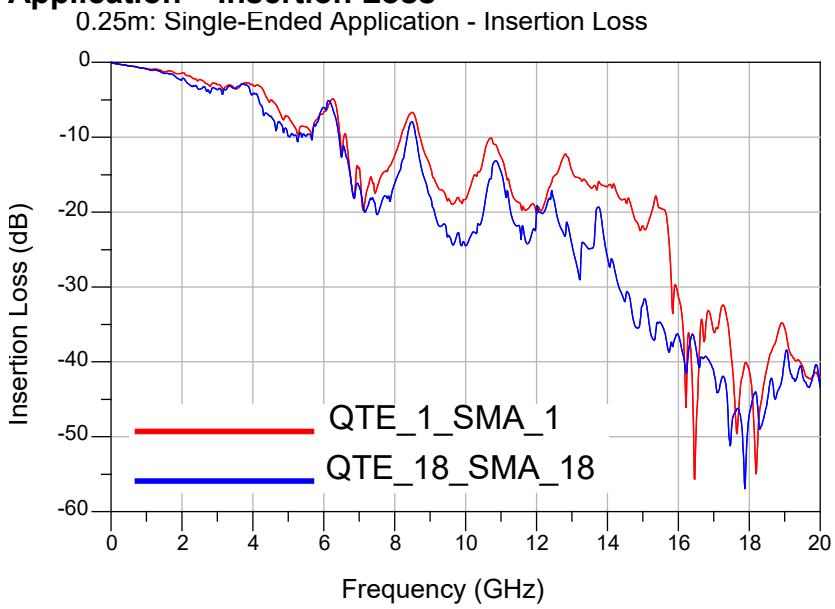
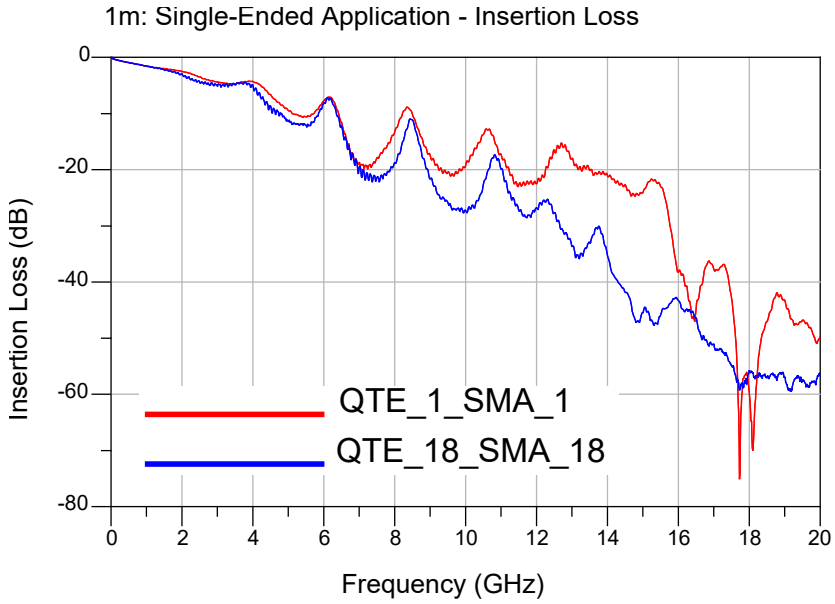
Appendix A – Frequency Domain Response Graphs

Single Ended Application – Insertion Loss





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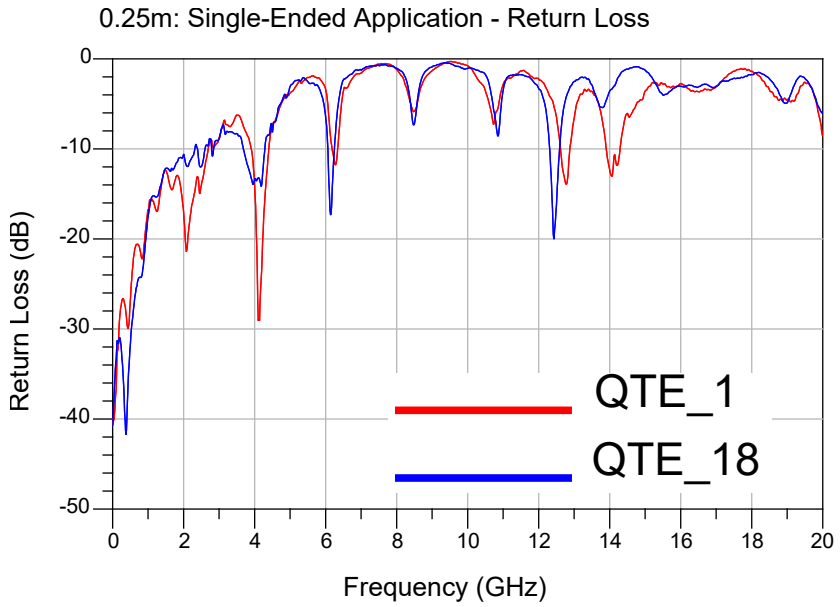
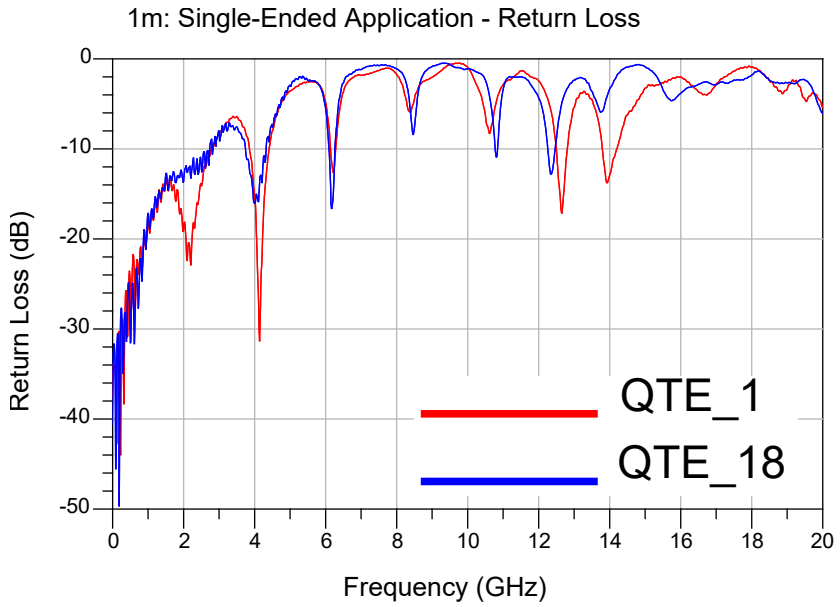
Single Ended Application – Return Loss





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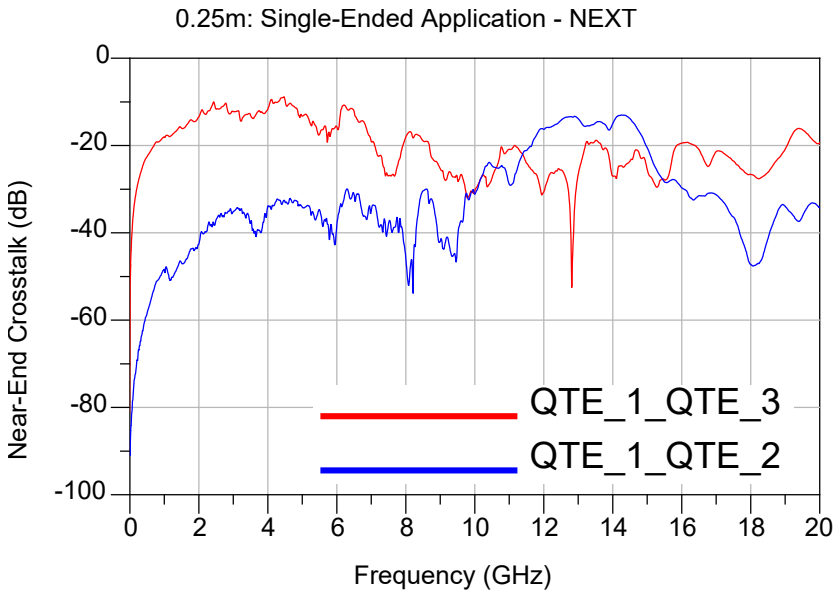
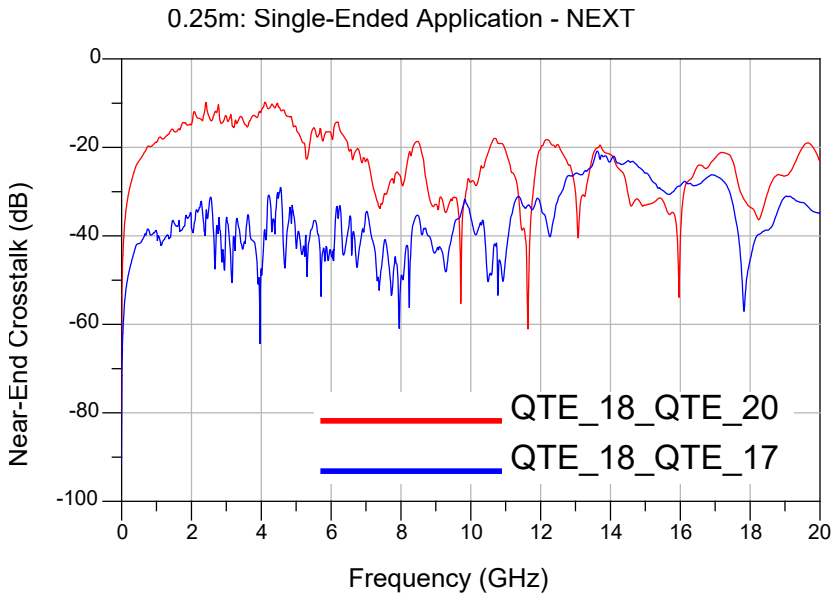
Single Ended Application – NEXT Configurations





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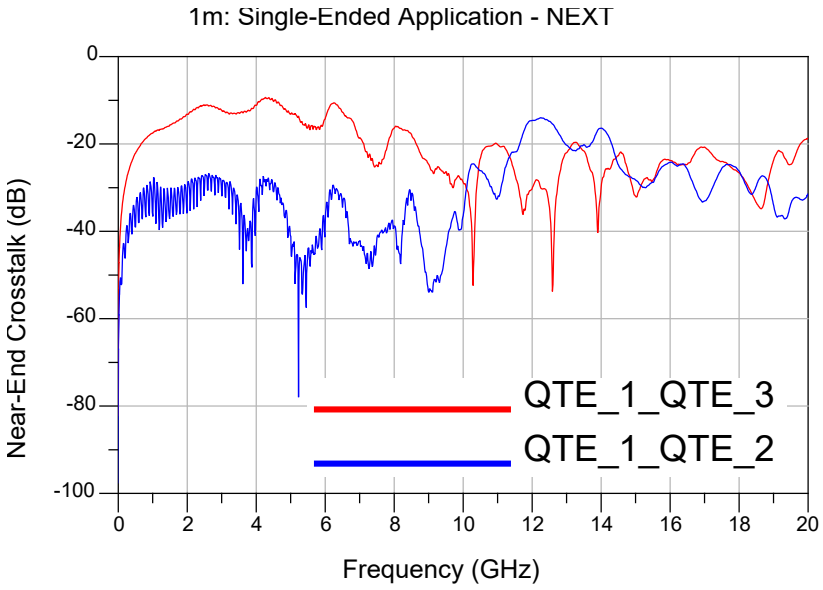

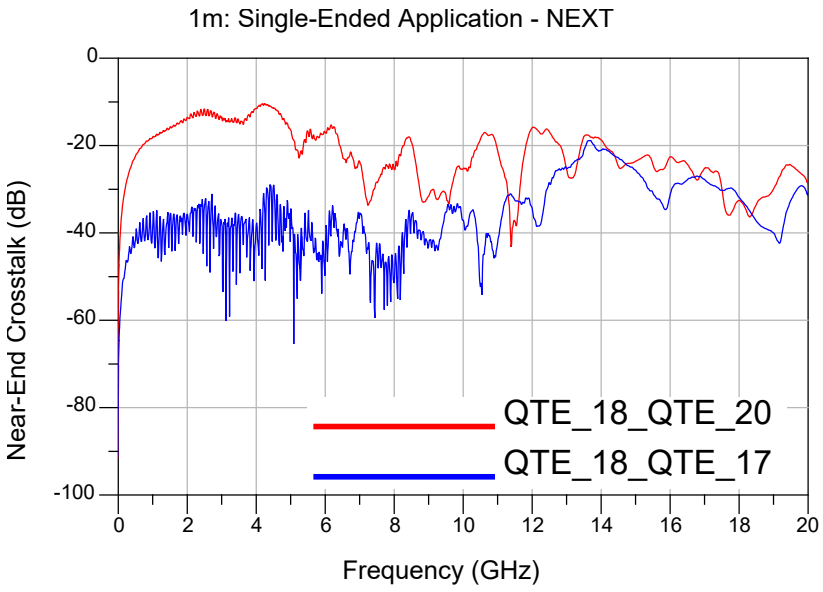

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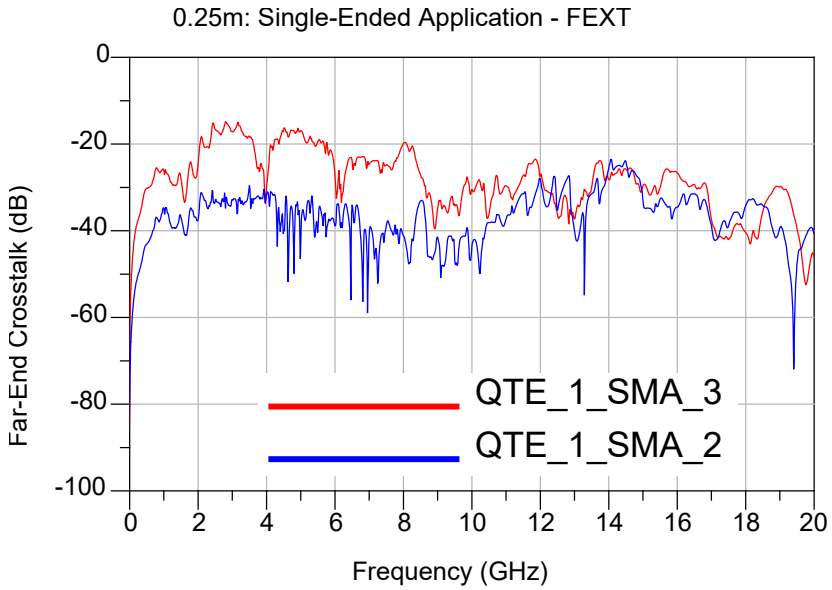
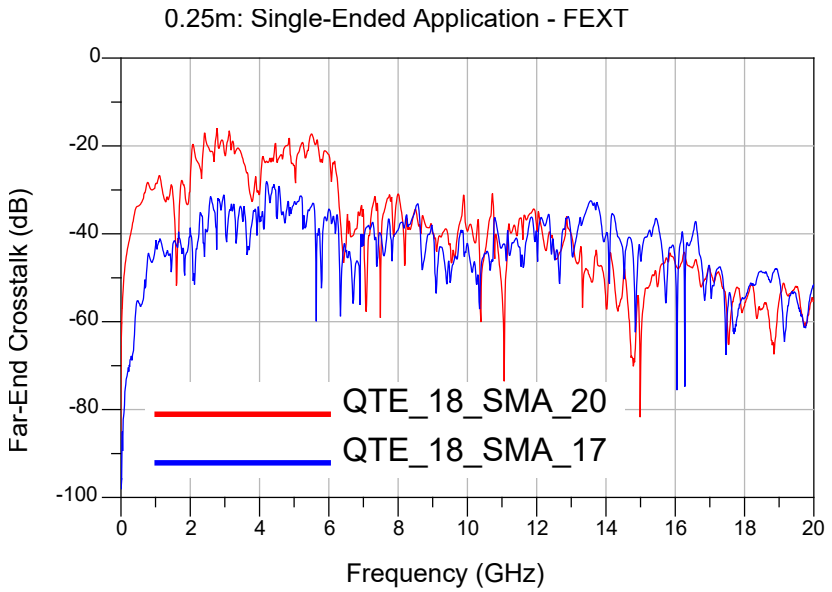
Single Ended Application – FEXT Configurations





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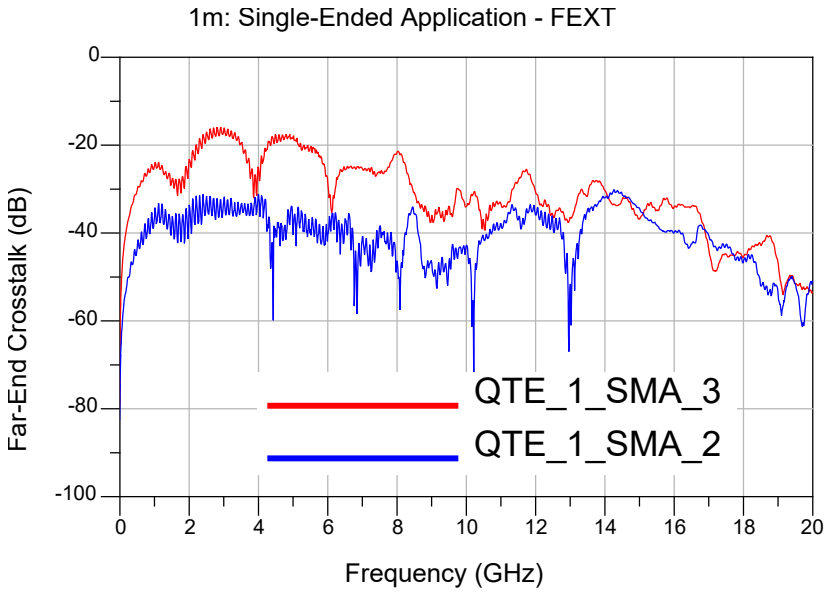

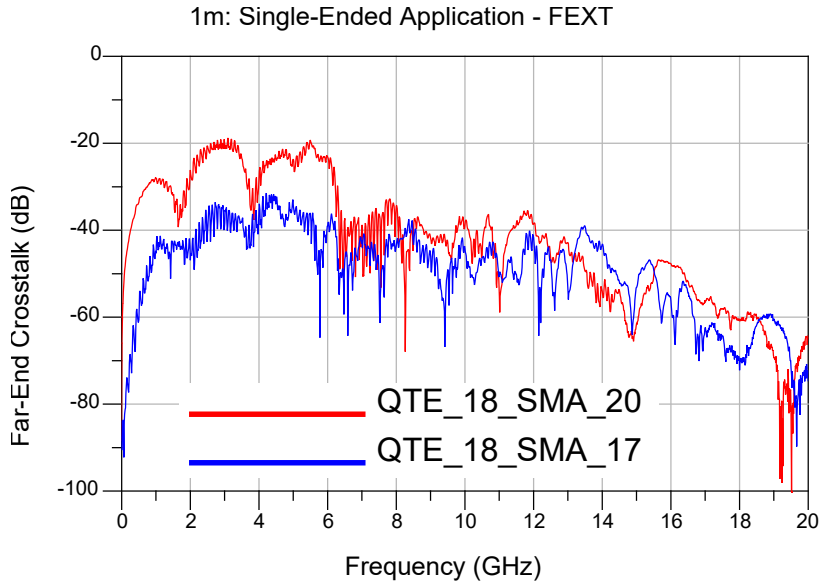

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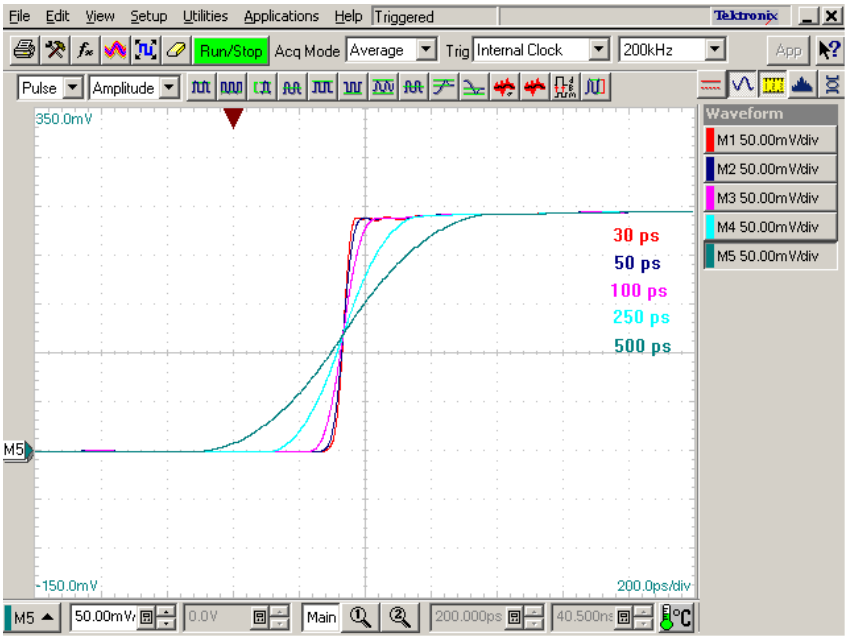
Appendix B – Time Domain Response Graphs

Single Ended Application – Input Pulse



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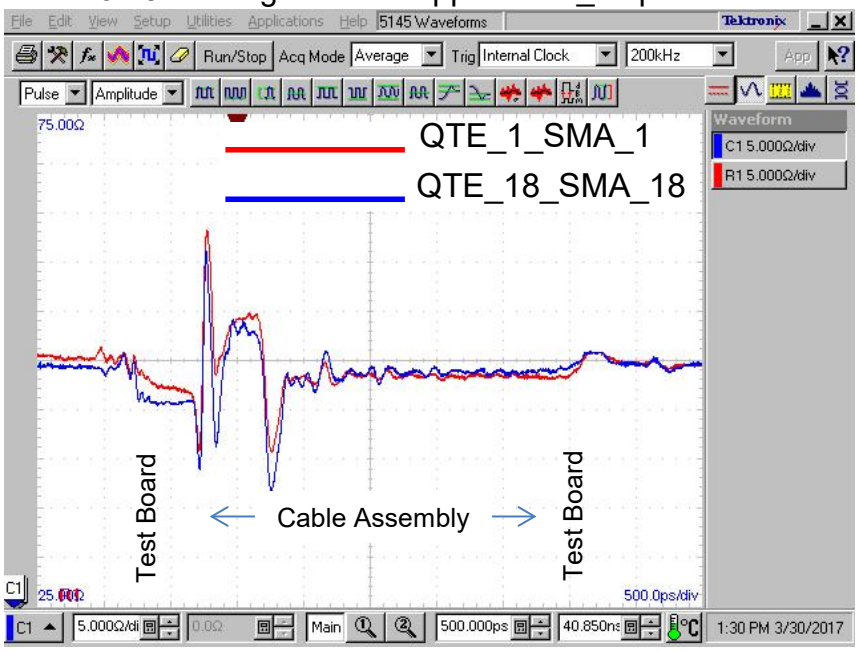
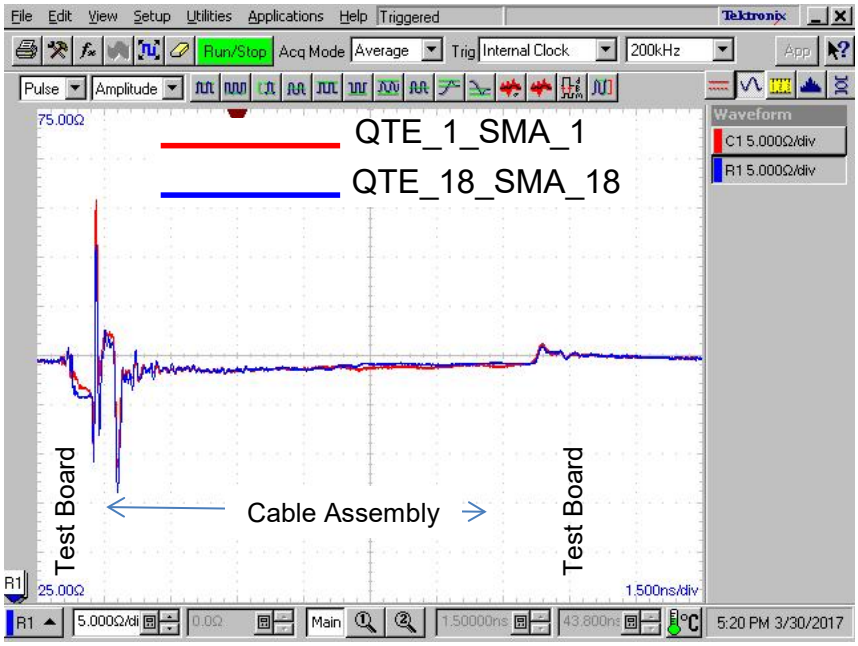
Single Ended Application – Cable Assembly Impedance

0.25m : Single Ended Application _ Impedance



1m : Single Ended Application _ Impedance



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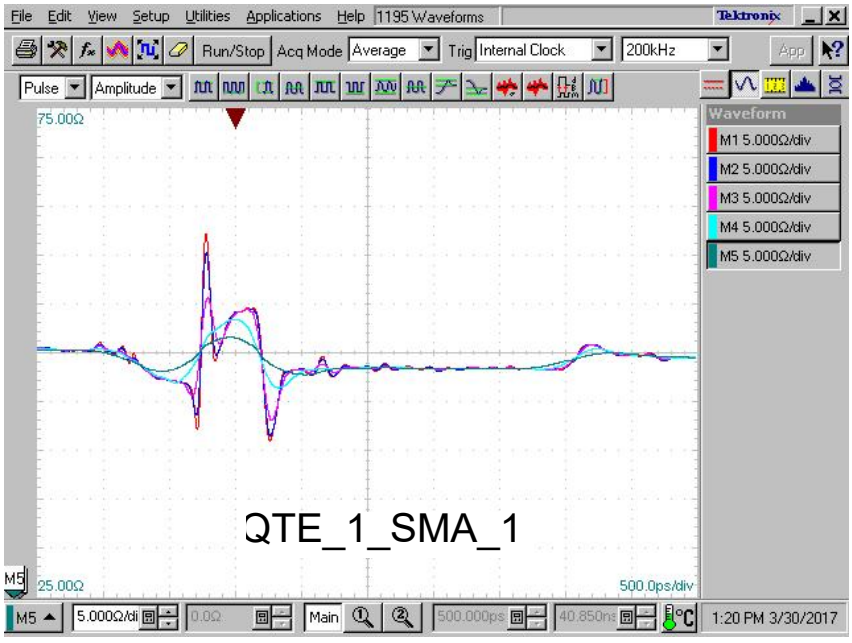

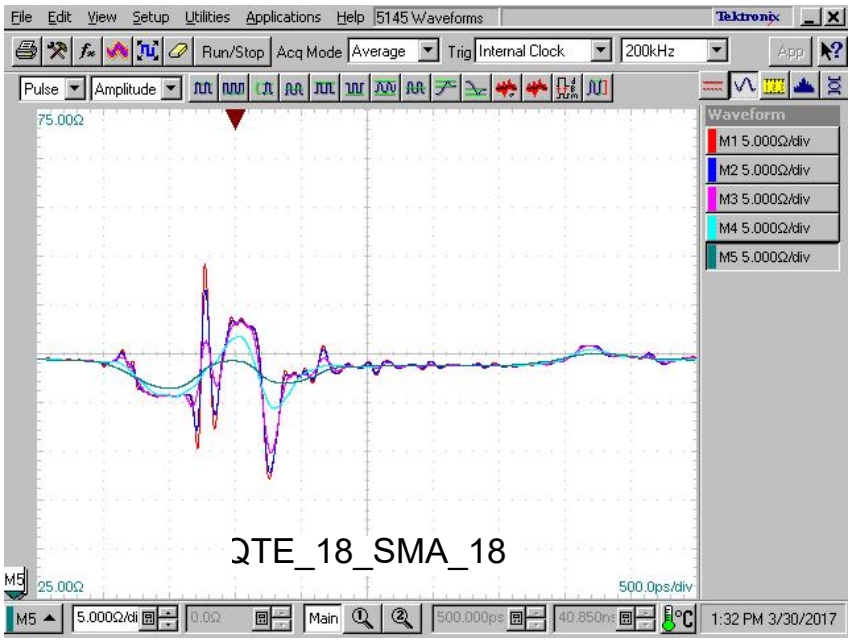

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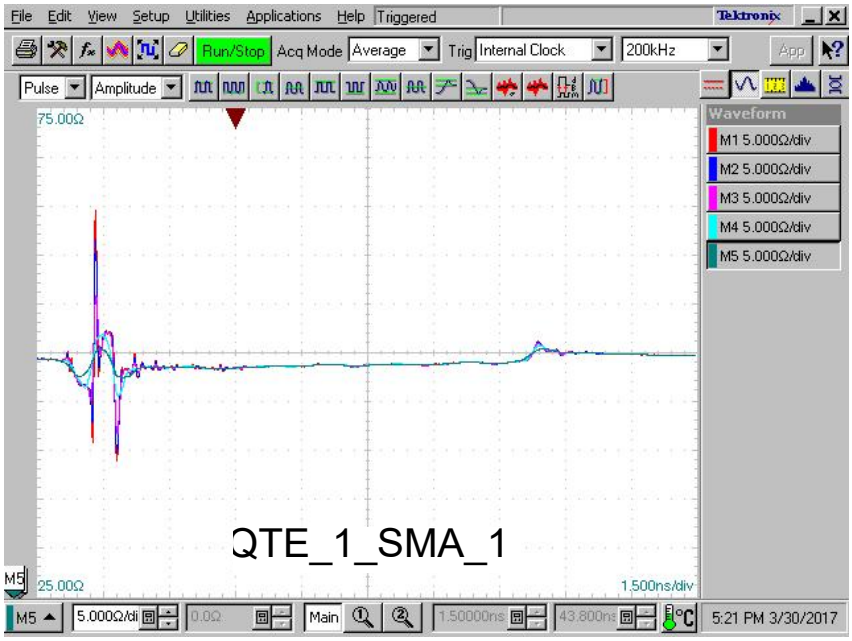
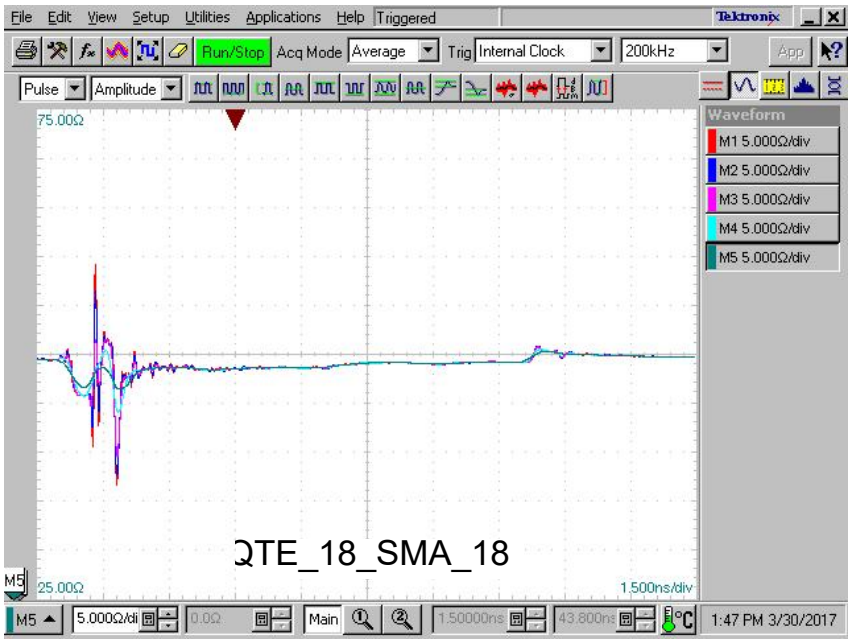
EQRF-020-1000-T-L-SMA-P-1





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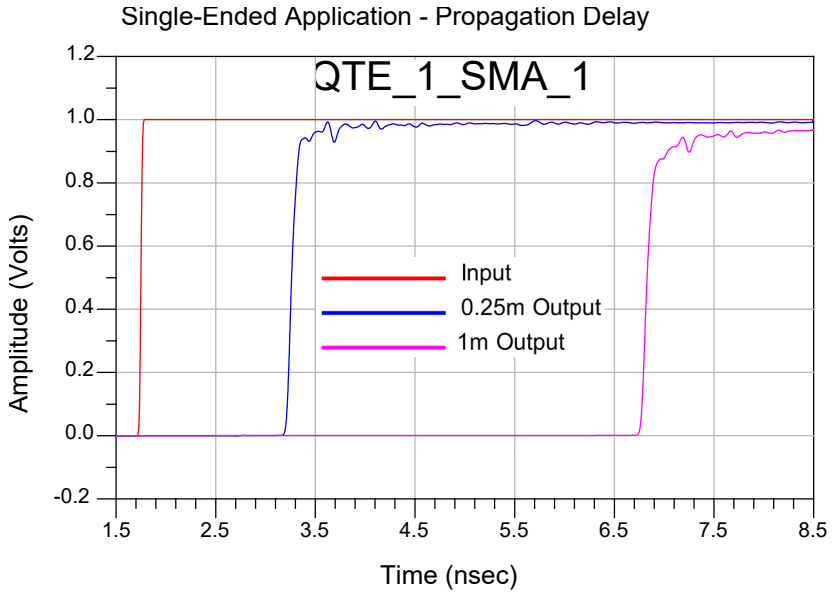
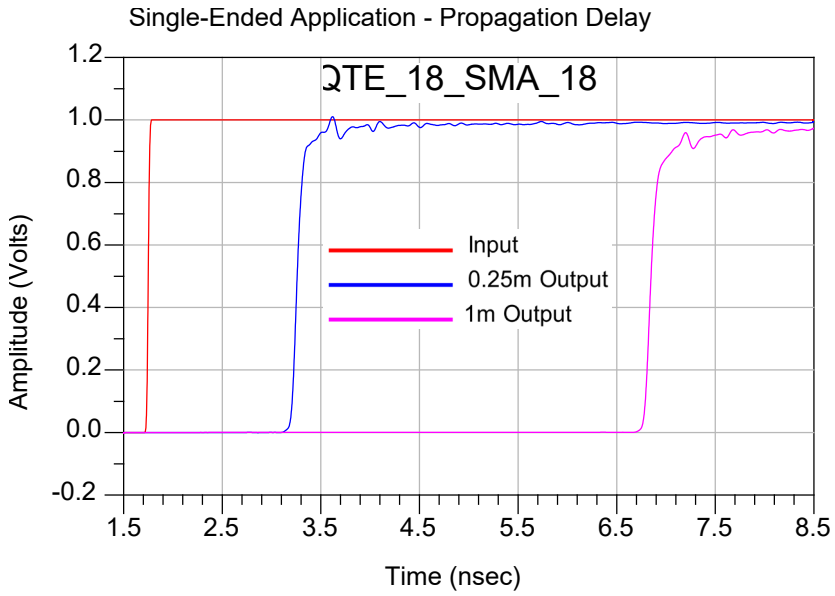
Single Ended Application – Propagation Delay





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Appendix C – Product and Test System Descriptions

Product Description

Product test samples are 0.80 mm High Speed ribbon coax cable assemblies. The part number are EQRF-020-0250-T-L-SMA-P-1and EQRF-020-1000-T-L-SMA-P-1, they mate with QSE-xxx-01-x-D-A and SMA-50. A photo of the mated test article mounted to SI test boards is shown below.

The coax cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in table below. There are a total of 20 positions per row. SMA jack numbers on the test boards correspond to the assembly line numbers. All adjacent lines are terminated where applicable.

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40
GROUND																			
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39

Table 5: Respective signal line numbers

Test System Description

The test fixtures are composed of four-layer FR-406 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Two test fixture specific to the EQRF series cable assembly identified by part PCB-107701-SIG-01A and PCB-107701-SIG-02A. The Auto Fixture Removal (AFR) calibration structures designed specifically for the EQRF series are on the same test fixture. Displayed on the following pages is information for the EQRF/AFR calibration structure and directives for mating EQRF fixtures.

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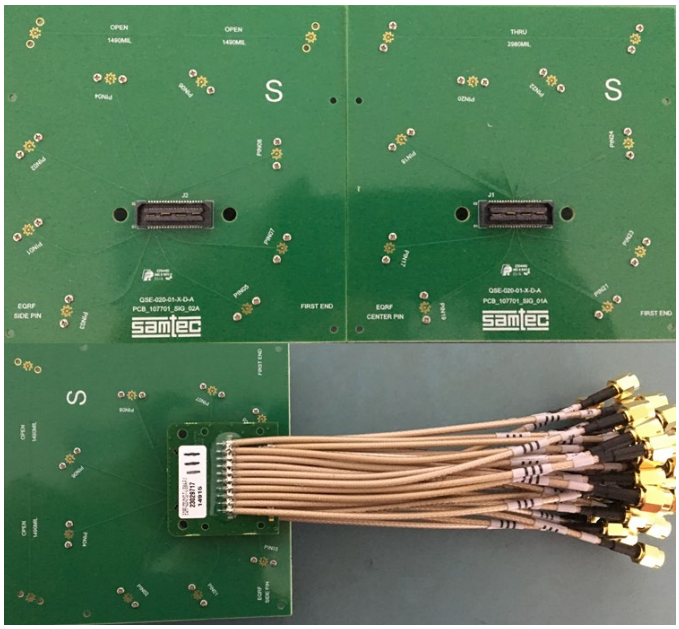
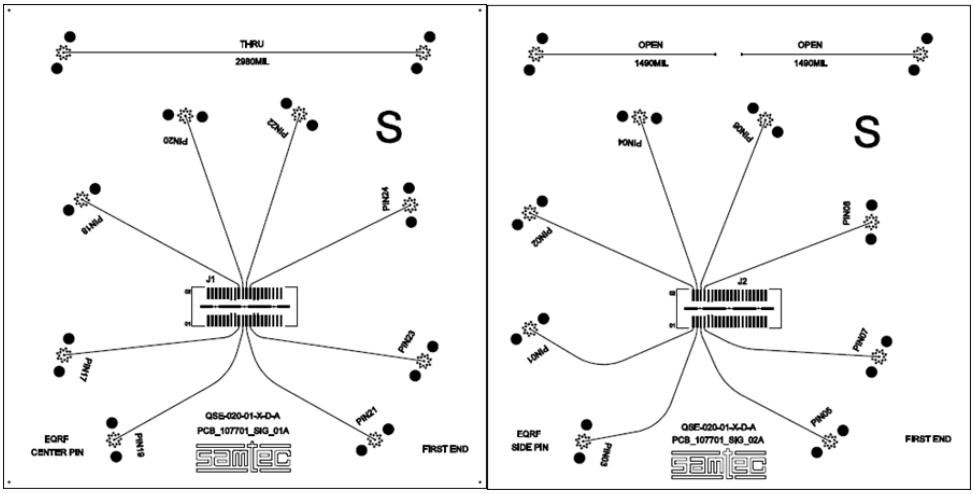
PCB-107701-SIG-XX Test Fixtures



Artwork of the PCB design is shown below.



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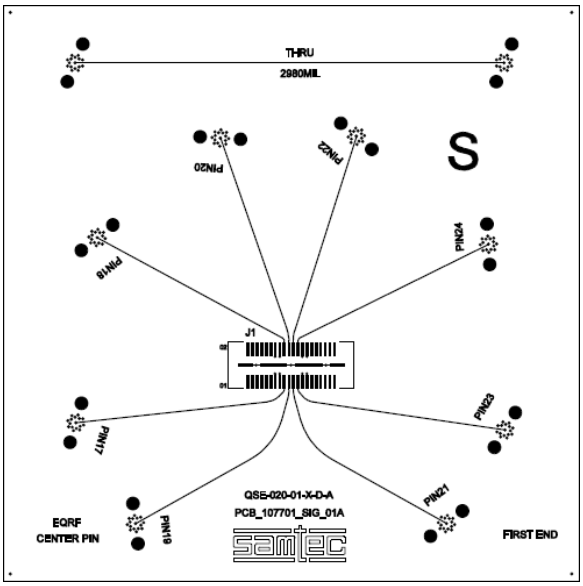
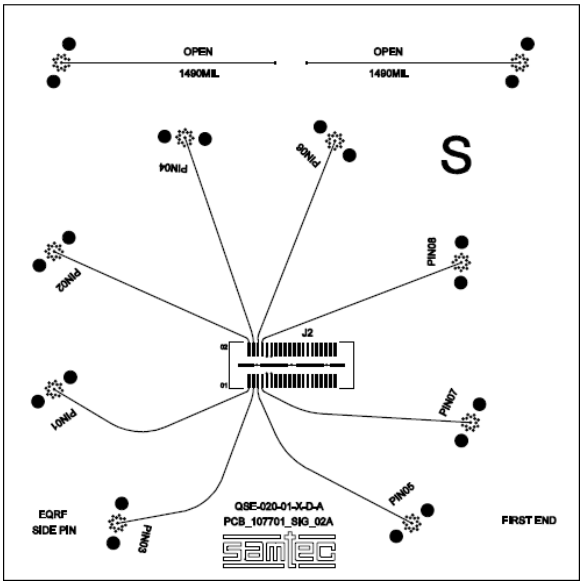
PCB Fixtures

The test fixtures used are as follows:





PCB-107701-SIG-01A – QSE for First End Center Pin
PCB-107701-SIG-02A – QSE for First End Side Pin

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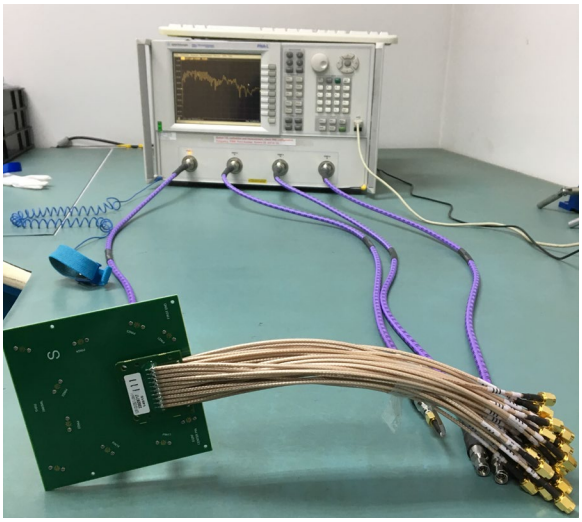
Appendix D – Test and Measurement Setup

The test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz	Number of points -1601
Stop Frequency – 20 GHz	IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

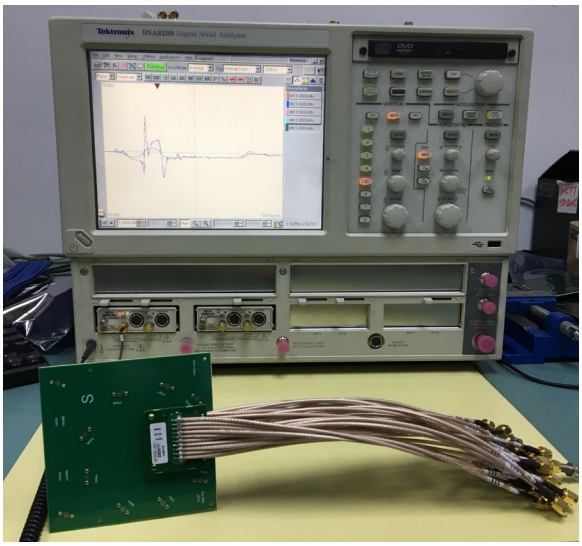
QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

Series: EQRF
Description: 0.80 mm Q Strip® High-Speed Combination RF Coax Cable Assembly

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale: 5 ohm / Div
Offset: Default / Scroll
Horizontal Scale: 500ps/ Div
Record Length: 4000
Averages: ≥ 16

DSA8200 Measurement Setup



Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: EQRF
Description: 0.80 mm Q Strip® High-Speed Combination RF Coax Cable Assembly

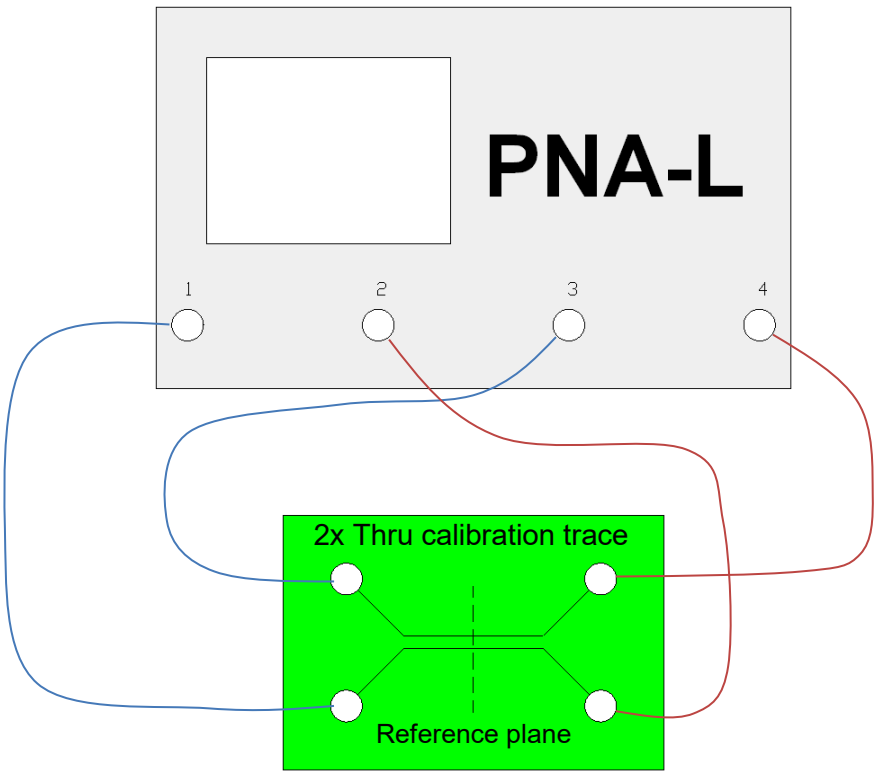
Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-cal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the EQRF test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.



Series: EQRF
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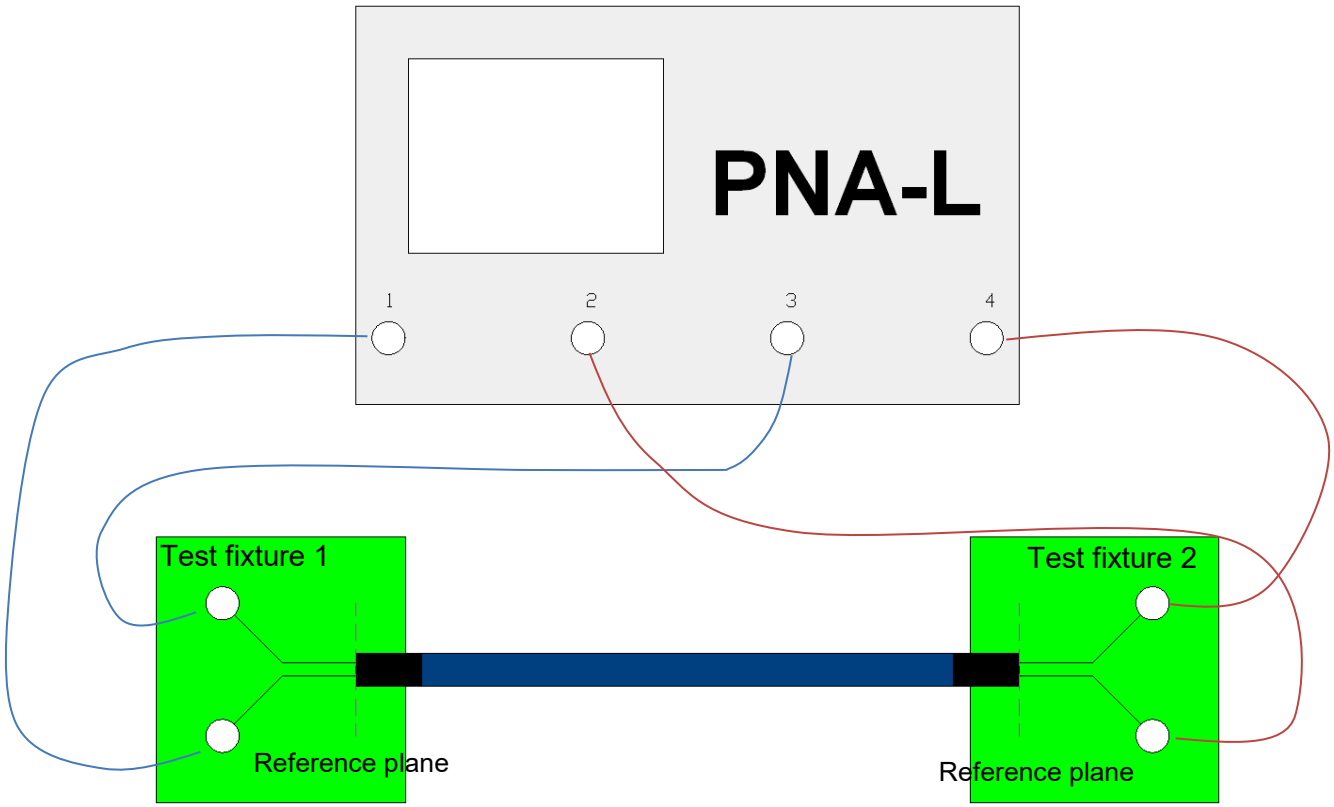
Measurements are then performed using the test boards as shown below. The test board effects are removed in post-processing via AFR in Agilent PLTS. The calibrated reference plane is located from the edge of connector footprint on each side. The S-Parameter measurements include:

A. Test board pads (footprint effects) for the QSE connector
B. The QSE series connector J1
C. The EQRF-020-XX-T-L-SMA-P-1test cable
D. The SMA Plug series connector J2

The figure below shows the location of the measurement reference plane.



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Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with band-width-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Impedance (TDR)
Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

Series: EQRF
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Appendix F – Glossary of Terms

ADS – Agilent Advanced Design System
AFR – Automatic Fixture Removal
CTLE – Continuous Time Linear Analyzer
DUT – Device under test
FD – Frequency domain
FEXT – Far-End Crosstalk
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PLTS – Agilent Physical Layer Design System
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
UI – Unit Interval
XROW – Across Row
Z – Impedance (expressed in ohms)