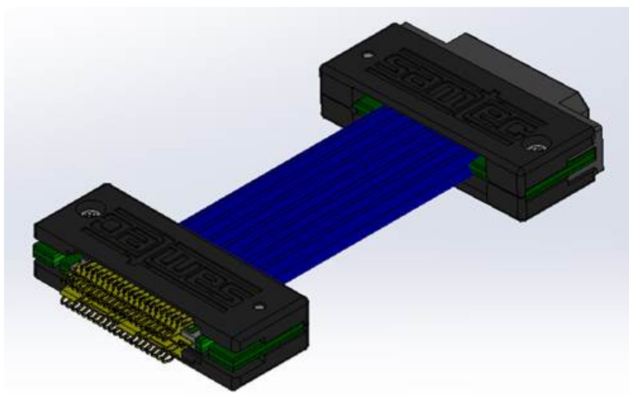
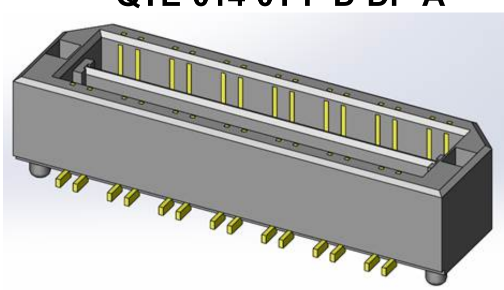
High Speed Characterization Report

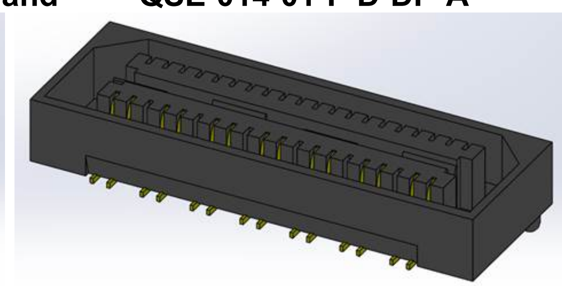
EQDP-014-XX.XX-TEU-SEU-5



Mated with:

QTE-014-01-F-D-DP-A and **QSE-014-01-F-D-DP-A**





Description:

0.80 mm Q Pairs® High Speed Cable Assembly

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Report Revision: 09/06/2018

Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

Table of Contents

Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

Cable Assembly Overview

The 0.8 mm (.0315") EQDP Cable Assembly is constructed using 30 AWG twinax ribbon cable. It is double row system up to 112 pins. The EQDP series cable assemblies are available in 14, 28, 42 and 56 positions per row and 43.7 mm (1.72") length minimum. The data in this report is only applicable to 250 mm, 500 mm and 1000 mm length cable assembly.

The test sample consists of two micro twinax ribbon cables that contain 7 differential pairs each. The cables are terminated by soldering a small transition PCB (termination board) at each end. The termination board has a connector soldered to it. The cable assemblies tested for this report are terminated with a QTE-DP-EM shrouded header at end 1 and a QSE-DP-EM high-speed socket at end 2. The cable assembly is wired to facilitate a Pin 1 to Pin 1 mapping between the cable terminations.

The EQDP cable assemblies were tested by mating to a QSE-DP socket at End 1 and to a QTE-DP header at End 2. One sample of each length assembly was tested. The actual part numbers that were tested are shown in Table 1, which also identifies End 1 and End 2 of each assembly. A relative sample picture is shown in Figure1.

Two differential pairs, the longest physical signal path (Long Path) and the shortest physical signal path (Short Path), of each assembly type were tested. The Long Path and Short Path are identified as, TEU_25,27 to SEU_25,27 and TEU_18,20 to SEU_18,20, respectively.

Length	Part Number	End 1	End 2
250 mm	EQDP-014-09.80-TEU-SEU-5	TEU	SEU
500 mm	EQDP-014-19.68-TEU-SEU-5	TEU	SEU
1000 mm	EQDP-014-39.37-TEU-SEU-5	TEU	SEU

Table 1: Sample Description

Figure 1: Test Sample

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520 Park East Blvd.
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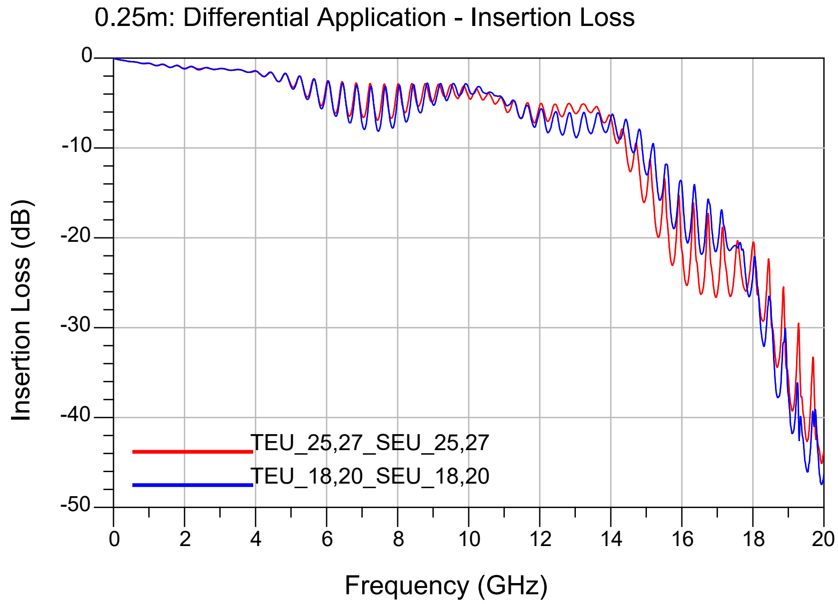
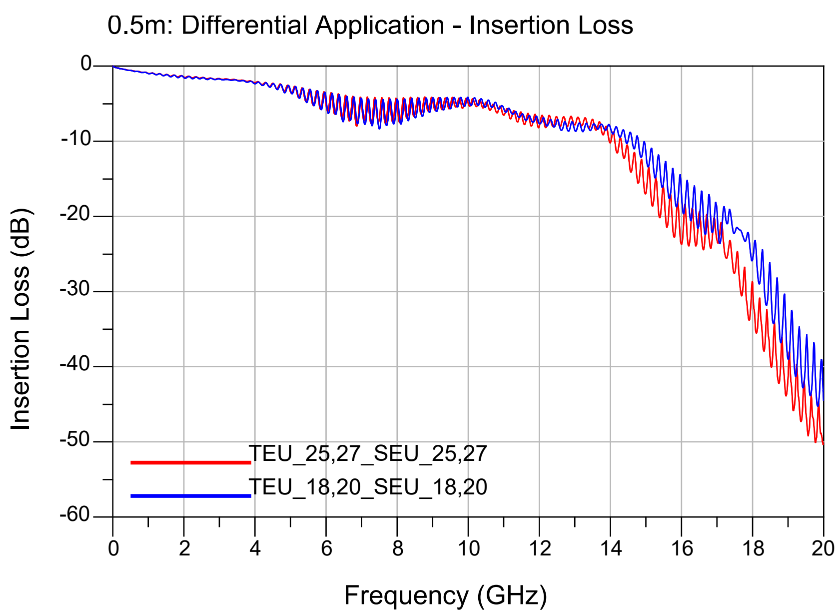
Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

Frequency Domain Data Summary

Bandwidth Chart – Differential Insertion Loss





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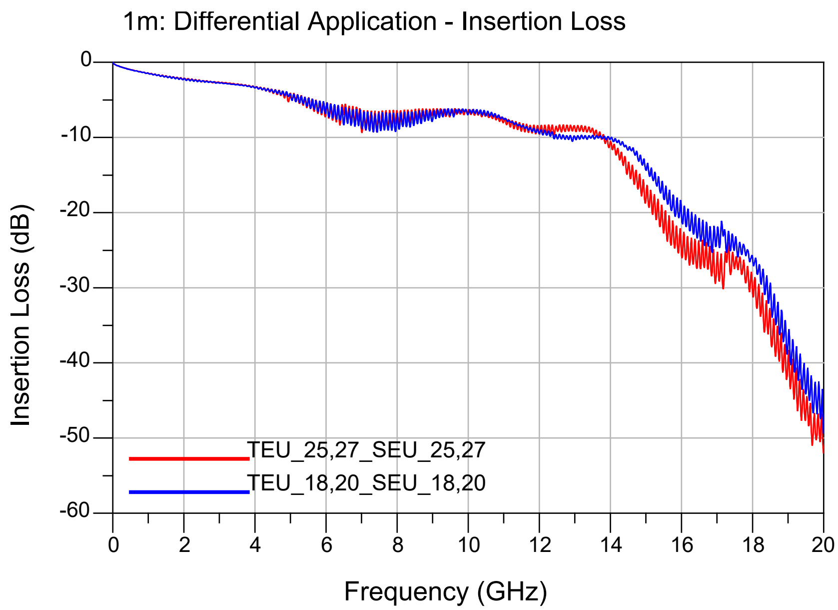

Series: EQDP
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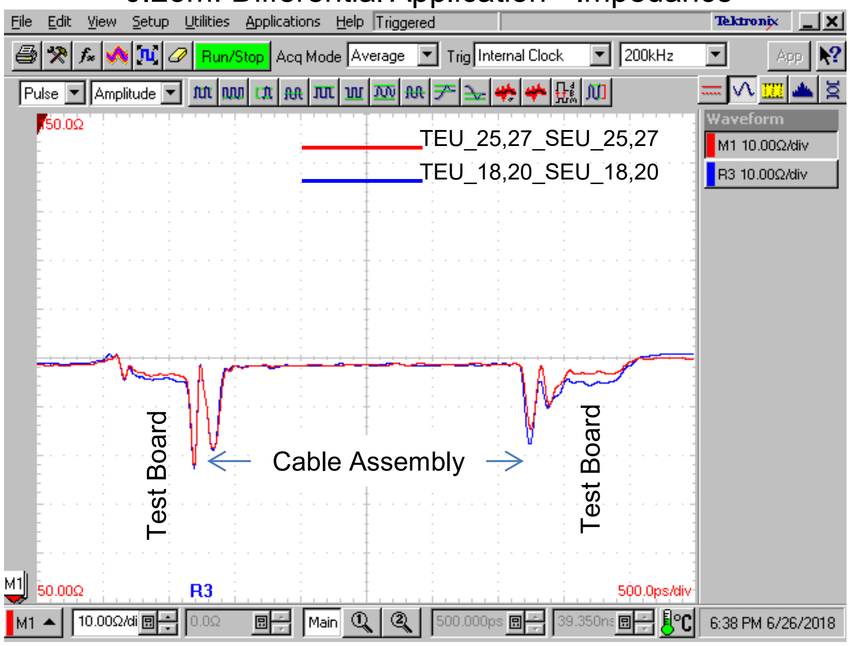
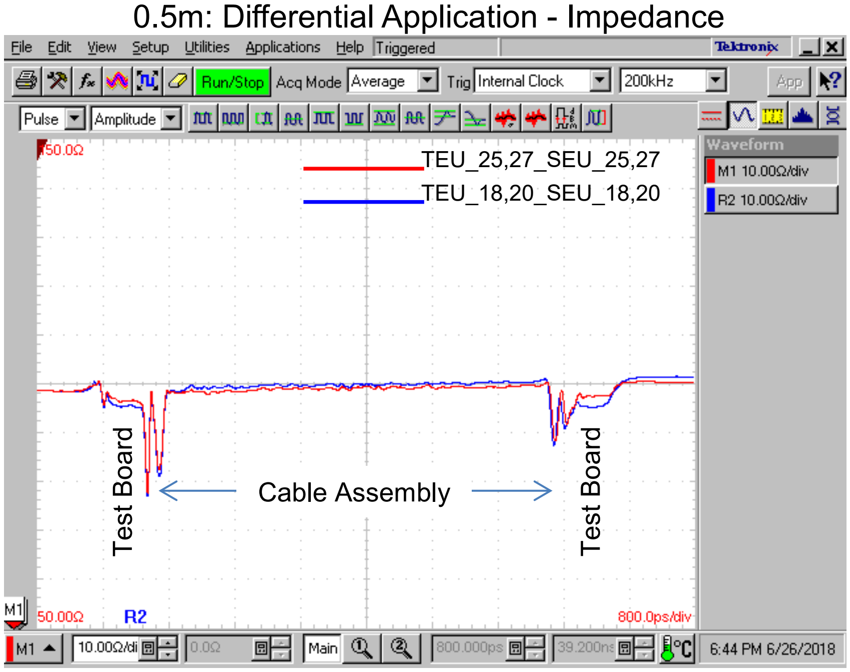
Time Domain Data Summary

0.25m: Differential Application - Impedance



0.5m: Differential Application - Impedance



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1m: Differential Application - Impedance

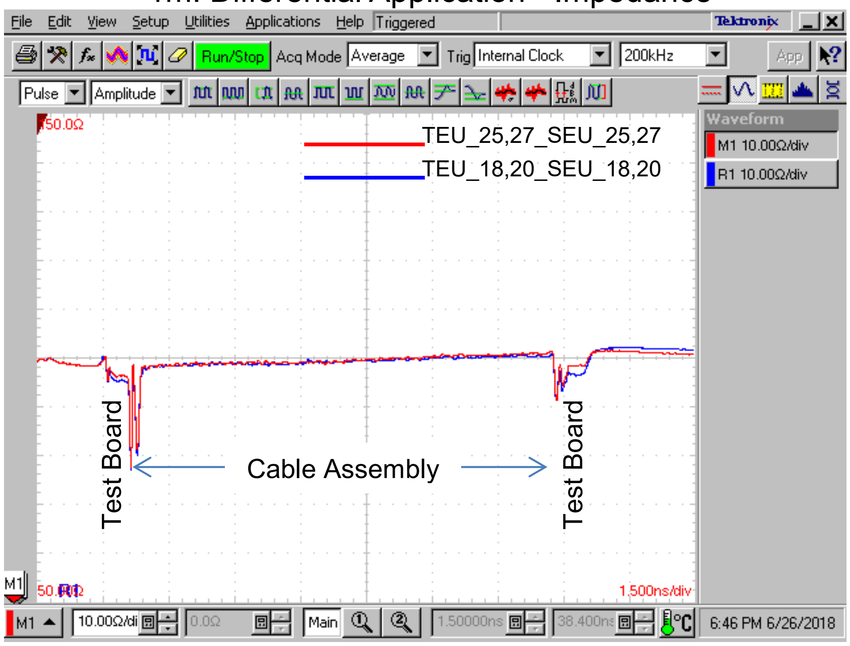

Table 2 - Propagation Delay (Cable Assembly)		
Cable length	**Driver/ Receiver**	**Driver/ Receiver**
	TEU_25,27 / SEU_25,27	TEU_18,20 / SEU_18,20
0.25m	1.363ns	1.361ns
0.5m	2.565ns	2.555ns
1m	4.939ns	4.934ns

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Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GSSG" differential drive configuration only.

Cable Assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this cable assembly, the following array configurations are evaluated:

Differential Impedance**:**
- Long Path (furthest from test fixture)
- Short Path (closest to test fixture)

Differential Crosstalk**:**
- In Row: Long Path (adjacent terminals in the long row)
- In Row: Short Path (adjacent terminals in the short row)
- Across Row: "Xrow": (from one row of terminals to the other row)

See Appendix C – Product and Test System Descriptions for details

Only one differential signal was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals might be encountered as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or the rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate the worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

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Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length and signal propagation time in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix B of this report.

The measured S-Parameters from the network analyzer are post-processed using Keysight ADS to obtain the time domain response for signal propagation time. The Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 10 mils of PCB trace on each connector side. Delay is measured at 100 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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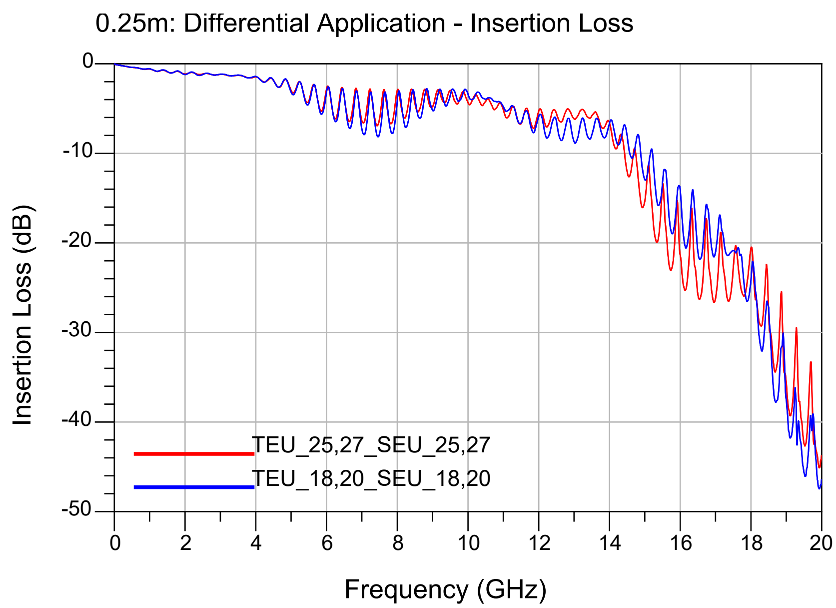
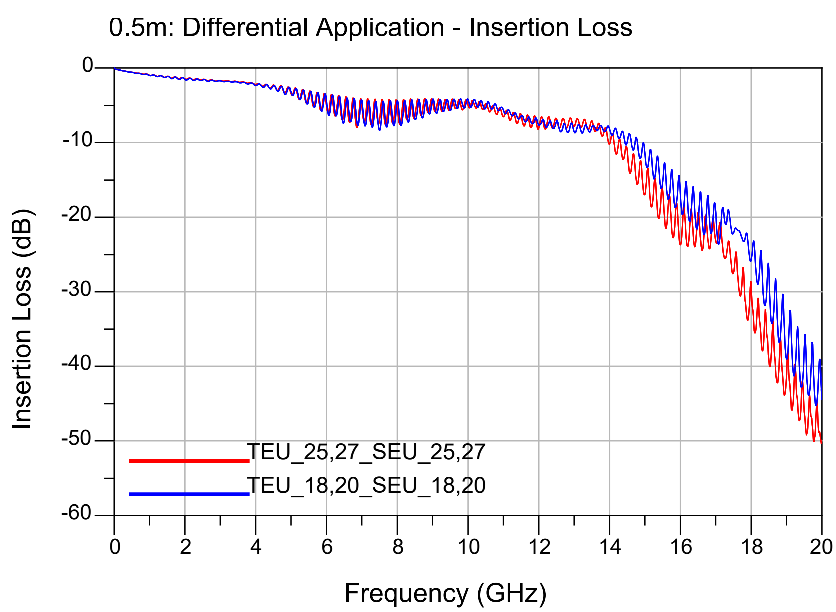
Appendix A – Frequency Domain Response Graphs

Differential Application – Insertion Loss





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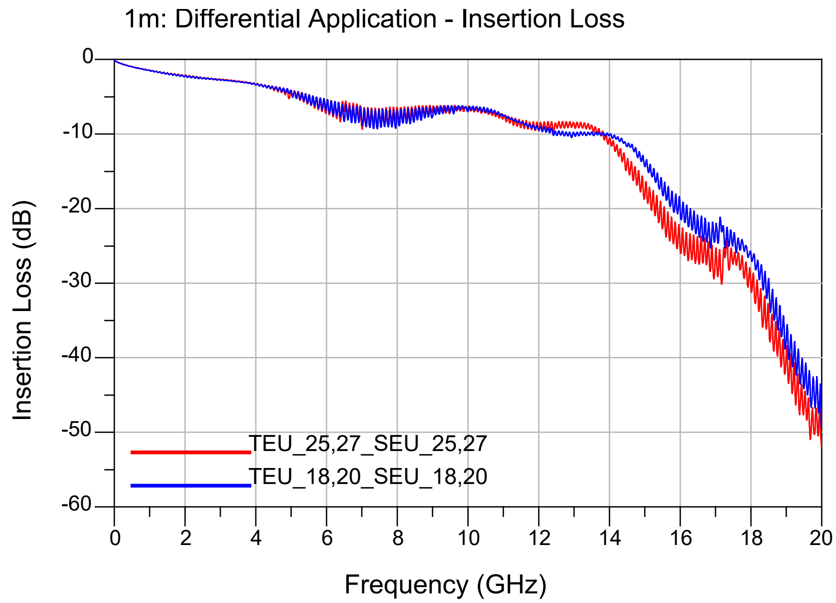
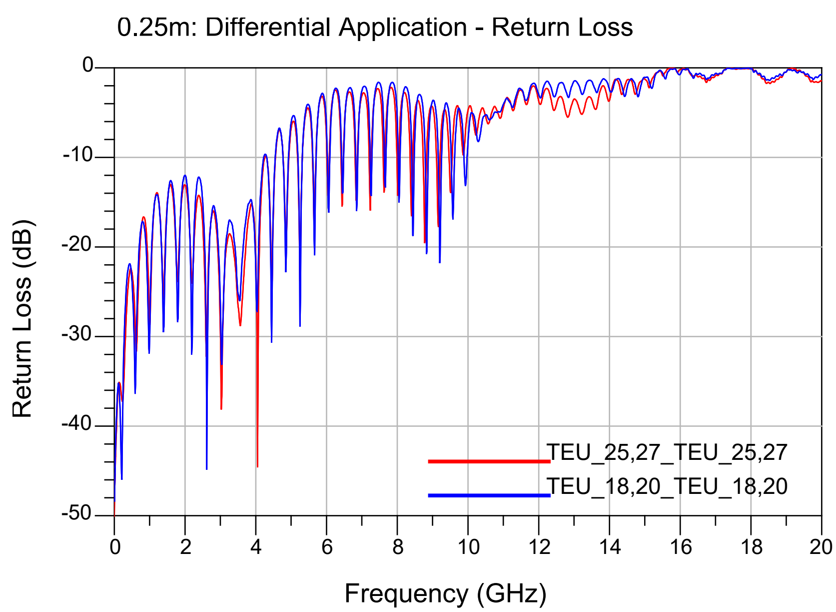


Differential Application – Return Loss



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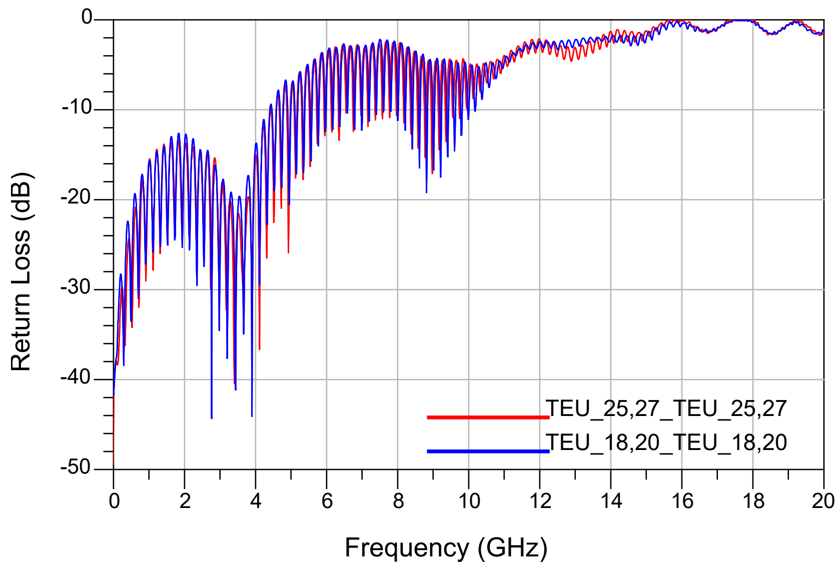
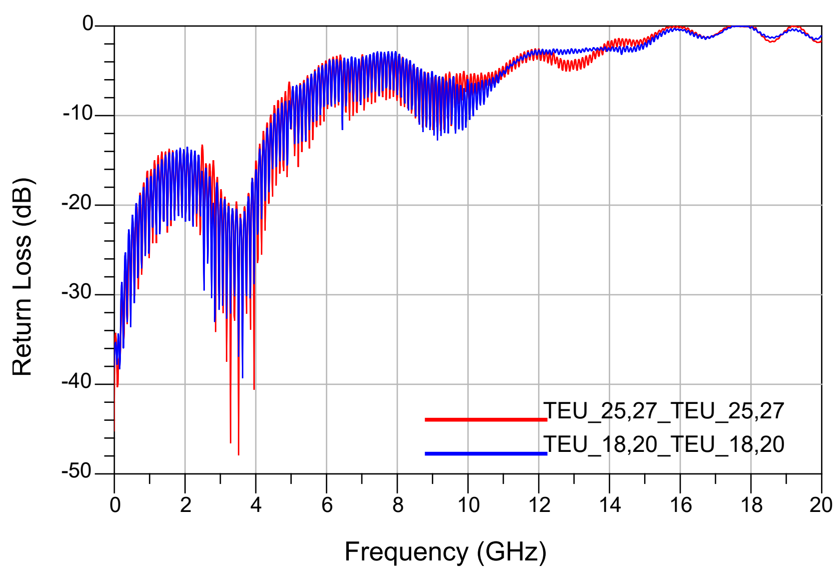
0.5m: Differential Application - Return Loss



1m: Differential Application - Return Loss



Series: EQDP
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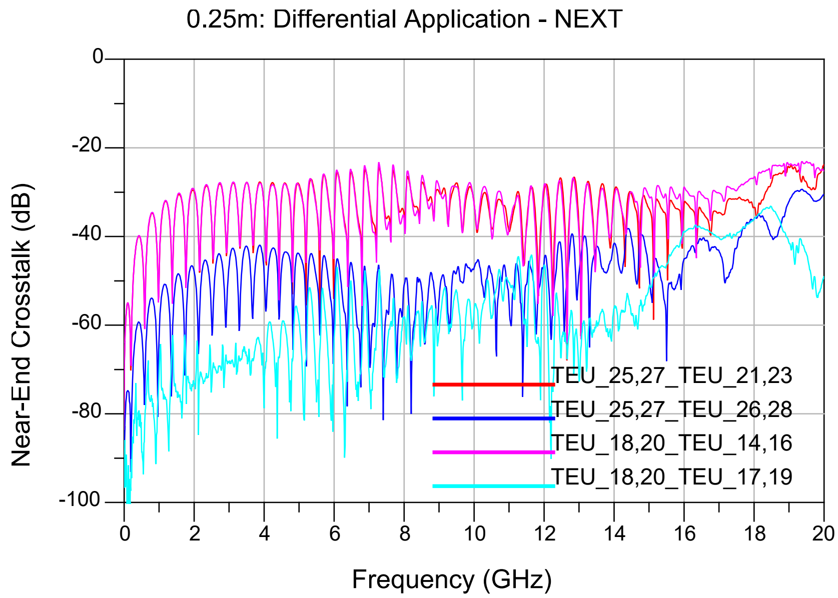
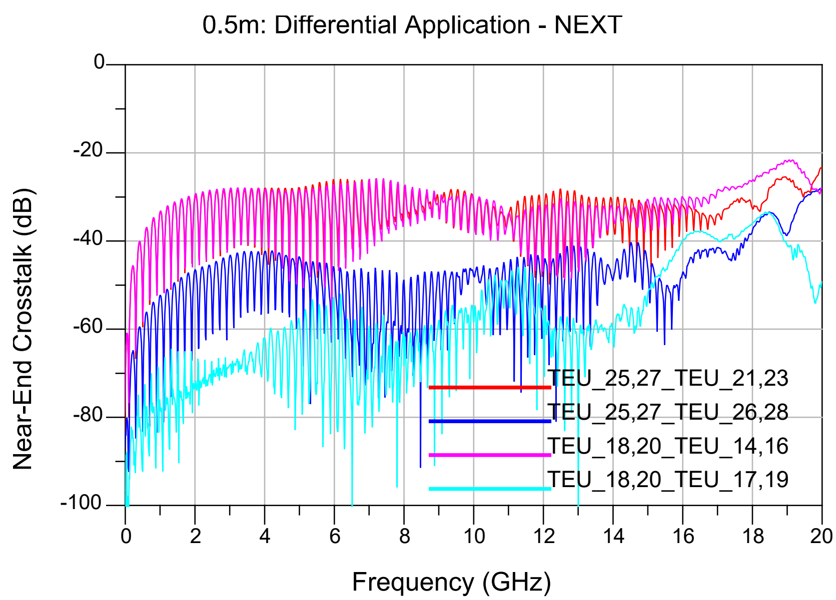
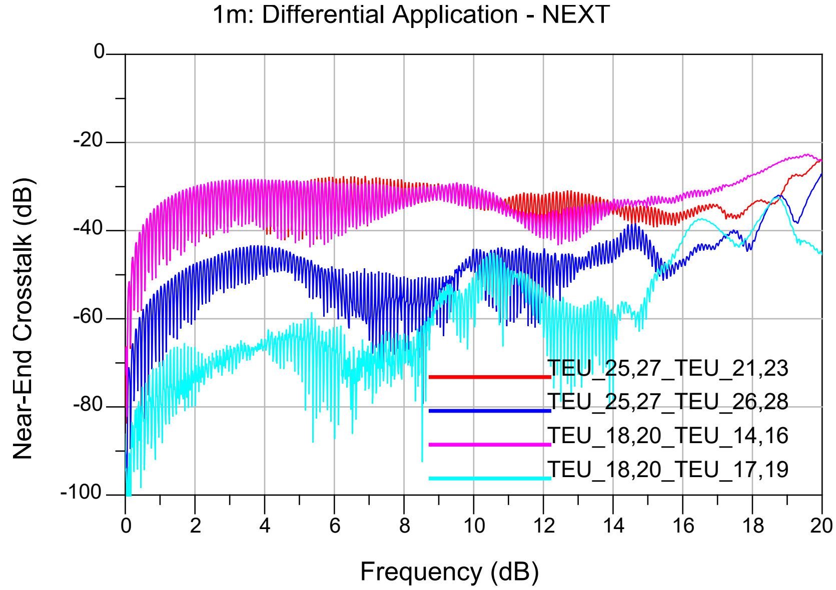
Differential Application – NEXT Configurations

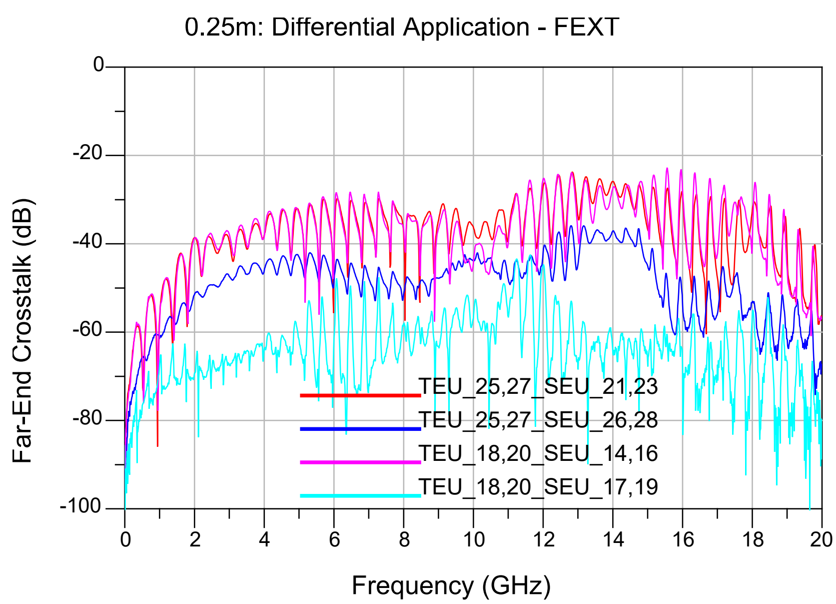




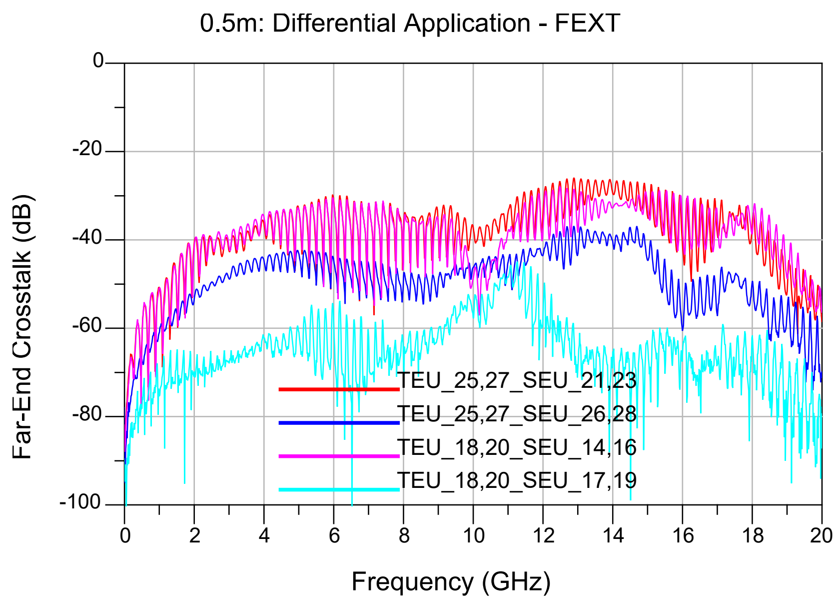
Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

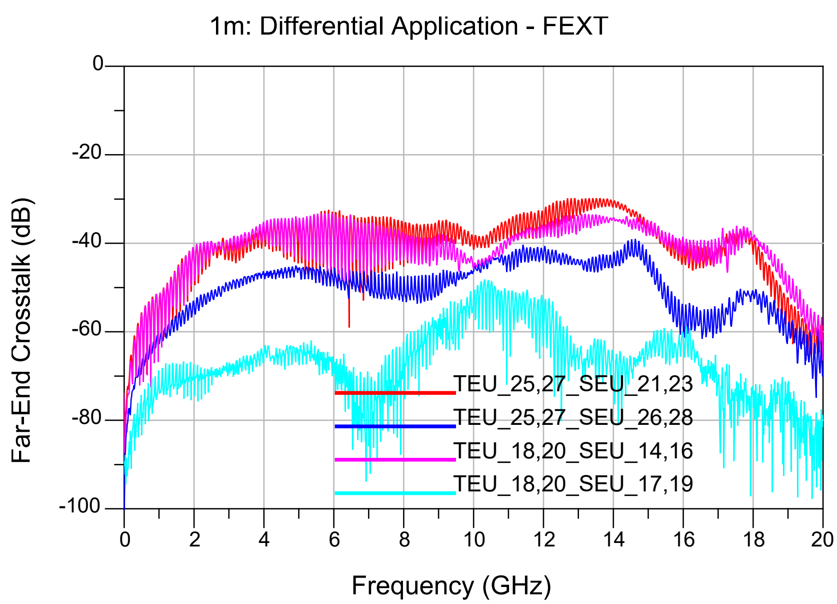


Differential Application – FEXT Configurations



Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

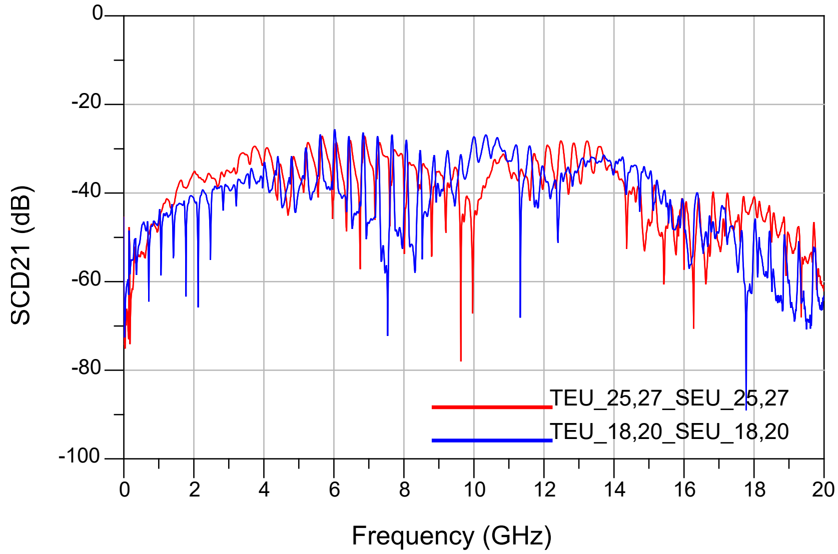




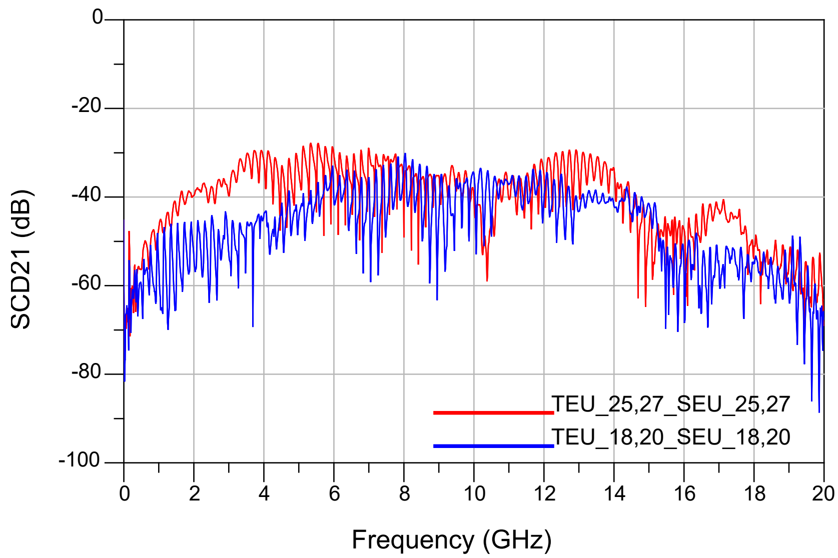
Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

Differential Application – Differential to Common Mode Conversion

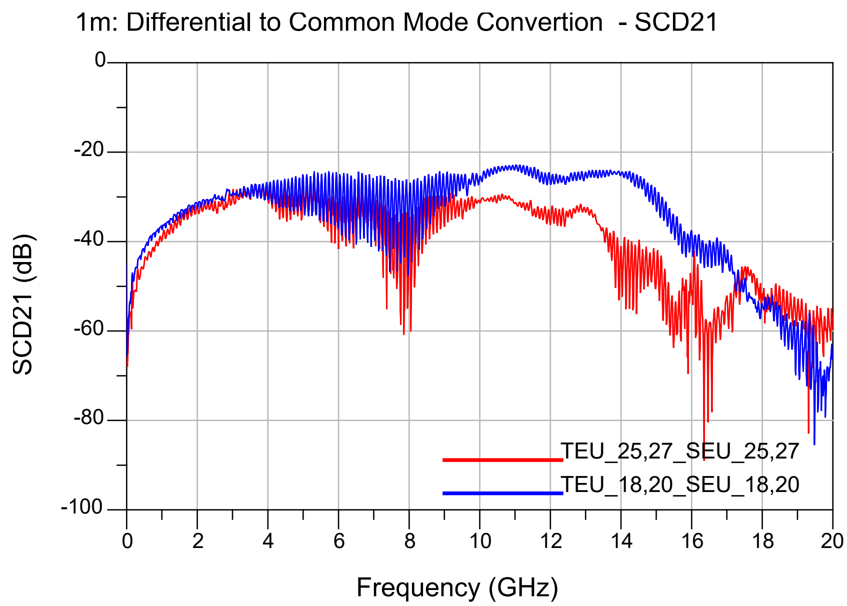
0.25m: Differential to Common Mode Convertion - SCD21



0.5m: Differential to Common Mode Convertion - SCD21



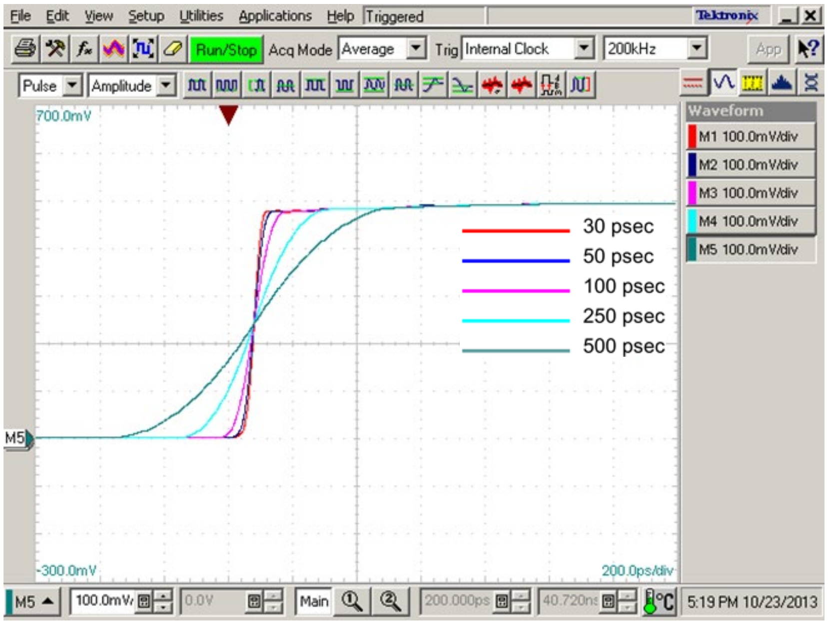
Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options



Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

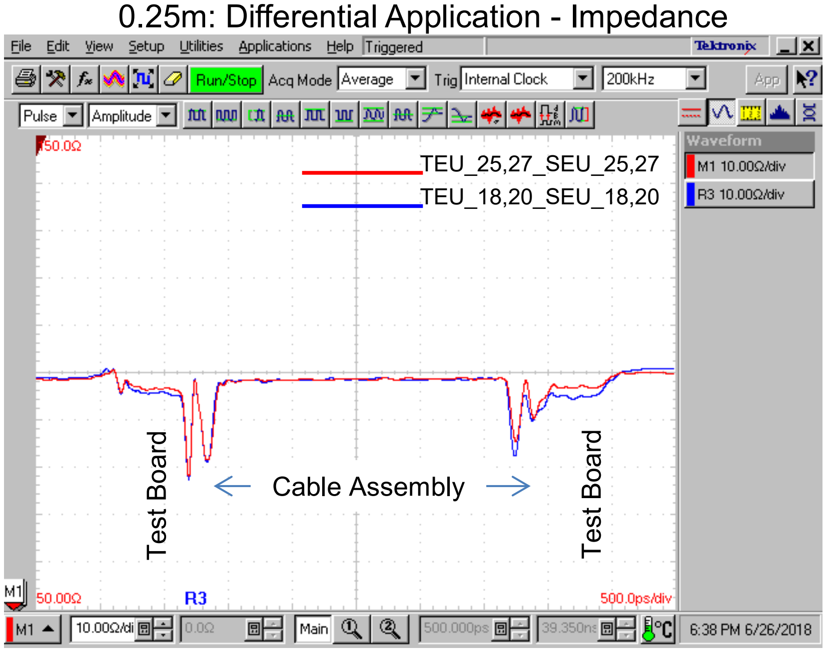
Appendix B – Time Domain Response Graphs

Differential Application – Input Pulse



Differential Application – Cable Assembly Impedance

0.25m: Differential Application - Impedance



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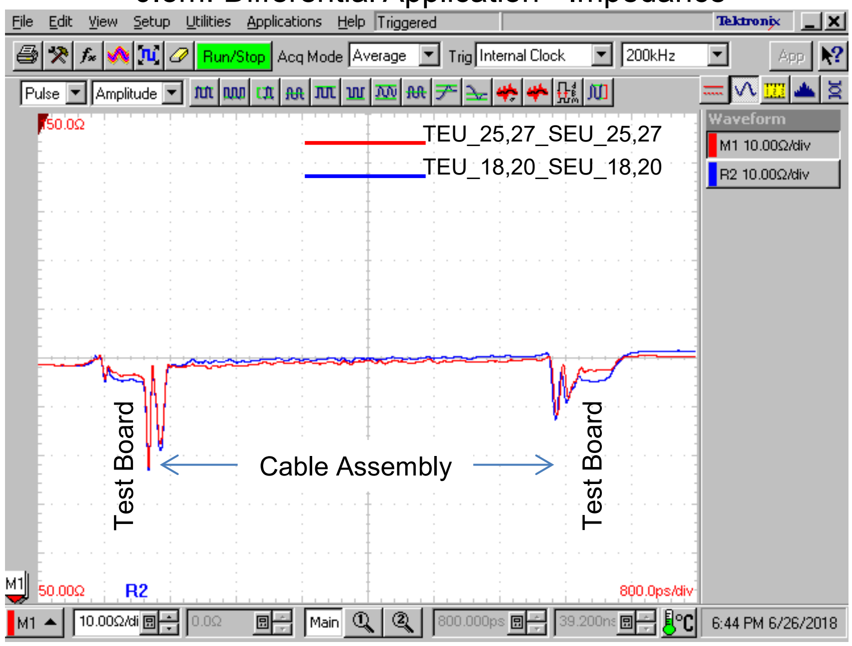
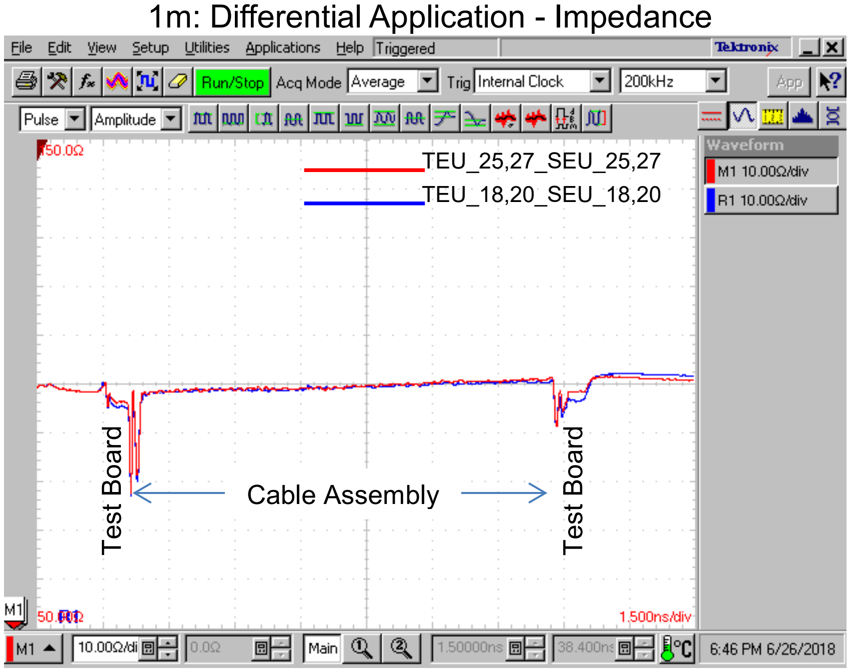
0.5m: Differential Application - Impedance



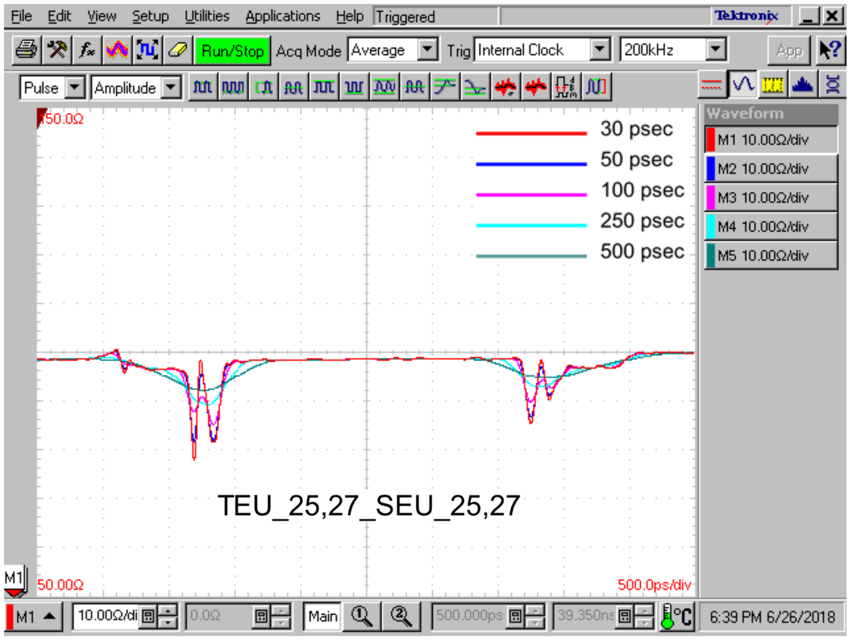
1m: Differential Application - Impedance

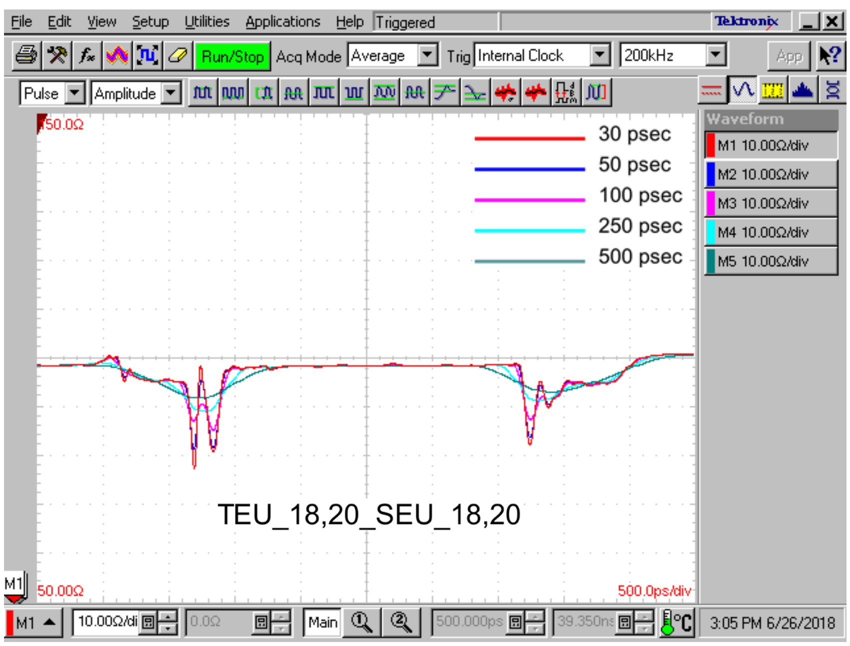


Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

Differential Application – Cable assembly Impedance

EQDP-014-09.80-TEU-SEU-5





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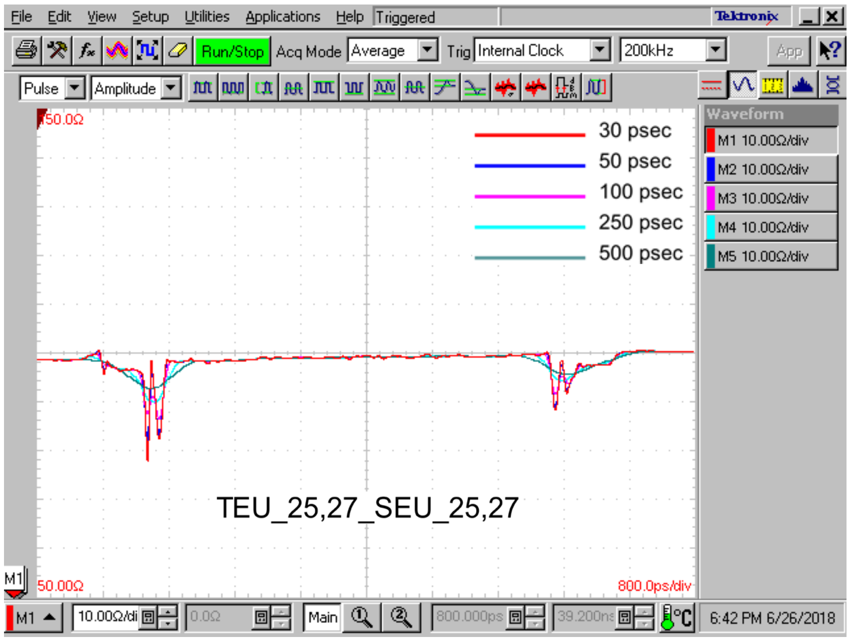
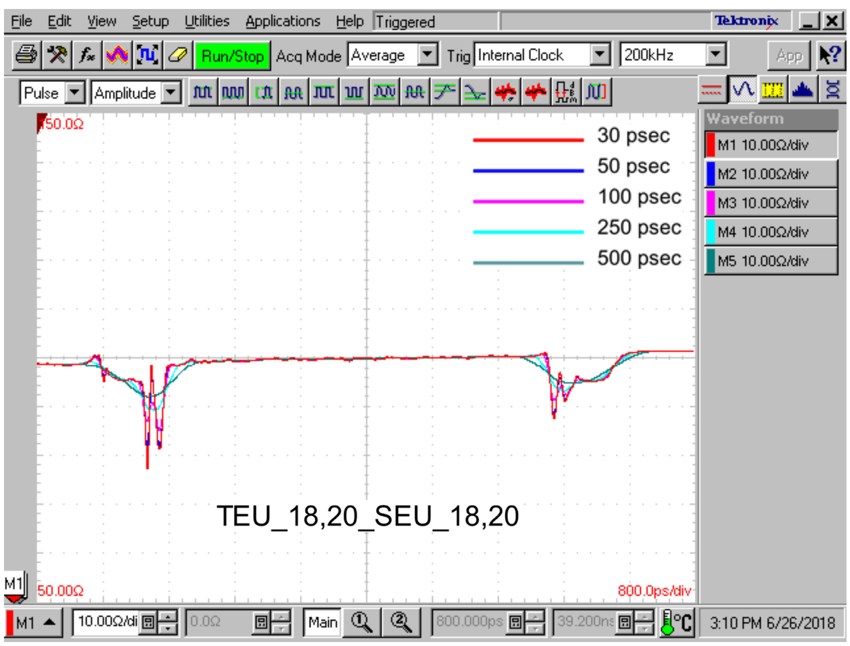
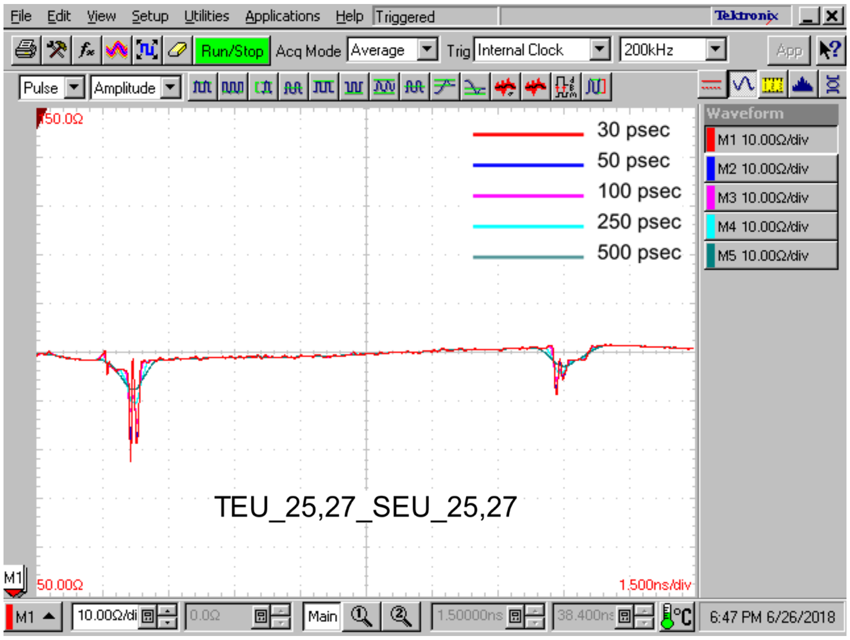
EQDP-014-19.68-TEU-SEU-5

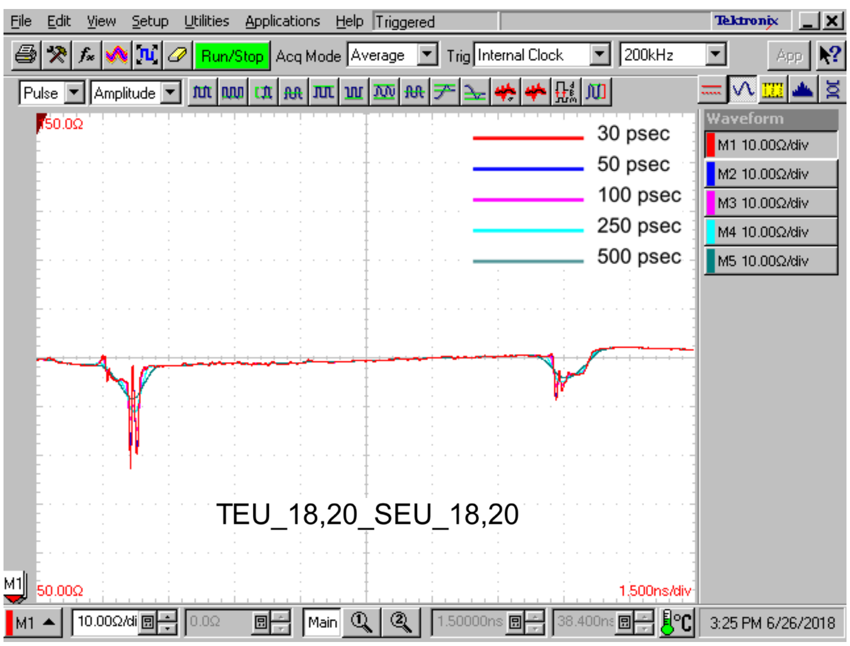




Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

EQDP-014-39.37-TEU-SEU-5





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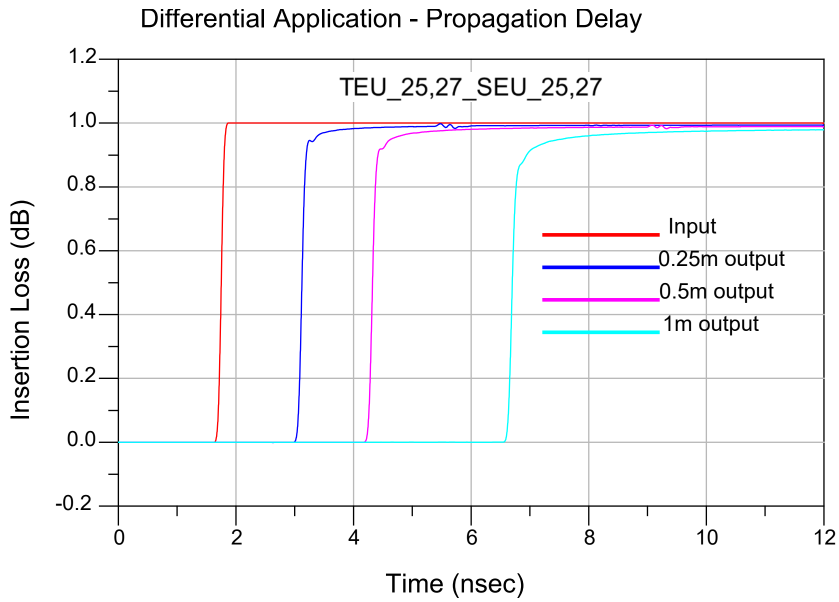
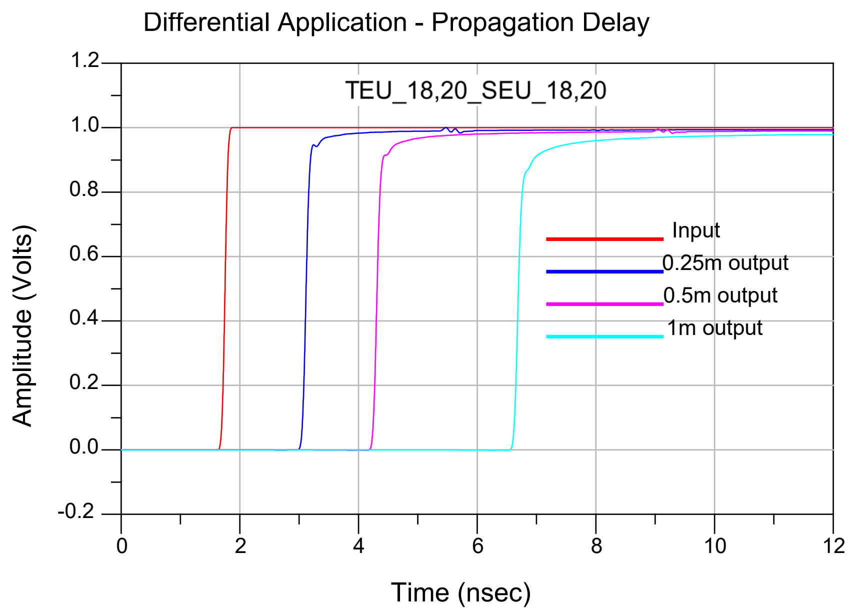
Differential Application – Propagation Delay





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Appendix C – Product and Test System Descriptions

Product Description

Product test samples are 0.8mm Q Strip® High Speed Coax Cable Assemblies. The part numbers are EQDP-014-09.80-TEU-SEU-5, EQDP-014-19.68-TEU-SEU-5 and EQDP-014-39.37-TEU-SEU-5. They mate with QSE-014-01-F-D-DP-A and QTE-014-01-F-D-DP-A. A photo of the mated test article mounted to SI test boards is shown below.

The cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in Table 3 below. There is a total of 7 differential pairs per row. All adjacent lines are terminated where applicable.

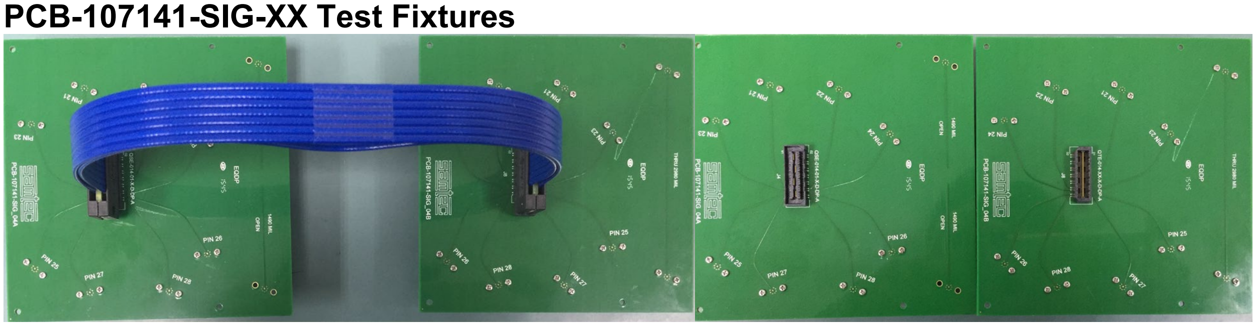
G	G		G	G		T	T		13	15		17	19		21	23		25	27
GROUND																			
G	G		G	G		T	T		14	16		18	20		22	24		26	28

Table 3: Respective signal line numbers as viewed from End 1

Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Two test fixtures are specific to EQDP series cable assemblies and identified by part numbers PCB-107141-SIG-03A and B to PCB-107141-SIG-04A and B. The Auto Fixture Removal (AFR) calibration structures designed specifically for the EQDP series are located on PCB-107141-SIG-03A and 04B. Displayed on the following pages is the information for the EQDP and AFR calibration structure and directives for the mating EQDP fixtures. To keep trace lengths short, two different test board sets were required to access the necessary signal pins.

PCB-107141-SIG-XX Test Fixtures



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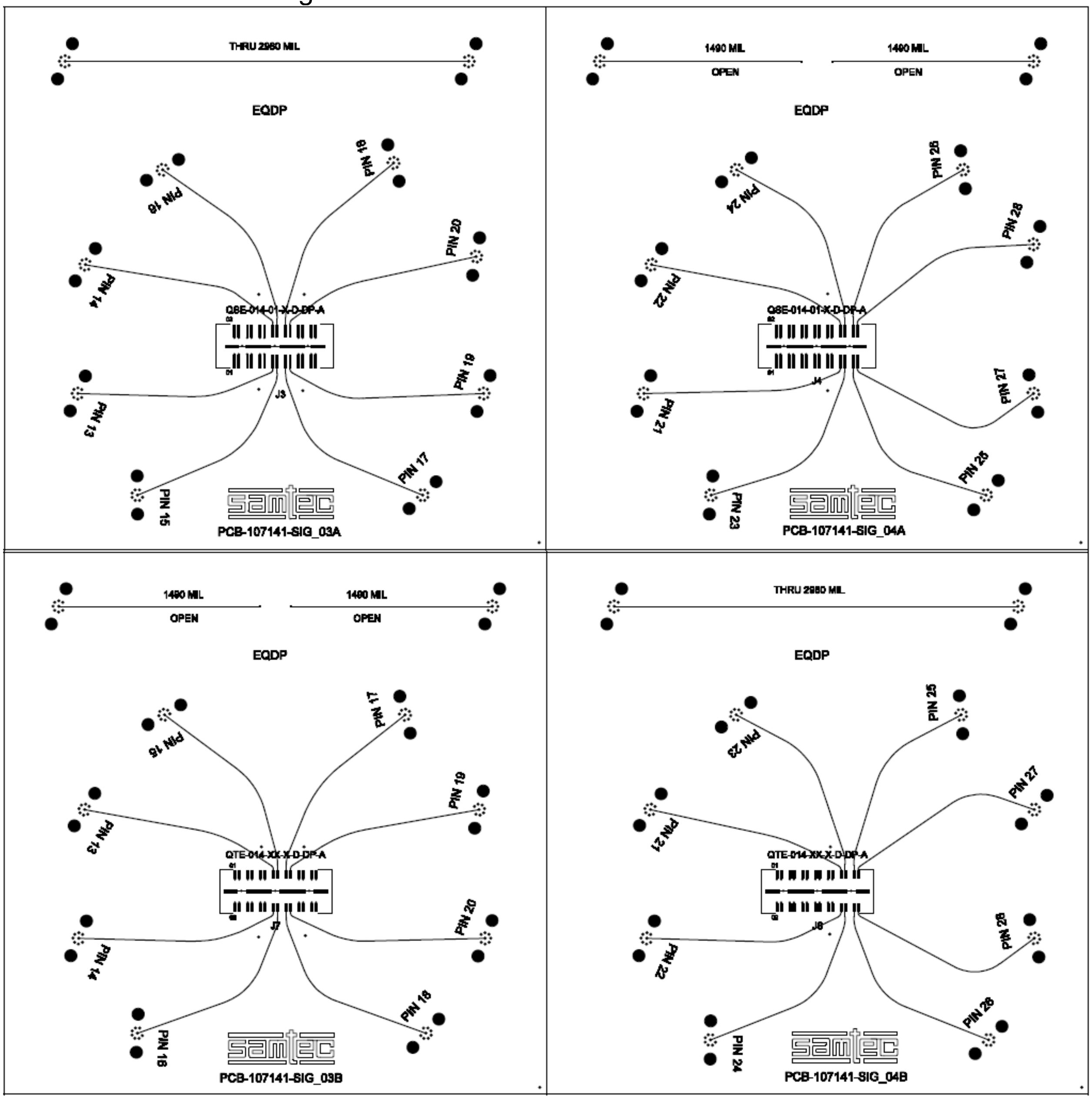
Artwork of the PCB design is shown below.



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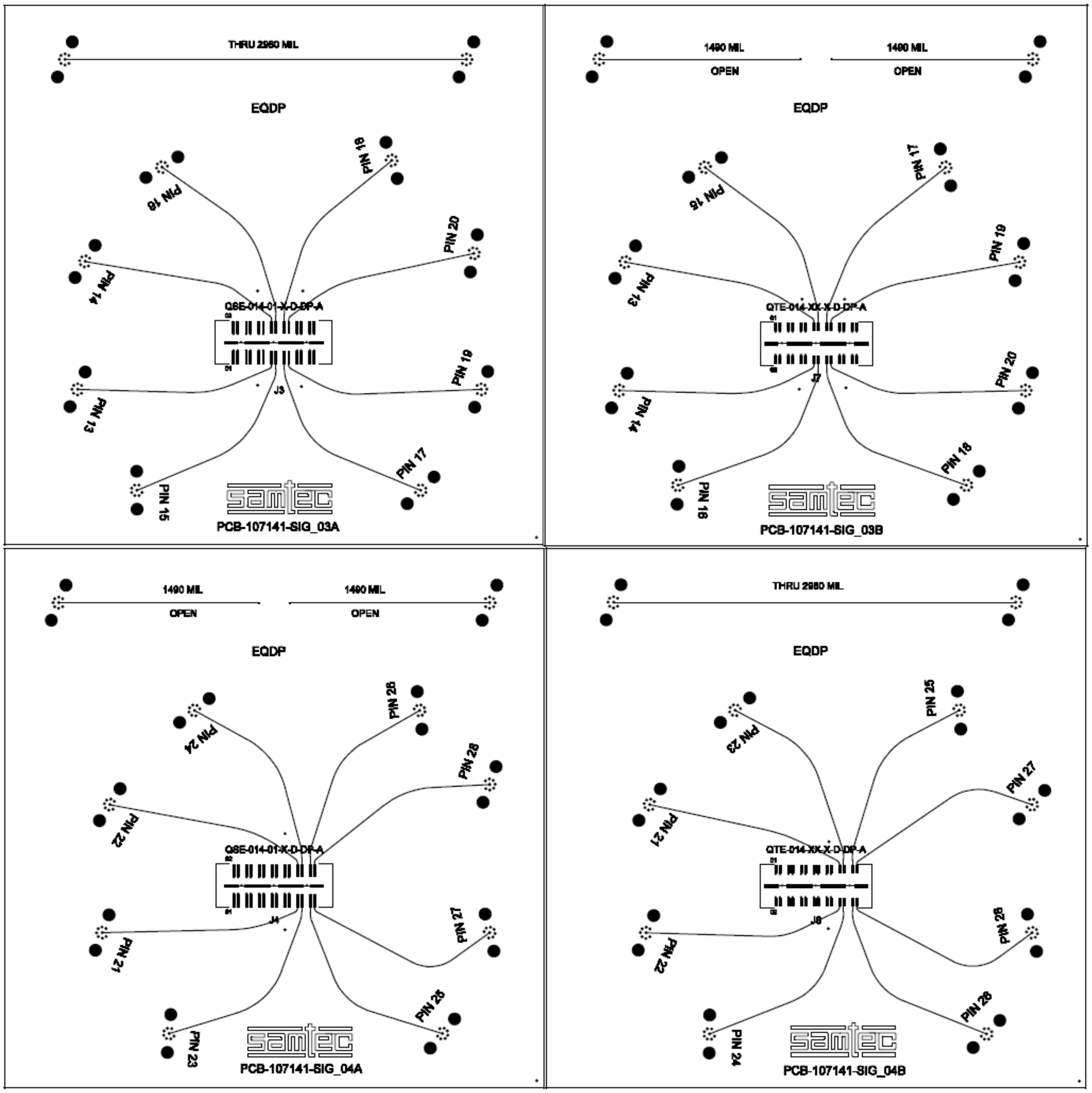
PCB Fixtures

The test fixtures used are as follows:



PCB-107141-SIG-03A– EQCD Cable Test Board 1
PCB-107141-SIG-03B– EQCD Cable Test Board 2
PCB-107141-SIG-04A– EQCD Cable Test Board 3
PCB-107141-SIG-04B– EQCD Cable Test Board 4

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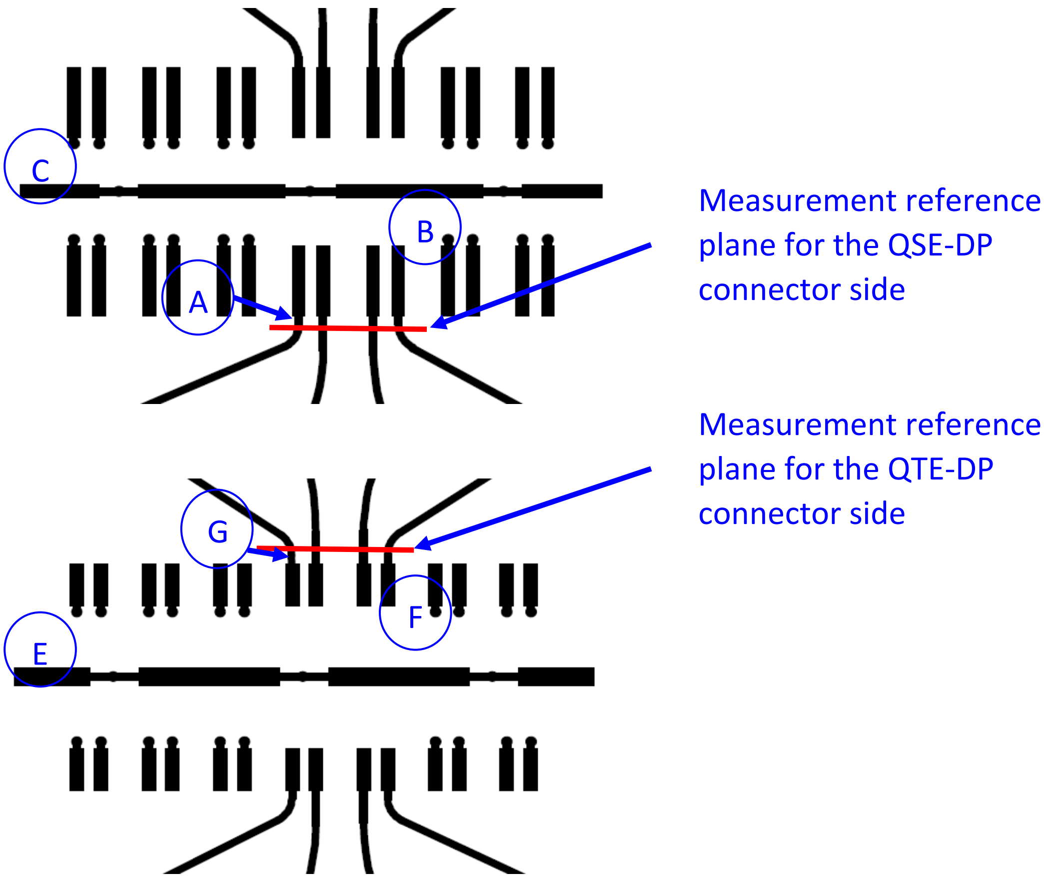
All traces on the test boards are length matched to 1.5" Measured from the edge of the pad to SMA. The AFR calibration effectively removes 1.49" of test board trace effects. This means that 10 mil of test board trace length effects are included in the measurement at each side.

The S-Parameter measurement includes:

A. 10 mil test board trace
B. Test board vias, pads (footprint effects) for the QSE-DP connector
C. The QSE-DP series connector
D. The EQDP-014-XX.XX-TEU-SEU-5 cable assembly
E. The QTE-DP series connector
F. Test board vias, pads (footprint effects) for the QTE-DP connector
G. 10 mil test board trace

The figure below shows the location of the measurement reference plane.



Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

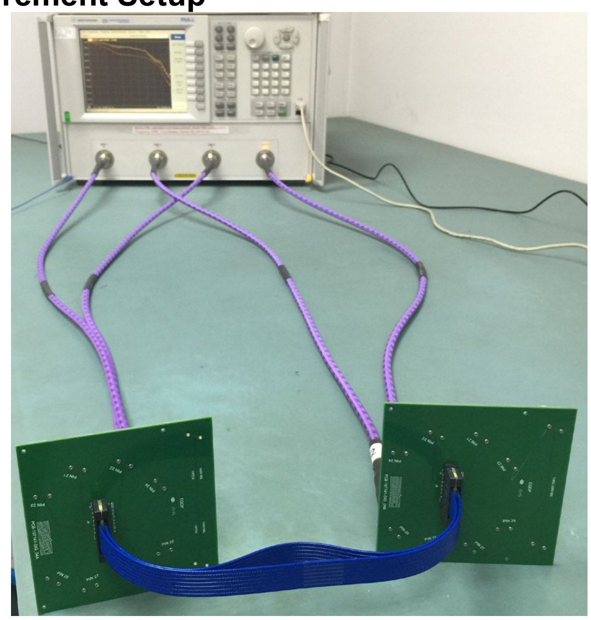
Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Keysight N5230C PNA-L network analyzer. Frequency domain data and graphs are extracted from the instrument by AFR application. Post-processed time domain data and graphs are generated using convolution algorithms within Keysight ADS. The network analyzer is configured as follows:

Start Frequency - 300 KHz	Number of points -1601
Stop Frequency - 20 GHz	IFBW - 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Keysight N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Keysight N4433A ECAL Module (300 KHz to 20 GHz)

Test Cables & Adapters

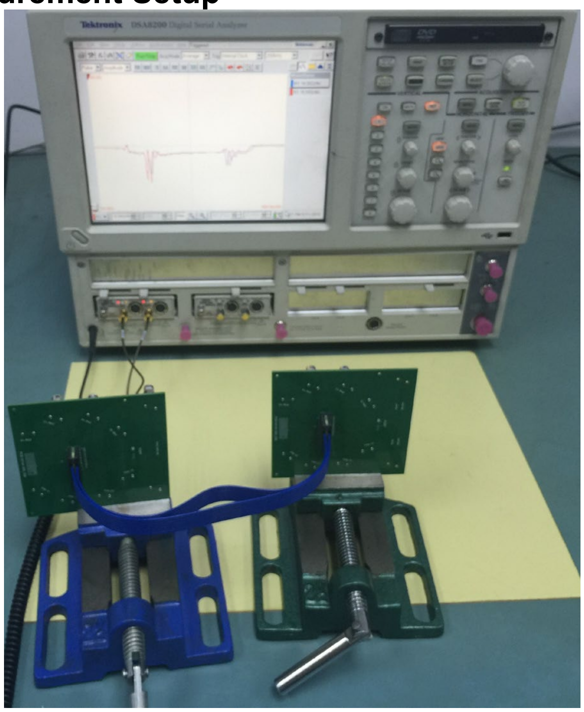
QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale: 10 ohm / Div
Offset: Default / Scroll
Horizontal Scale: 500ps/ Div, 800ps/ Div, 1.5ns/ Div
Record Length: 4000
Averages: ≥ 16

DSA8200 Measurement Setup



Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: EQDP
Description: 0.8 mm Q Pairs® High Speed Cable Assembly, TEU-SEU End Options

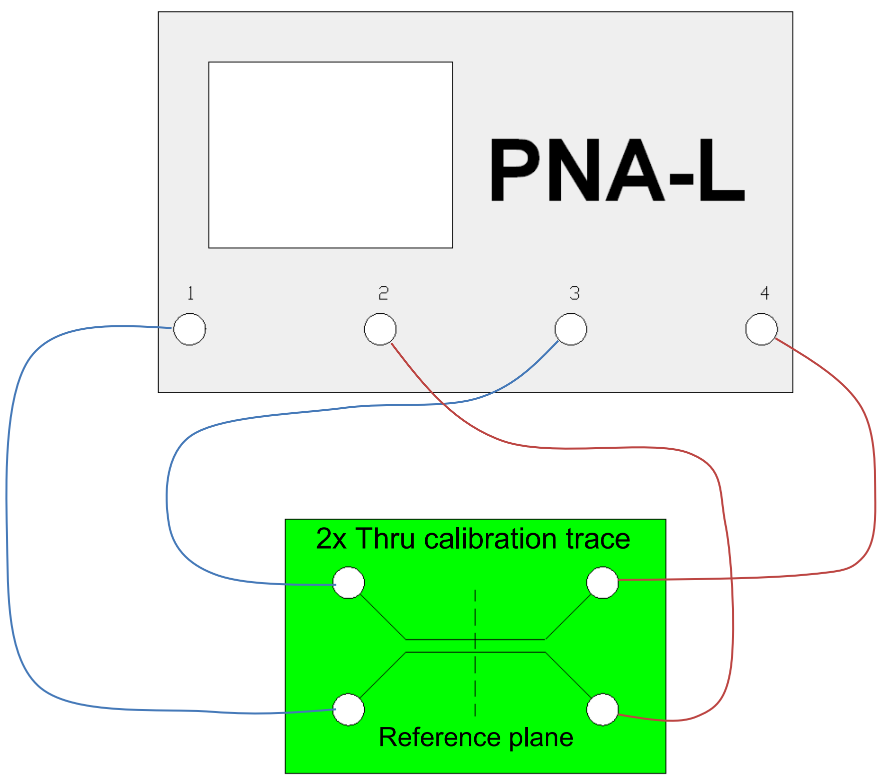
Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-CAL module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the EQDP test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.



Series: EQDP
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Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Impedance (TDR)
Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

Series: EQDP
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Appendix F – Glossary of Terms

ADS – Agilent Advanced Design System
AFR – Automatic Fixture Removal
CTLE – Continuous Time Linear Analyzer
DUT – Device under test
FD – Frequency domain
FEXT – Far-End Crosstalk
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PLTS – Agilent Physical Layer Design System
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
UI – Unit Interval
XROW – Across Row
Z – Impedance (expressed in ohms)