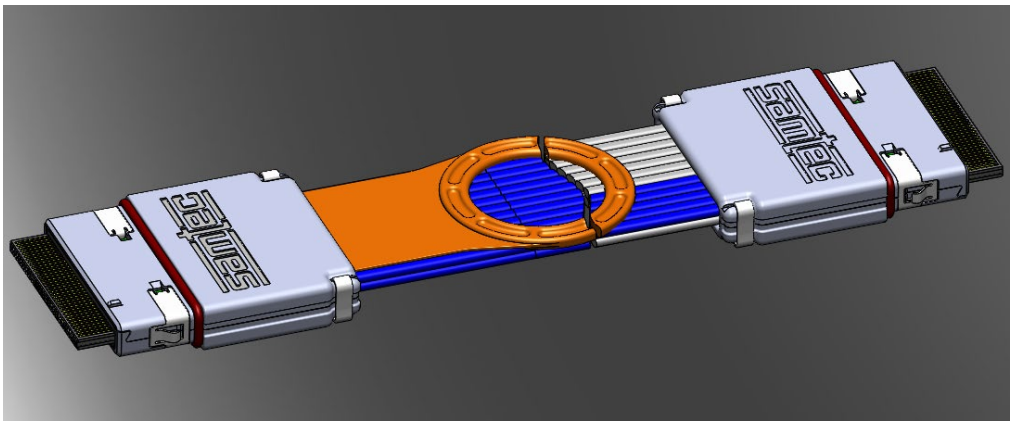
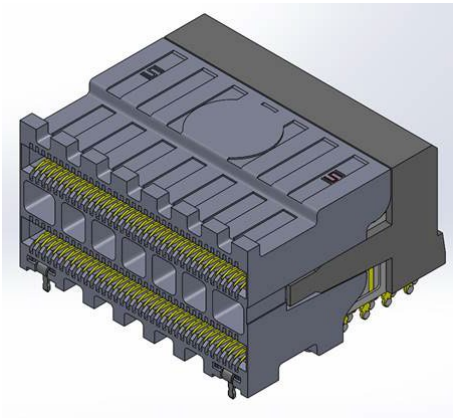
# High Speed Characterization Report

## HDLSP-035-XXXX



**Mated with**:

**HDI6-035-01-RA**



## Description:
## 0.635 mm Eye Speed® HD High-Speed
## High-Density I/O Cable Assembly

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Report Revision: 12/27/2019

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

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**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## Cable Assembly Overview

The 0.635 mm (.025") HDLSP Cable Assembly is constructed using 32 AWG low skew twinax cable. The cable is terminated at both ends with edge card connector, the cable assembly is wired to facilitate a Pin A1 to Pin B1 mapping between the cable terminations. The HDLSP series cable assemblies is available in 35 positions per row,12 pairs per side. The data in this report is applicable to 1000 mm and 2000 mm length cable assembly.

Each HDLSP cable assembly was tested by mating it to HDI6-035-01-RA at both ends. One sample of each assembly was tested. The actual part numbers that were tested are shown in Table 1, which also identifies End 1 and End 2 of each assembly. A relative sample picture is shown in Figure1. Two differential pairs, a Long Path and a Short Path, of each assembly type were tested.

| Length | Part Number | End 1 | End 2 |
|---|---|---|---|
| 1000 mm | HDLSP-035-1000 | Edge-Card | Edge-Card |
| 2000 mm | HDLSP-035-2000 | Edge-Card | Edge-Card |

**Table 1: Sample Description**

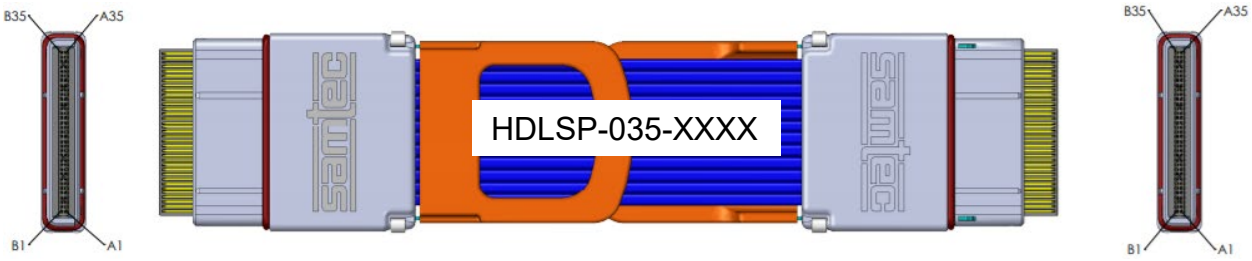


**Figure 1: Test Sample**

**Series:** HDLSP
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# Frequency Domain Data Summary

## Bandwidth Figures – Differential Insertion Loss

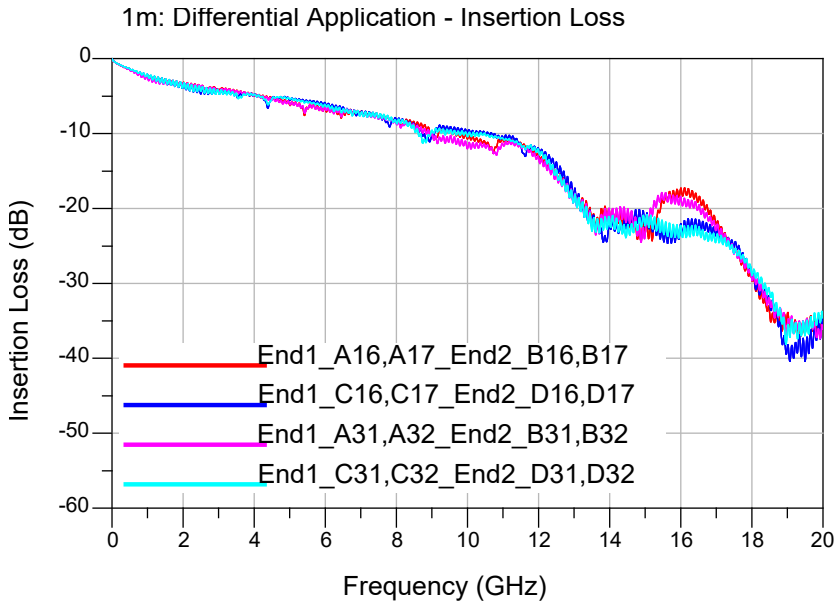


Figure 2

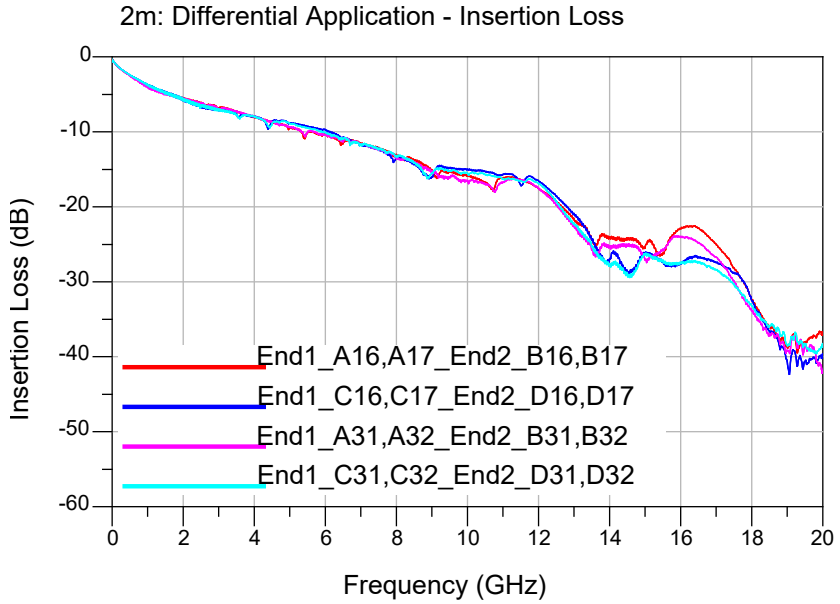


Figure 3

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## Time Domain Data Summary

1 m: Differential Application - Impedance

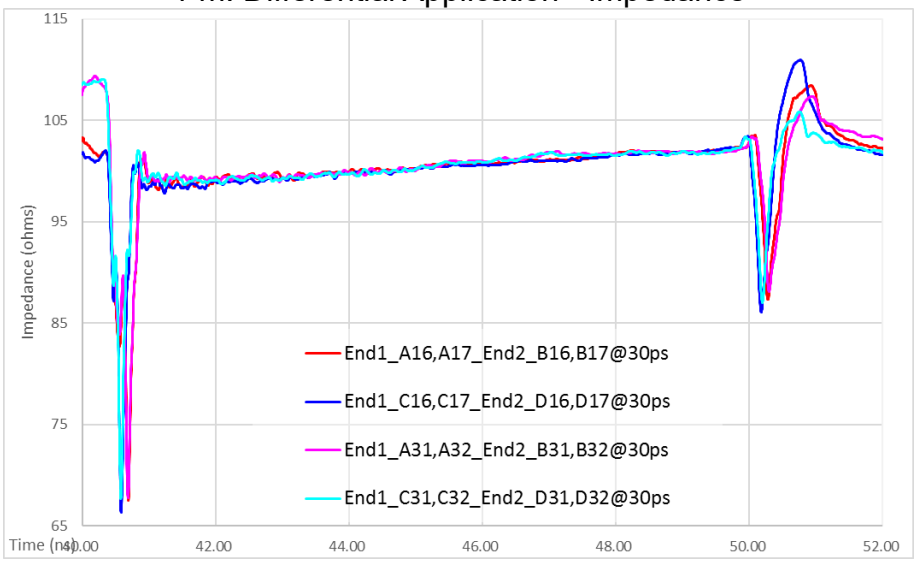


Figure 4

Because the same type cable is used in the cable assemblies with different lengths, only the impedance profile of 1 m cable assembly is reported.

**Table 2 - Propagation Delay (Cable Assembly)**

| Driver | Receiver | 1 m | 2 m |
|---|---|---|---|
| End1_A16，A17 | End2_B16，B17 | 5.043 ns | 9.746 ns |
| End1_C16，C17 | End2_D16，D17 | 4.942 ns | 9.645 ns |
| End1_A31，A32 | End2_B31，B32 | 5.044 ns | 9.744 ns |
| End1_C31，C32 | End2_D31，D32 | 4.939 ns | 9.640 ns |

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## Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

### Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GSSG" differential drive configuration only.

### Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this cable assembly, the following array configurations are evaluated:

Differential Impedance**:**

- Long Path (furthest from test fixture)
- Short Path (closest to test fixture)

Differential Crosstalk**:**

- Across Row: “Xrow”: (from one row of terminals to the other row)

See Appendix C – Product and Test System Descriptions for details

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 100 ps.

Unless otherwise stated, measured rise times were at 20%-80% signal levels.

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## Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

## Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length and signal propagation time in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix B of this report.

The measured S-Parameters from the network analyzer are post-processed using Keysight ADS to obtain the time domain response for signal propagation time. The Time Domain procedure is provided in Appendix D of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 10 mils of PCB trace on each connector side. Delay is measured at 100 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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# Appendix A – Frequency Domain Responses

## Differential Application – Insertion Loss

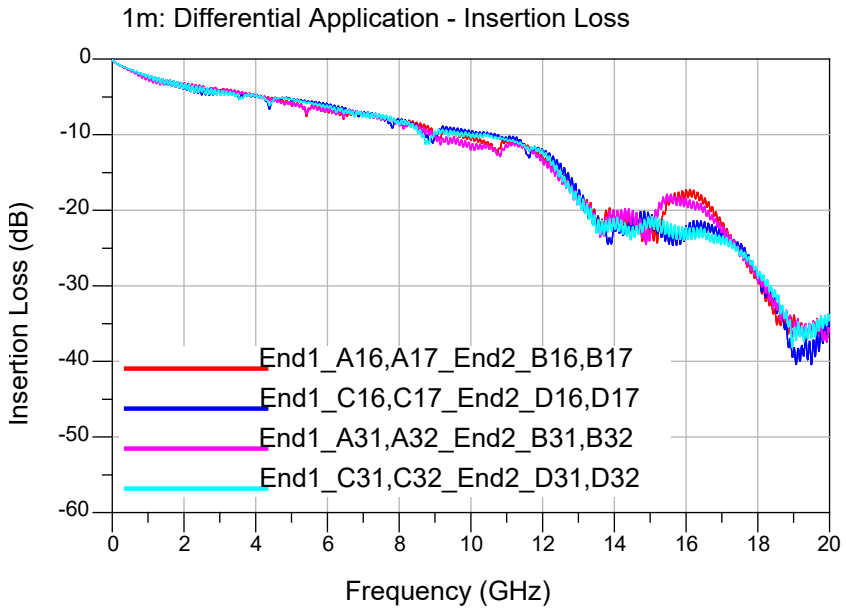


Figure 5

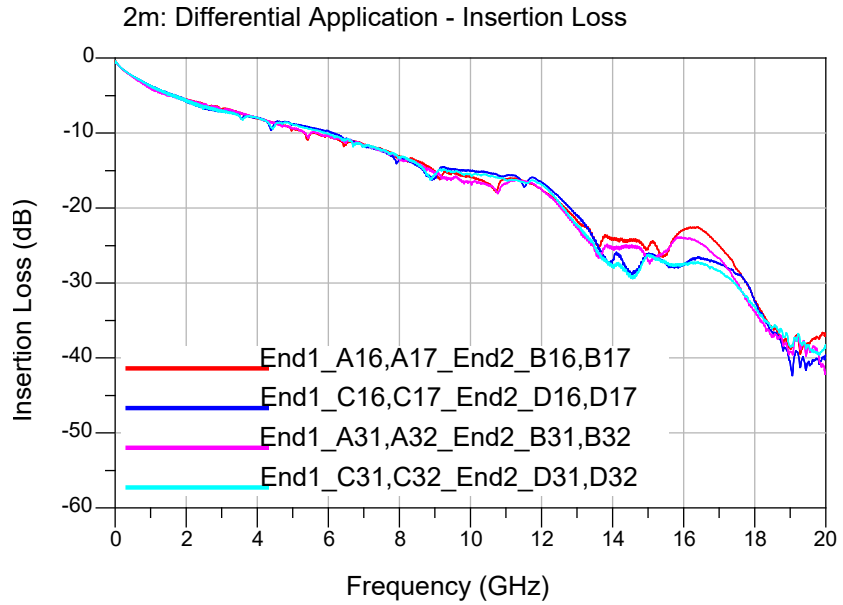


Figure 6

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## Differential Application – Return Loss

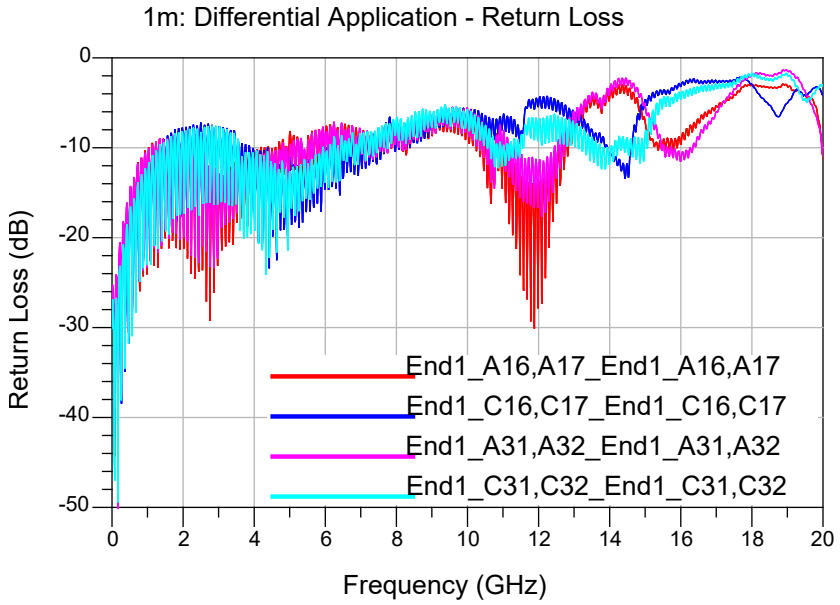


Figure 7

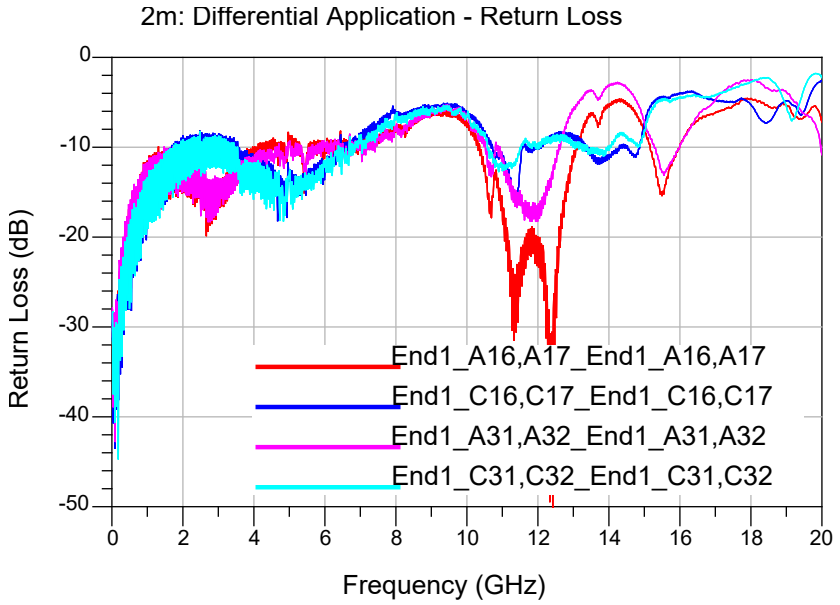


Figure 8

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## Differential Application – NEXT Configurations

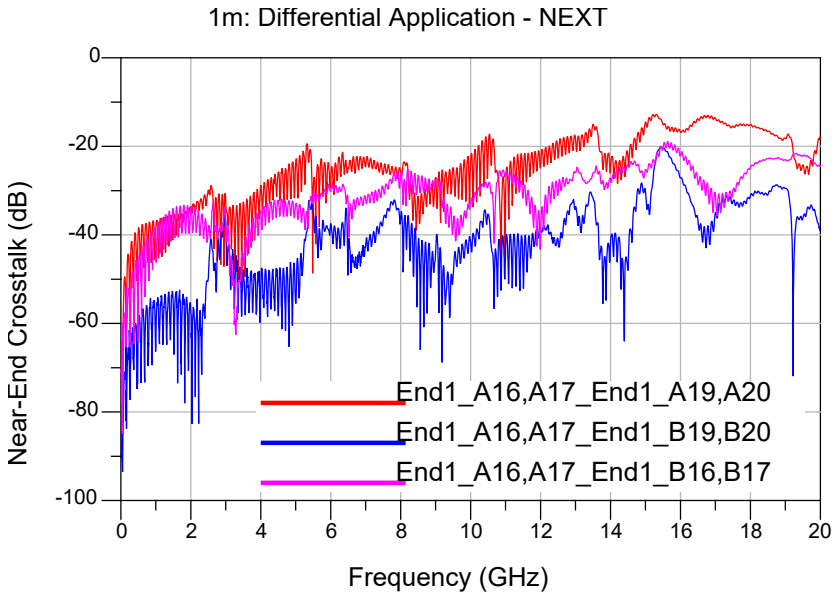


Figure 9

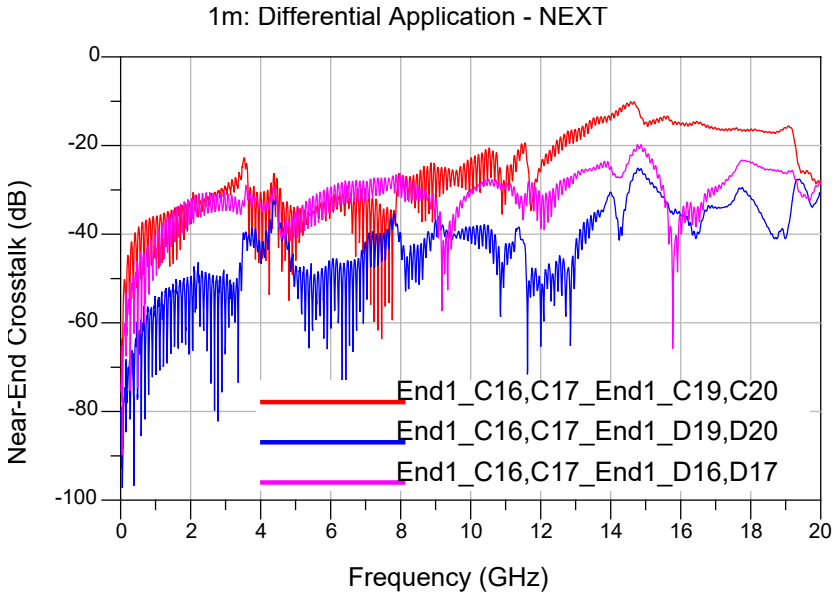


Figure 10

**Series:** HDLSP
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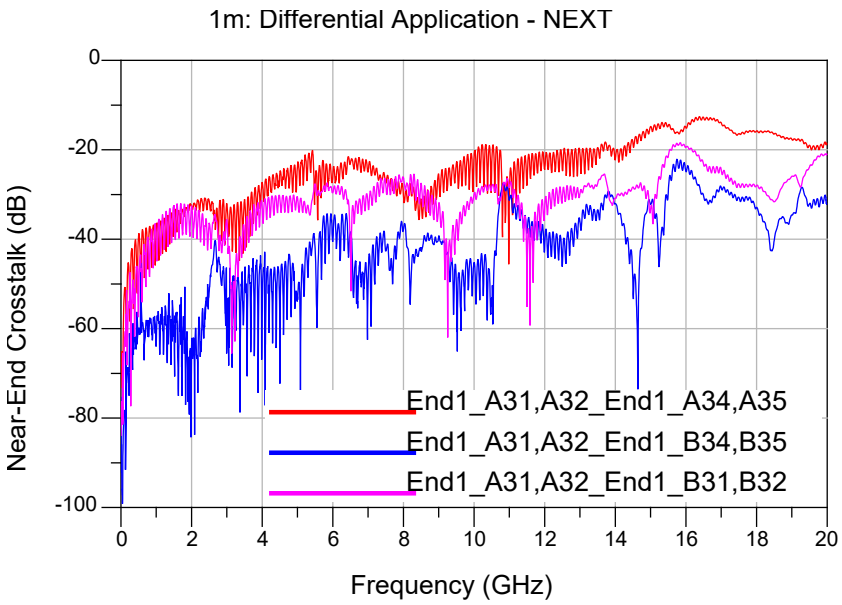


Figure 11

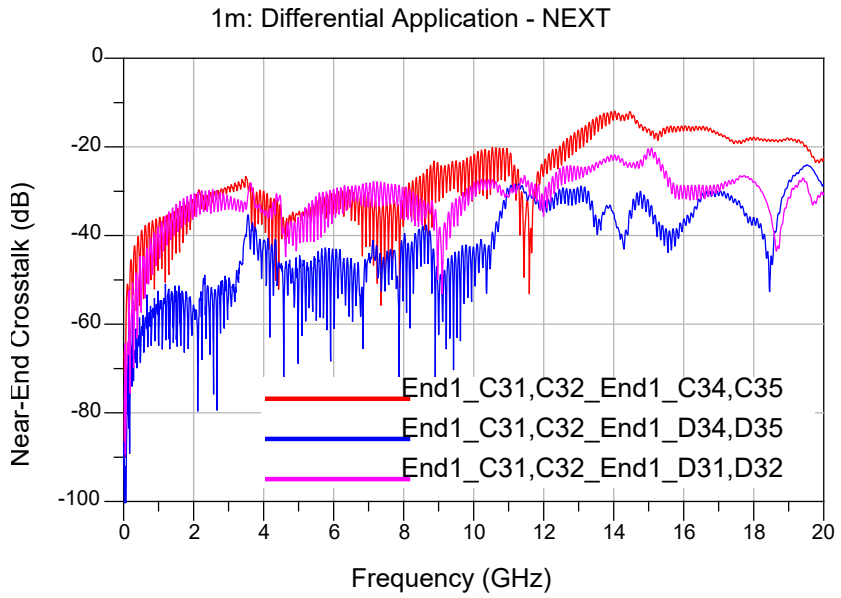


Figure 12

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

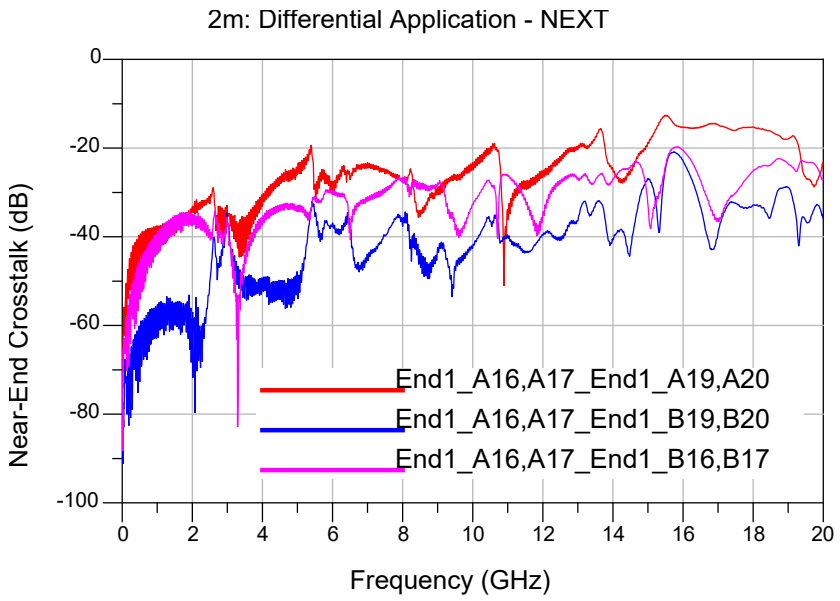


Figure 13

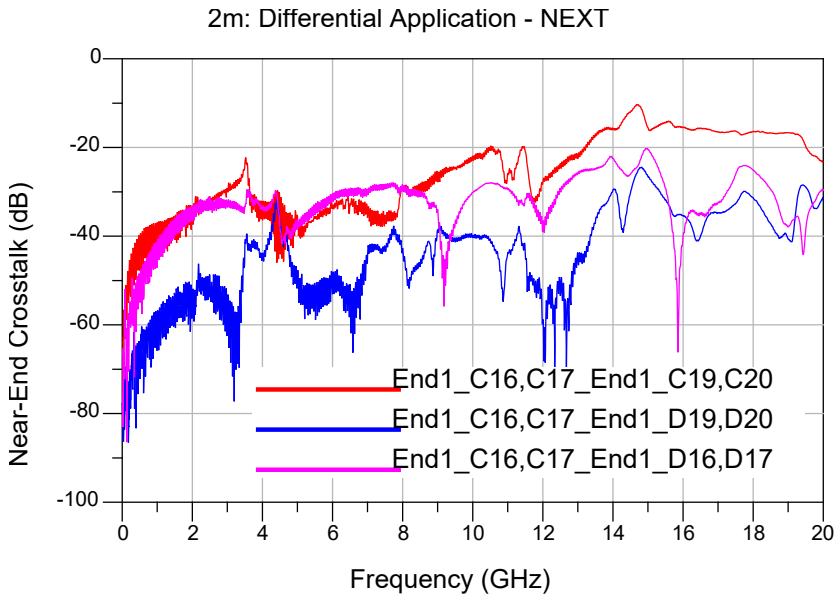


Figure 14

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

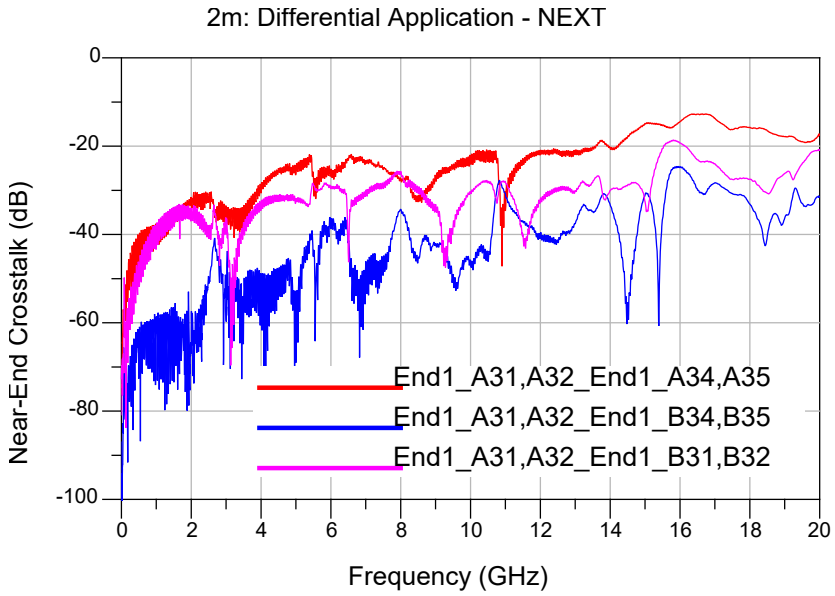


Figure 15

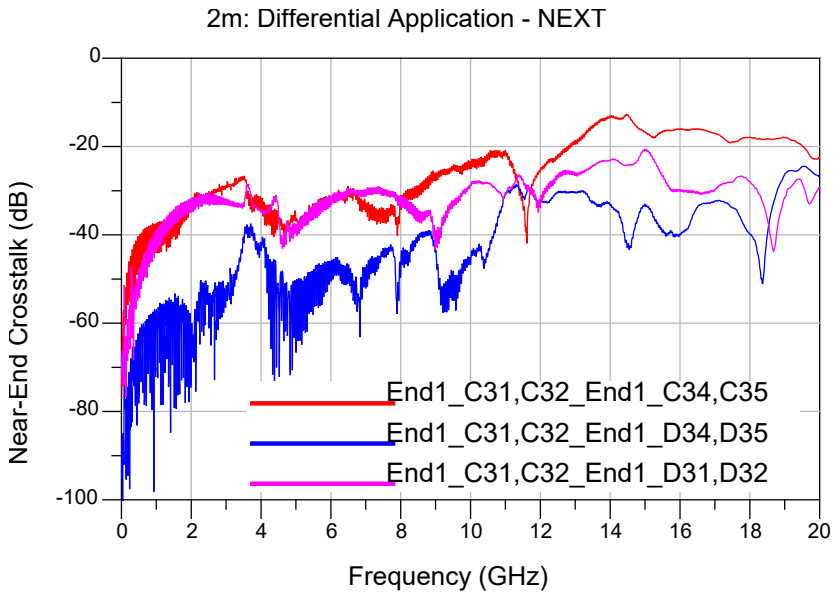


Figure 16

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## Differential Application – FEXT Configurations

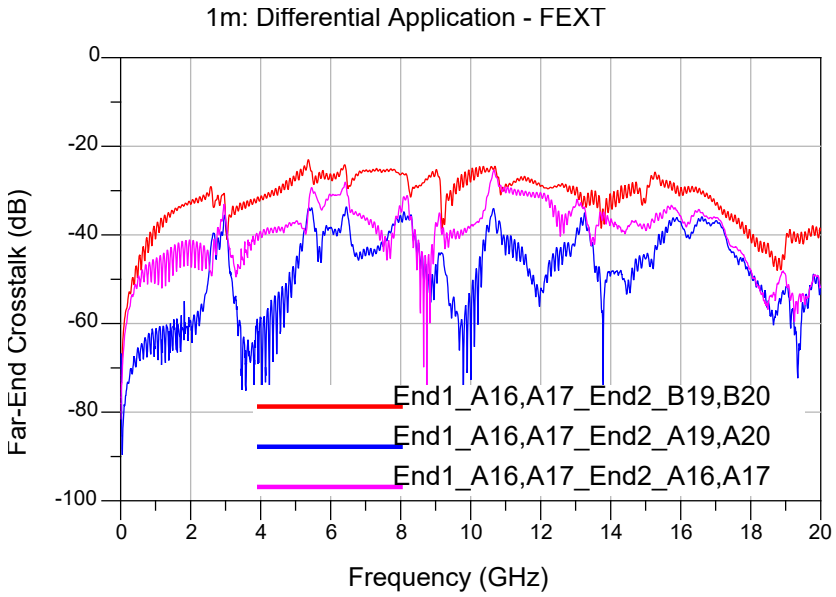


Figure 17

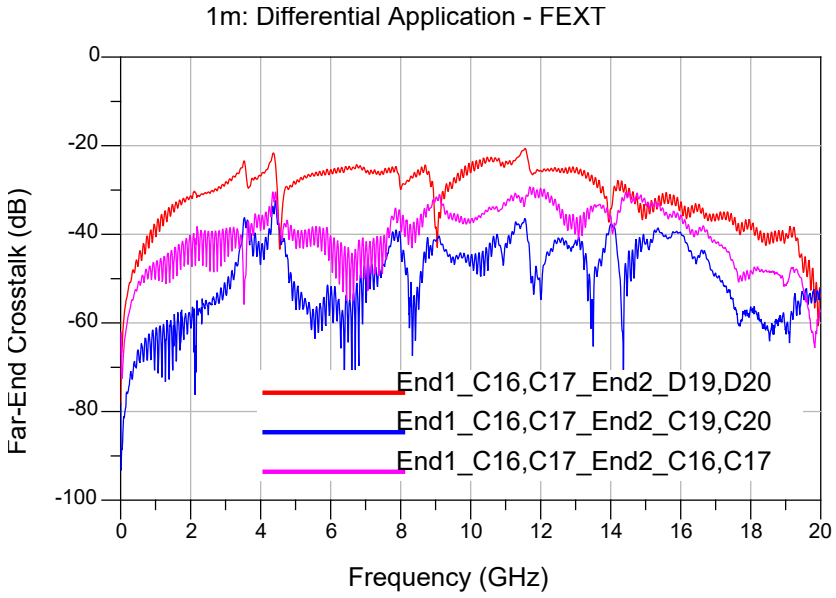


Figure 18

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

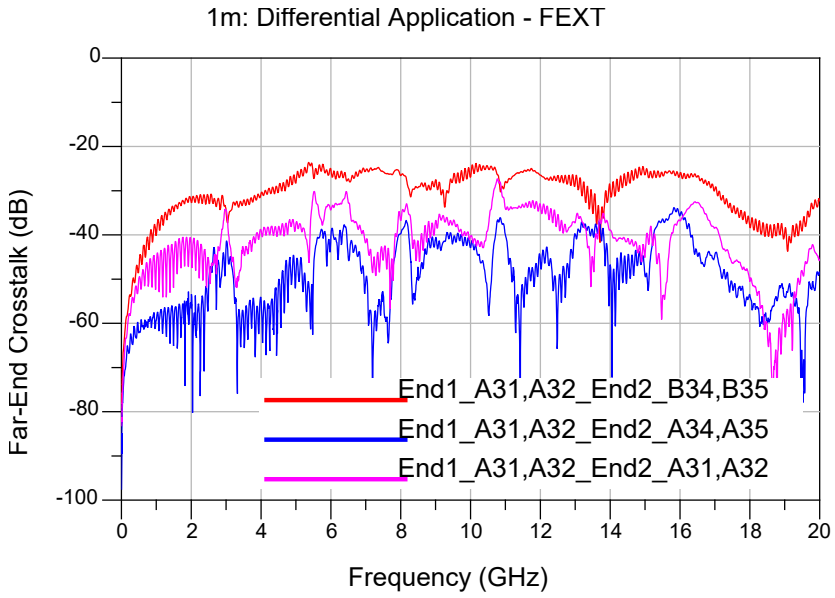


Figure 19

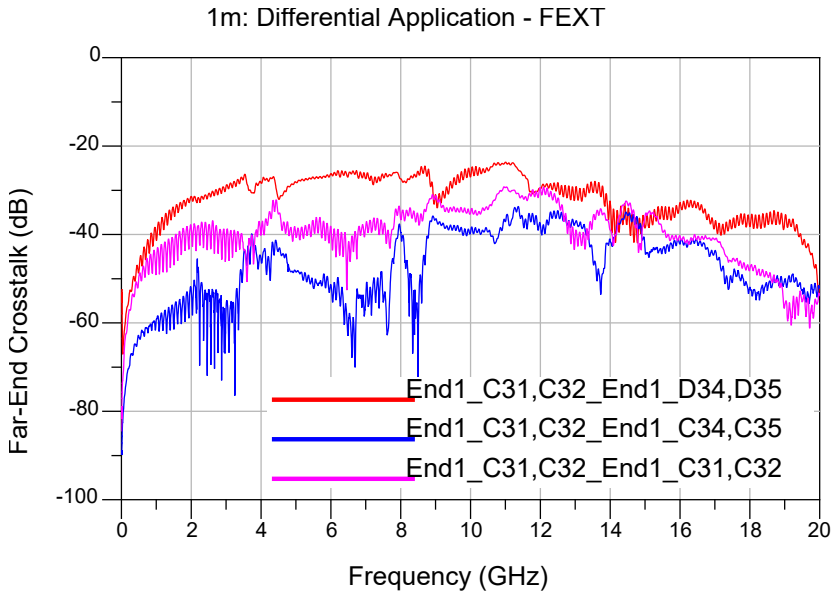


Figure 20

**Series:** HDLSP
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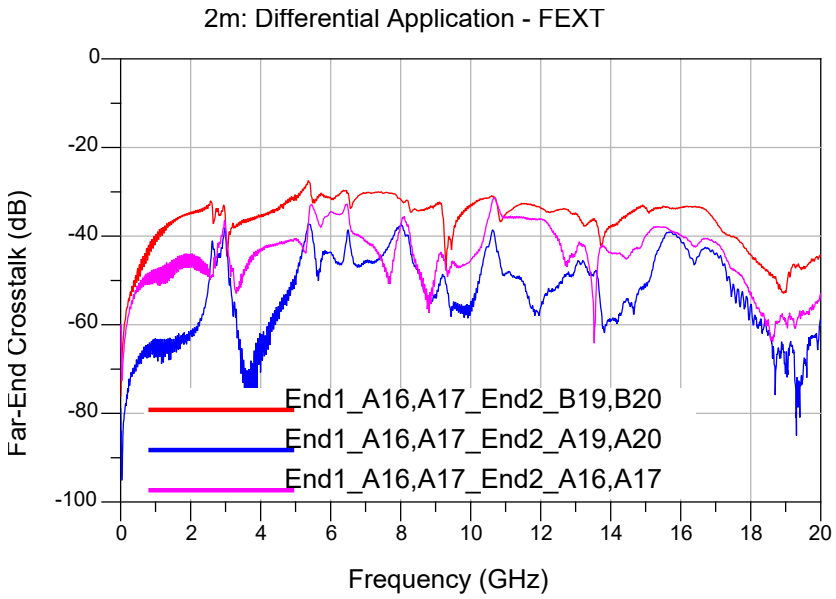


Figure 21

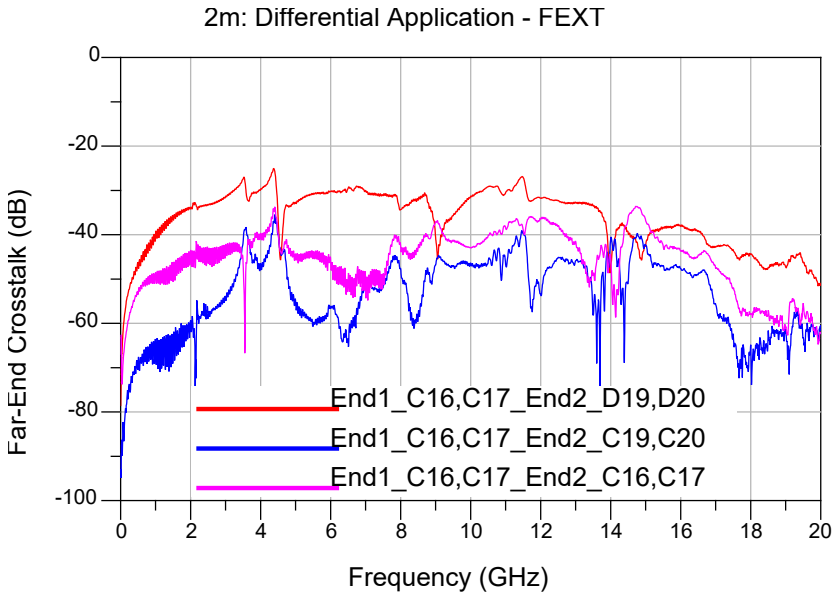


Figure 22

**Series:** HDLSP
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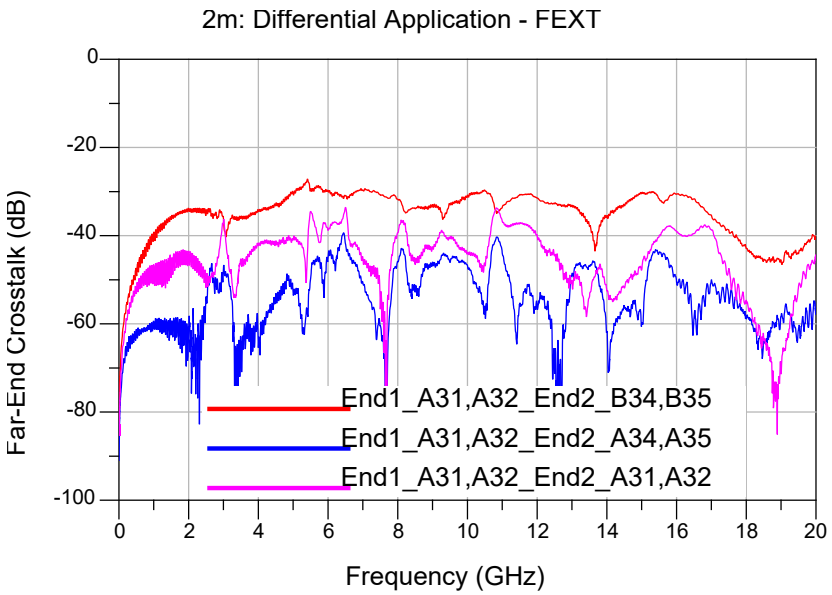


Figure 23

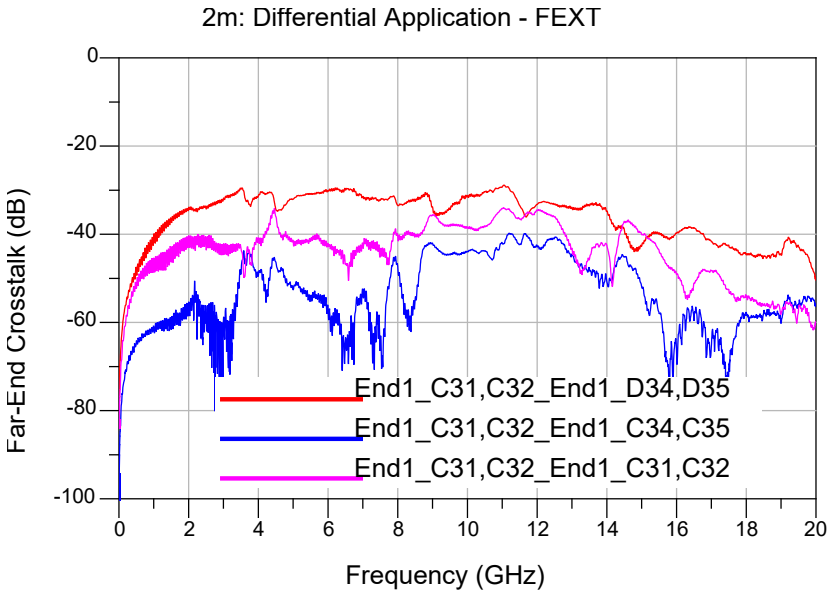


Figure 24

**Series:** HDLSP
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## Differential Application – Differential to Common Mode Conversion

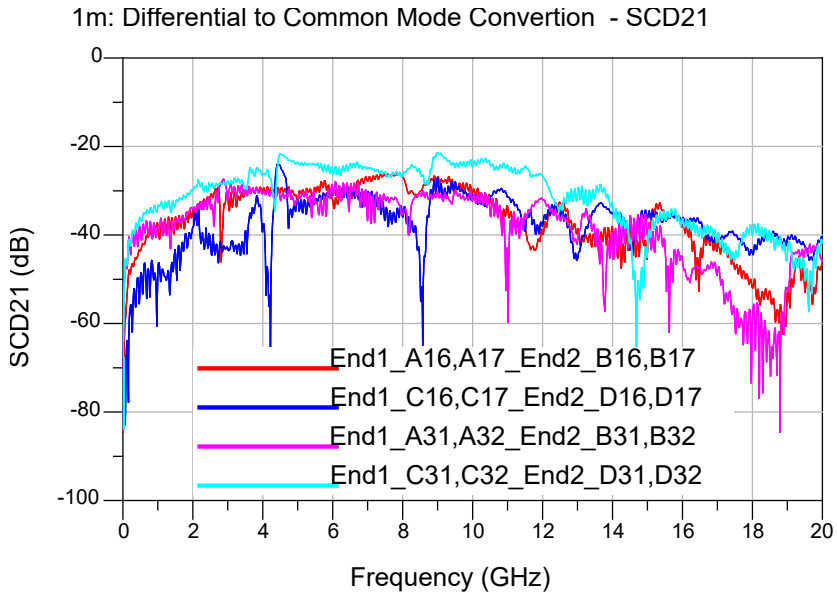


Figure 25

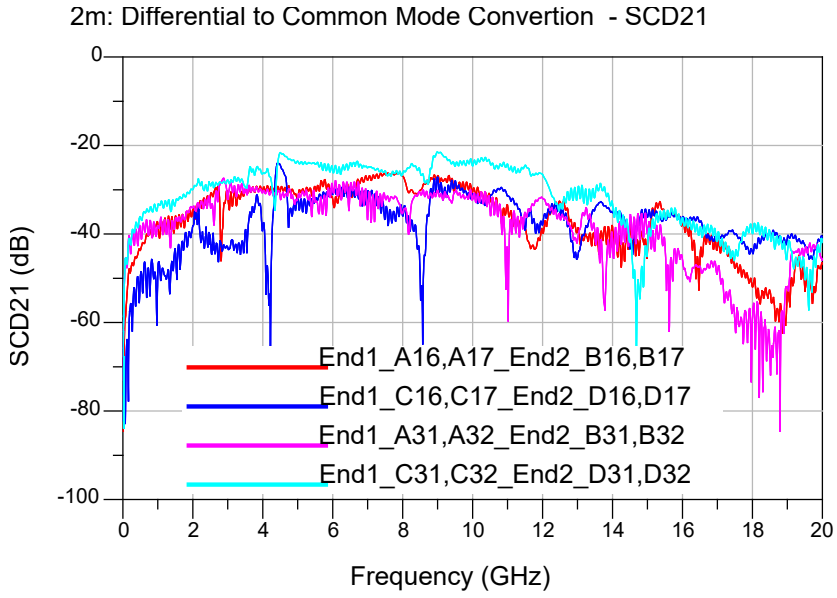


Figure 26

**Series:** HDLSP
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# Appendix B – Time Domain Responses

## Differential Application – Input Pulse

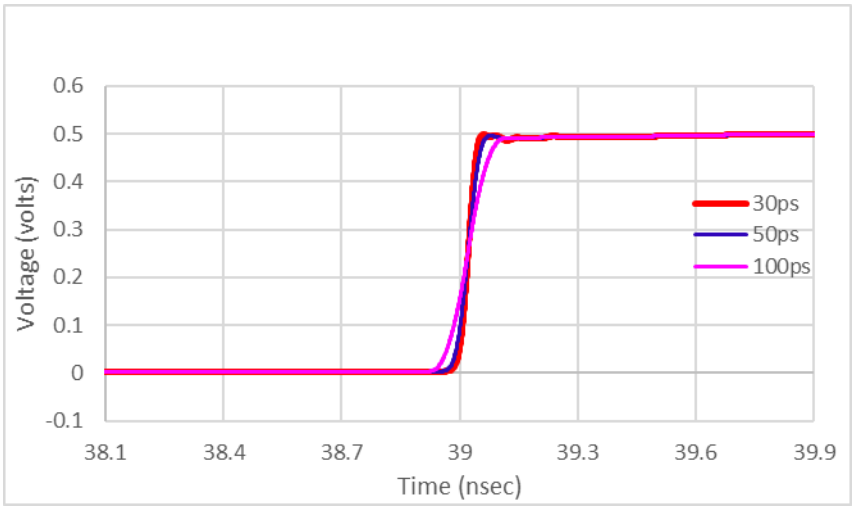


Figure 27

## Differential Application – Cable assembly Impedance

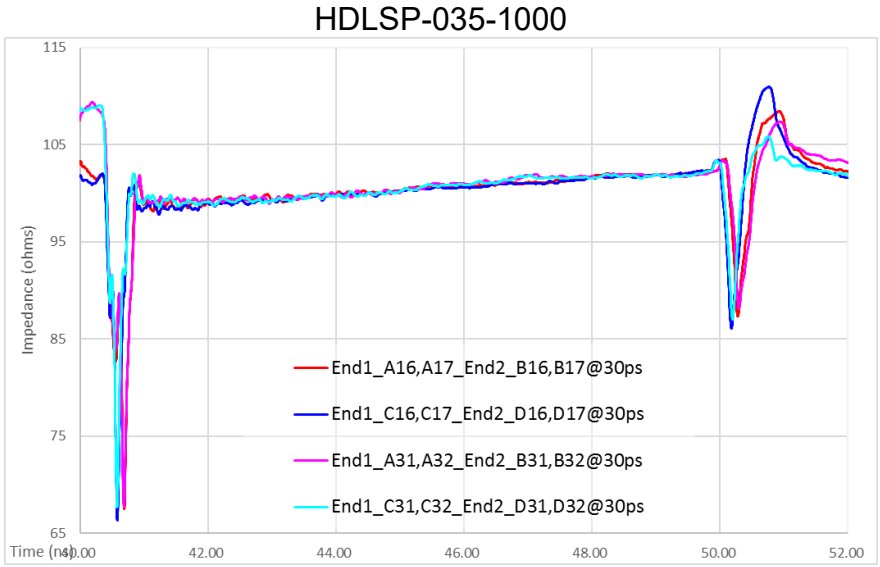


Figure 28

**Series:** HDLSP
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## Differential Application – Cable assembly Impedance

HDLSP-035-1000

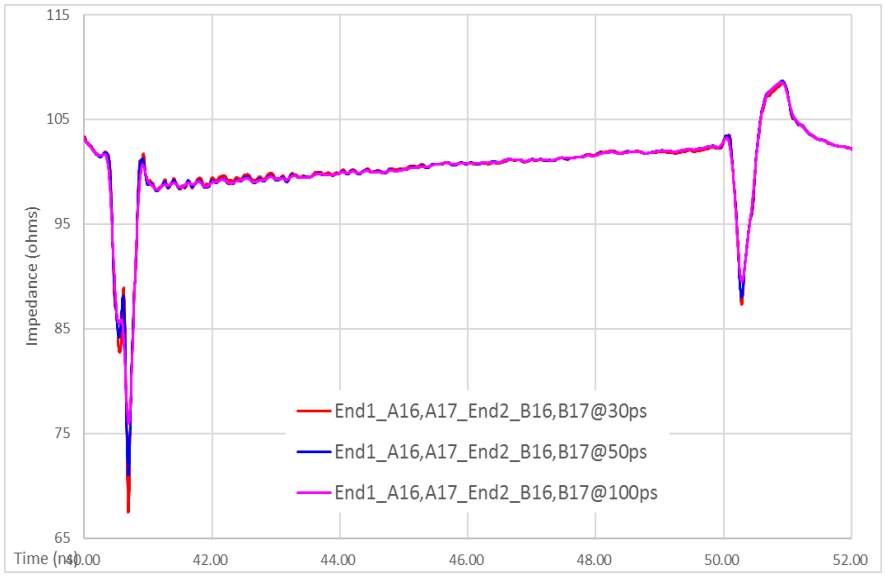


Figure 29

HDLSP-035-1000

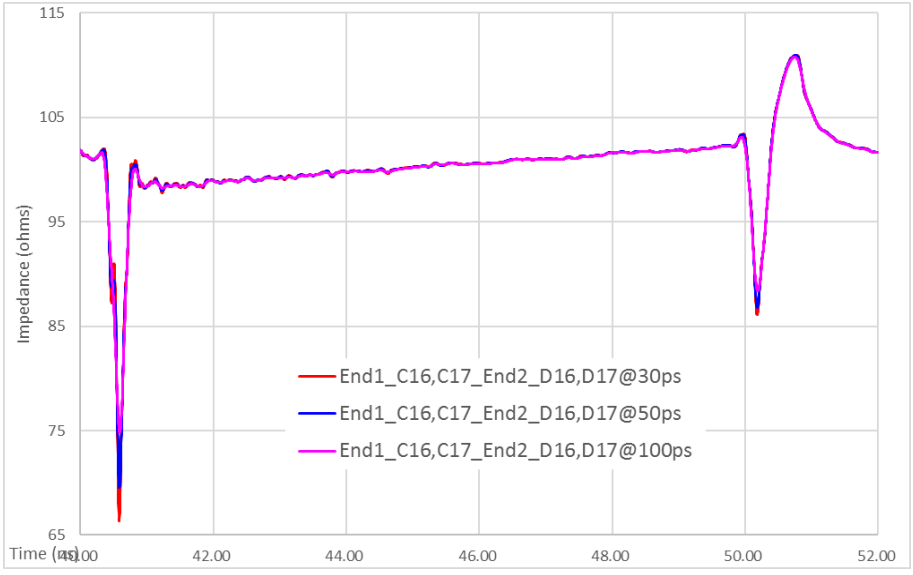


Figure 30

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

HDLSP-035-1000

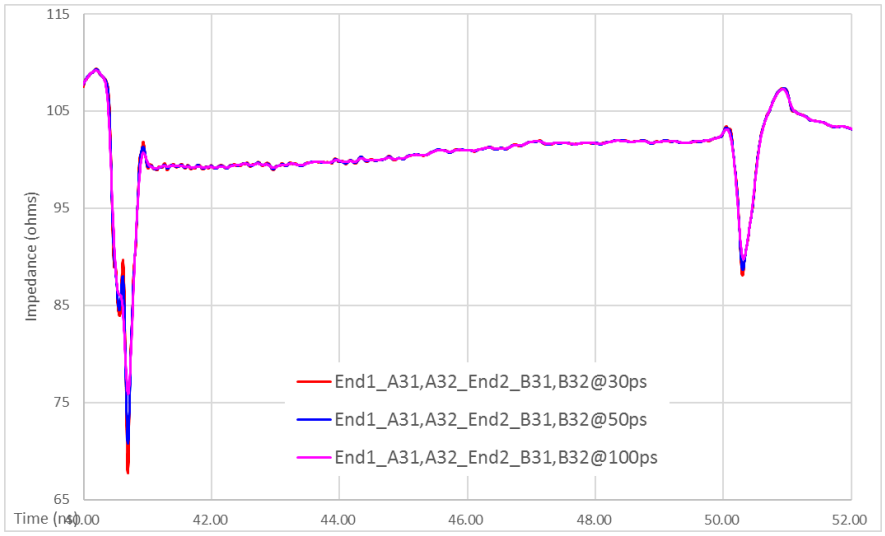


Figure 31

HDLSP-035-1000

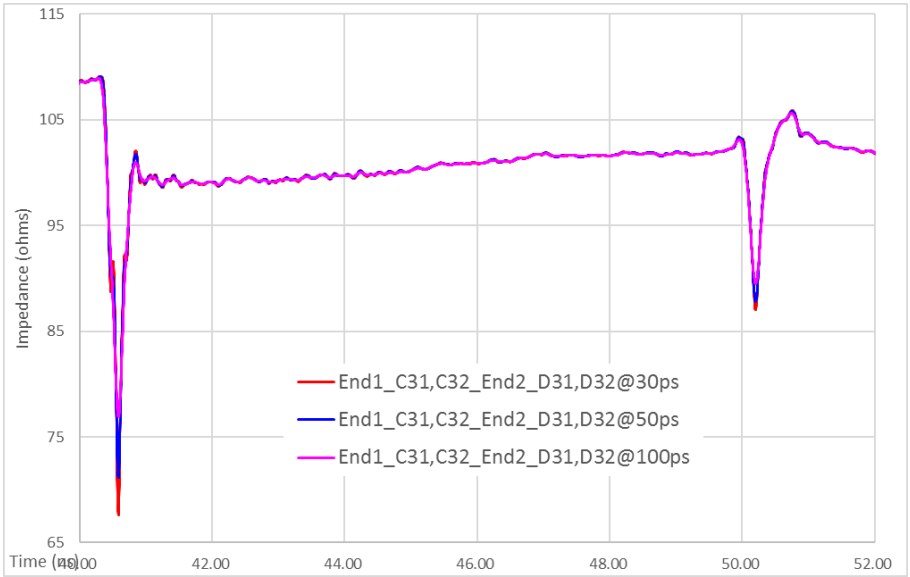


Figure 32

## Differential Application – Propagation Delay

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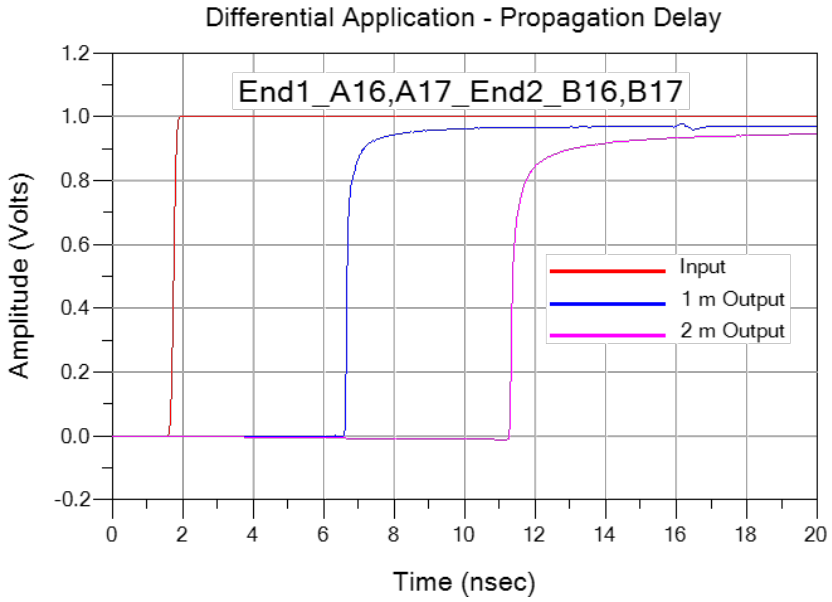


Figure 33

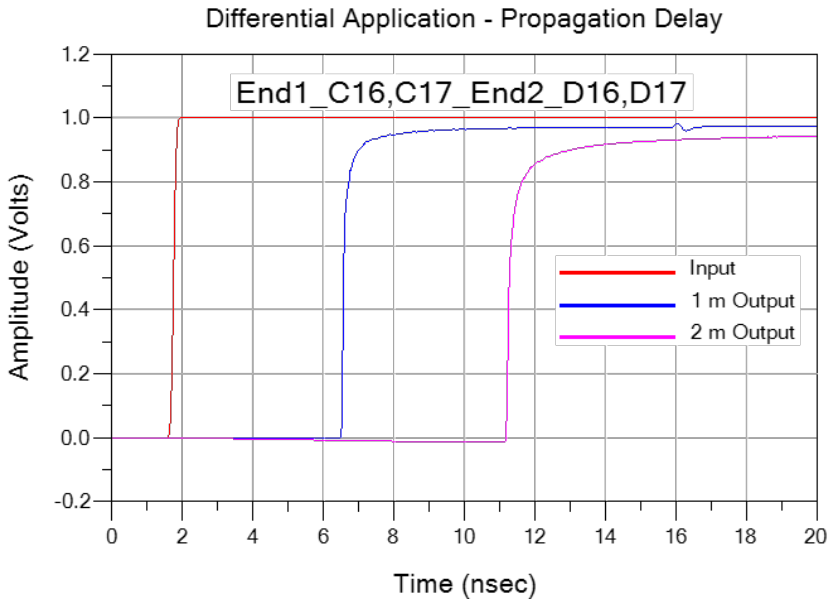


Figure 34

**Series:** HDLSP
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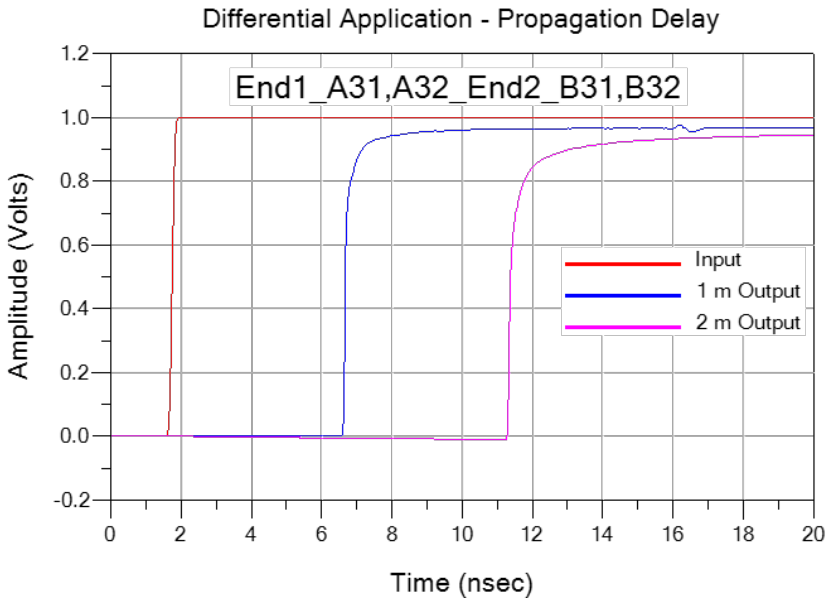



Figure 35

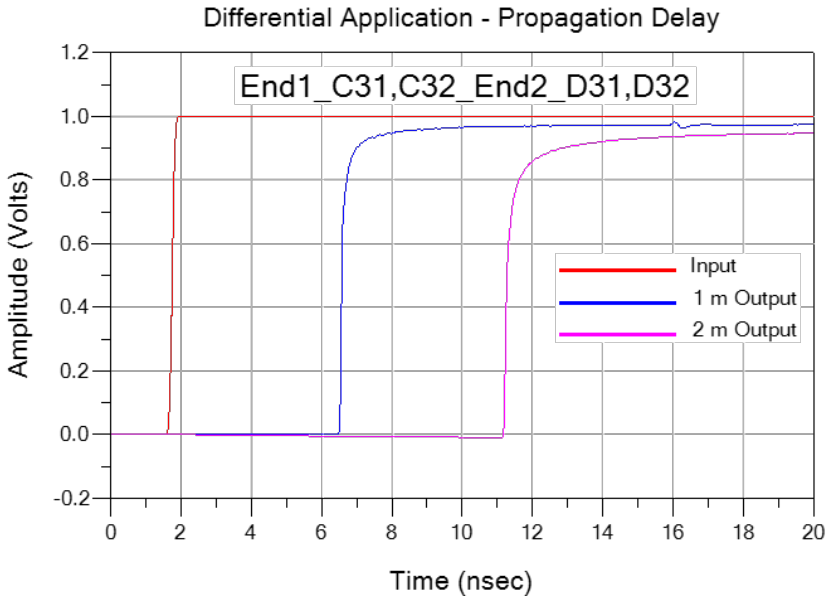



Figure 36

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

# Appendix C – Product and Test System Descriptions

## Product Description

Product test samples are 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assemblies. The part numbers are HDLSP-035-1000 and HDLSP-035-2000. They mate with HDI6-035-01-RA. A photo of the mated test article mounted to SI test boards is shown below.

The cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in Table 3. There are a total of 35 positions per row. SMA jack numbers on the test boards correspond to the assembly line numbers. All adjacent lines are terminated where applicable.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Side A | A1 | A2 | G | A4 | A5 | G | A7 | A8 | G | A10 | A11 | G | A13 | A14 | G | A16 | A17 | G | A19 | A20 | G | A22 | A23 | G | A25 | A26 | G | A28 | A29 | G | A31 | A32 | G | A34 | A35 |
| Side B | B1 | B2 | G | B4 | B5 | G | B7 | B8 | G | B10 | B11 | G | B13 | B14 | G | B16 | B17 | G | B19 | B20 | G | B22 | B23 | G | B25 | B26 | G | B28 | B29 | G | B31 | B32 | G | B34 | B35 |

Table 3: Respective signal line numbers as viewed from End 1

## Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Four test fixtures are specific to HDLSP series cable assembly and identified by part numbers PCB-109922-SIG-02 to PCB-109922-05. The Auto Fixture Removal (AFR) calibration structures designed specifically for the HDLSP series are located on the same boards. Displayed on the following pages is the information for the HDLSP and AFR calibration structure and directives for the mating HDLSP fixtures.

## PCB-109922-SIG-XX Test Fixtures

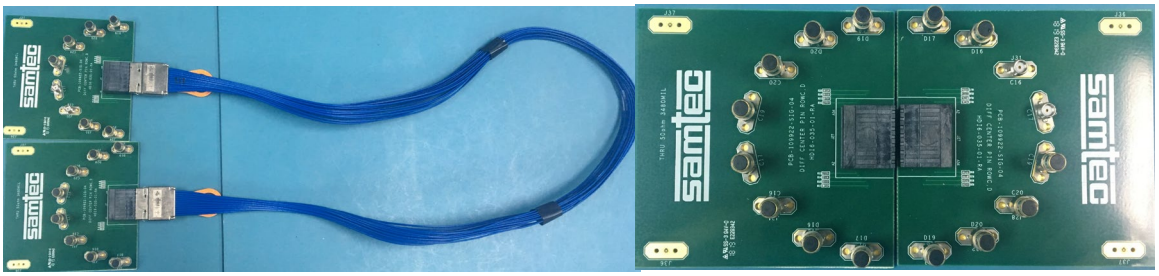


Figure 37

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

Artwork of the PCB design is shown below.

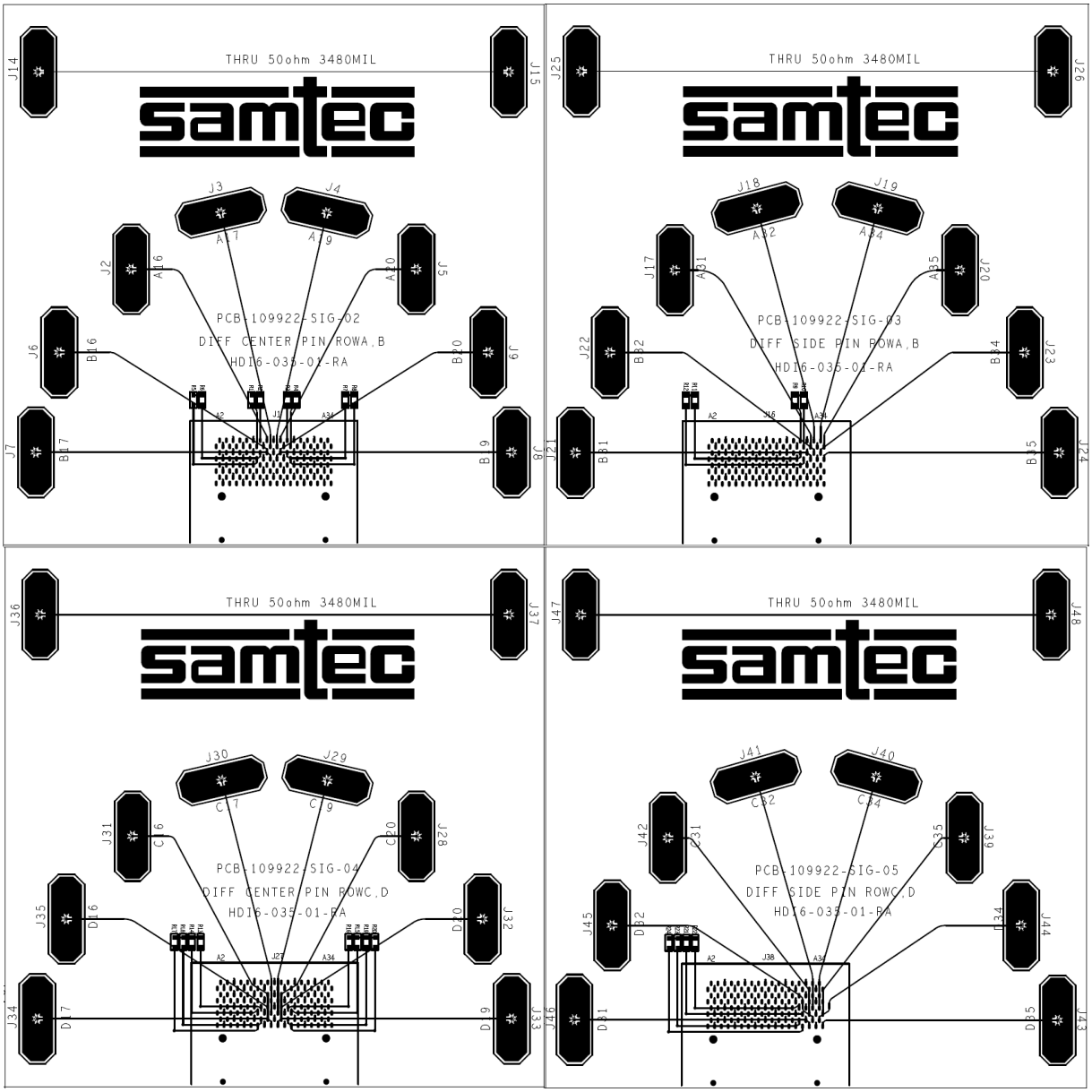



Figure 38

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## PCB Fixtures

The test fixtures used are as follows:

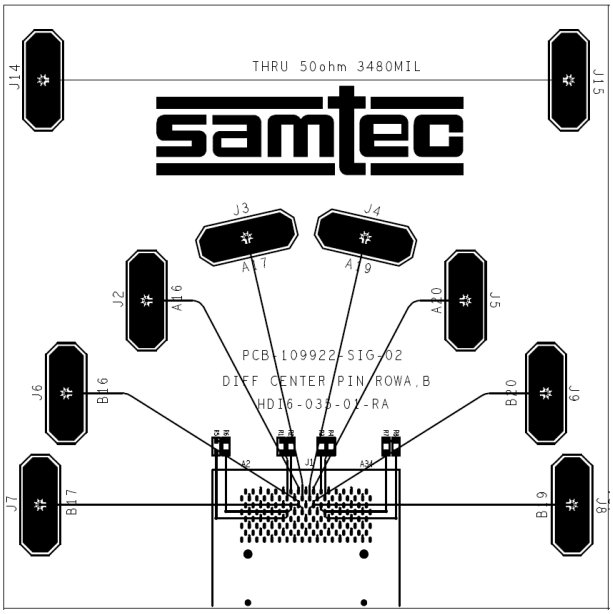



Figure 39

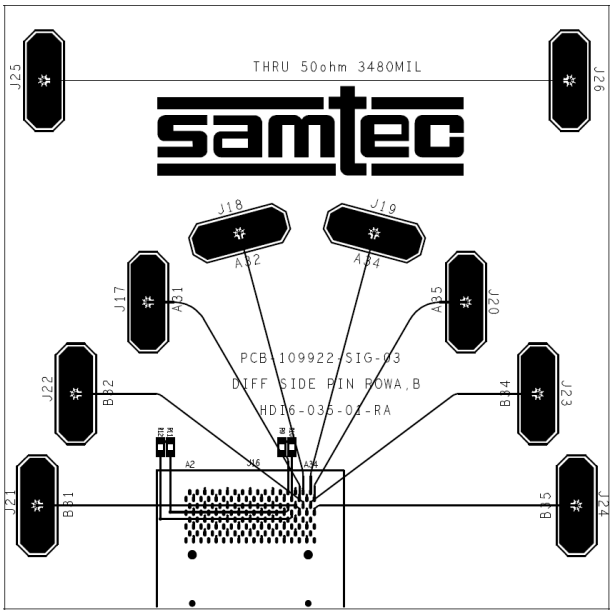



Figure 40

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

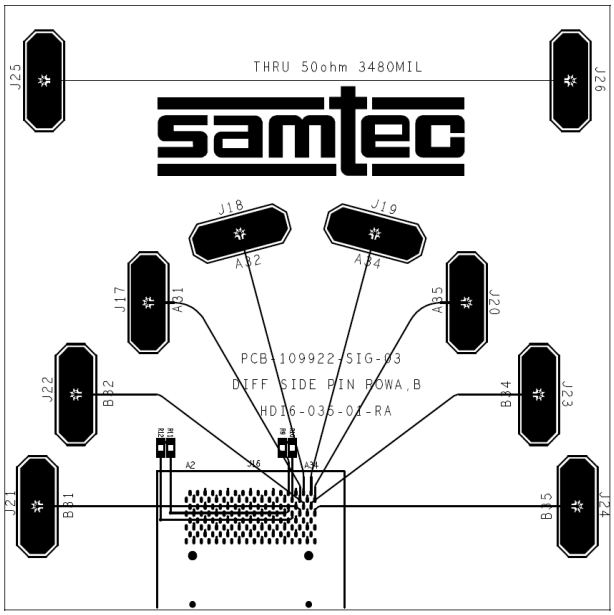



Figure 41

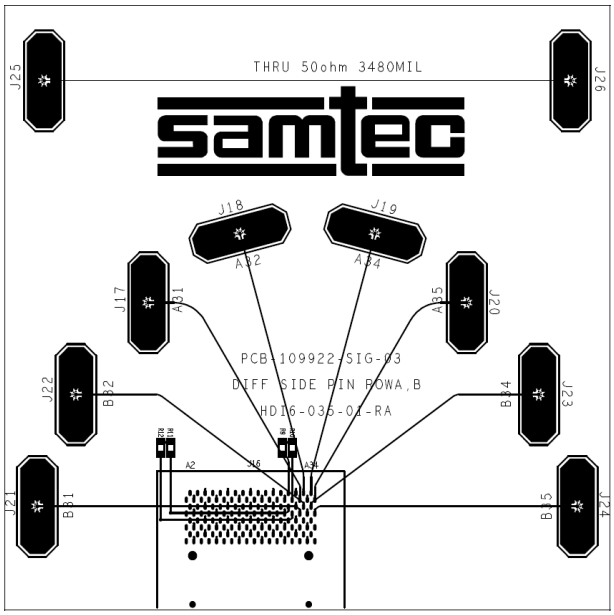



Figure 42

PCB-109922-SIG-02 – Differential Center Pin for Row A,B
PCB-109922-SIG-03 – Differential Side Pin for Row A,B
PCB-109922-SIG-04 – Differential Center Pin for Row C,D
PCB-109922-SIG-05 – Differential Side Pin for Row C,D

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are extracted from the instrument by AFR application. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

| | |
|---|---|
| Start Frequency – 300 KHz | Number of points -1601 |
| Stop Frequency – 20 GHz | IFBW – 1 KHz |

With these settings, the measurement time is approximately 20 seconds.

### N5230C Measurement Setup

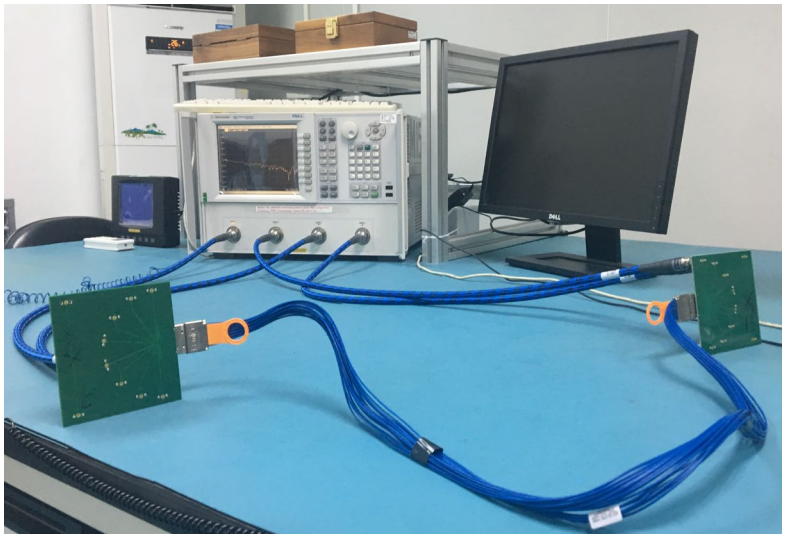


Figure 43

### Test Instruments

| QTY | Description |
|---|---|
| 1 | Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz) |
| 1 | Agilent N4433A ECAL Module (300 KHz to 20 GHz) |

### Test Cables & Adapters

| QTY | Description |
|---|---|
| 4 | Gore OWD01D02039-4 (DC-26.5 GHz) |

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale: 10 ohm / Div
Offset: Default / Scroll
Horizontal Scale: 2ns/ Div
Record Length: 4000
Averages: ≥ 16

**DSA8200 Measurement Setup**

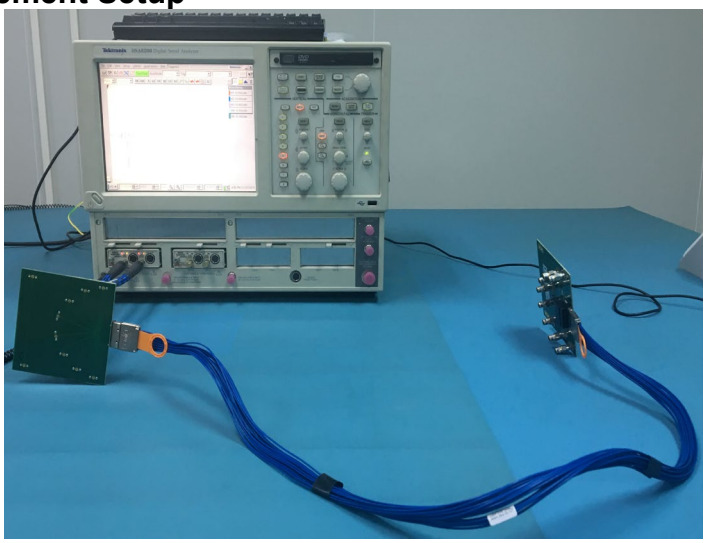


Figure 44

**Test Instruments**

| QTY | Description |
|---|---|
| 1 | Tektronix DSA8200 Digital Serial Analyzer |
| 2 | Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module |

**Test Cables & Adapters**

| QTY | Description |
|---|---|
| 2 | JUNFLON- MWX-021-0025DMSDMS/B (DC-20 GHz) |

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

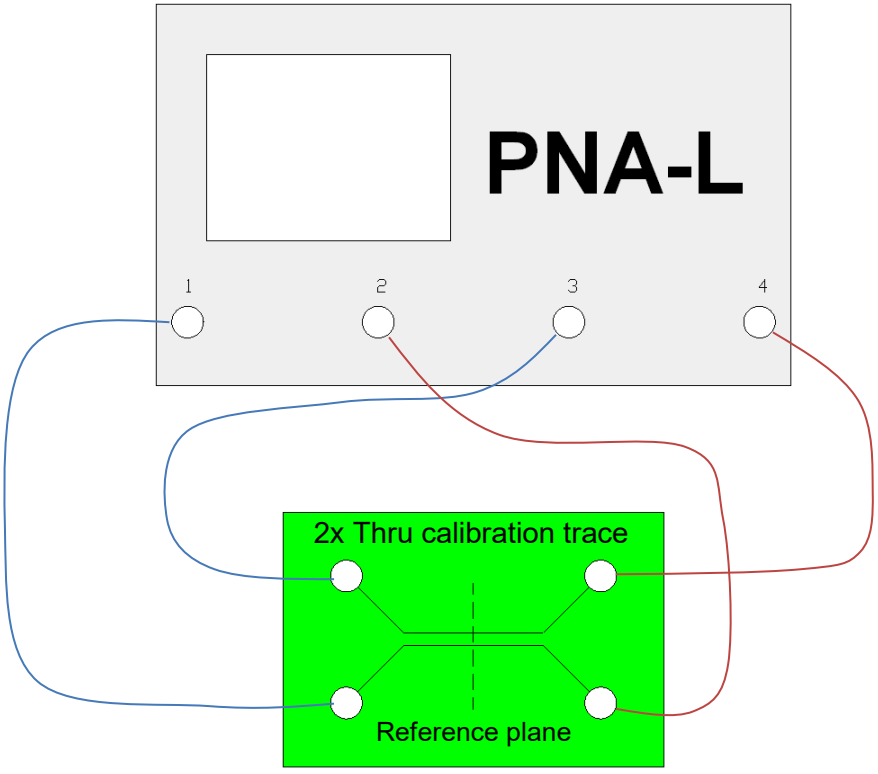
# Appendix E - Frequency and Time Domain Measurements

## Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-CAL module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the HDLSP test boards, this is greater than 20 GHz.

The figure below shows how the 2X THRU reference traces is utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2X THRU.



**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with band-width-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2017 update 1. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://suddendocs.samtec.com/notesandwhitepapers/tech-note_using-plts-for-time-domain-data_web.pdf

### Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same figure. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

### Impedance (TDR)

Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

**Series:** HDLSP
**Description:** 0.635 mm Eye Speed® HD High-Speed High-Density I/O Cable Assembly

## Appendix F – Glossary of Terms

ADS – Keysight Advanced Design System
AFR – Automatic Fixture Removal
PCB – Printed Circuit Board
SUT – System Under Test
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
XROW – Across Row