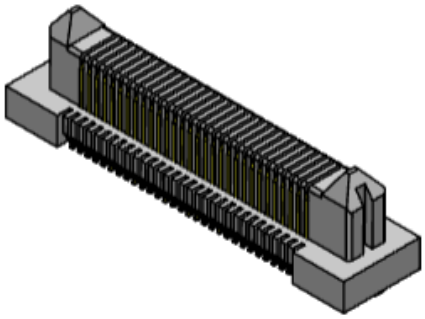
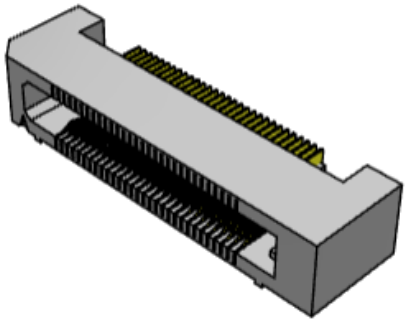
High Speed Characterization Report

ERM5-XXX-02.0-X-DV-X-X



ERF5-XXX-X-X-X-RA-X



Description:
0.50 mm Edge Rate® Rugged High-Speed Interconnect, ERM5 Terminal mating to ERF5 Right-Angle Socket

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Report Revision: 01/07/2022

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

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Connector Overview

The ERM5/ERF5 is a board-mounted interconnect designed for use in high-speed systems. The ERx5 uses the Edge Rate® contact system which is designed for applications requiring high-mating cycles and 28 Gbps performance. The ERF5-RA Right-Angle Series is available in 10, 20, 30, 40 and 50 positions per row. The data in this report is applicable to the ERM5 mated to ERF5 Right-Angle connector.

Frequency Domain Data Summary

Bandwidth Chart – Single-Ended Insertion Loss

ERM5_ERF5-RA Connector Series – Short Row

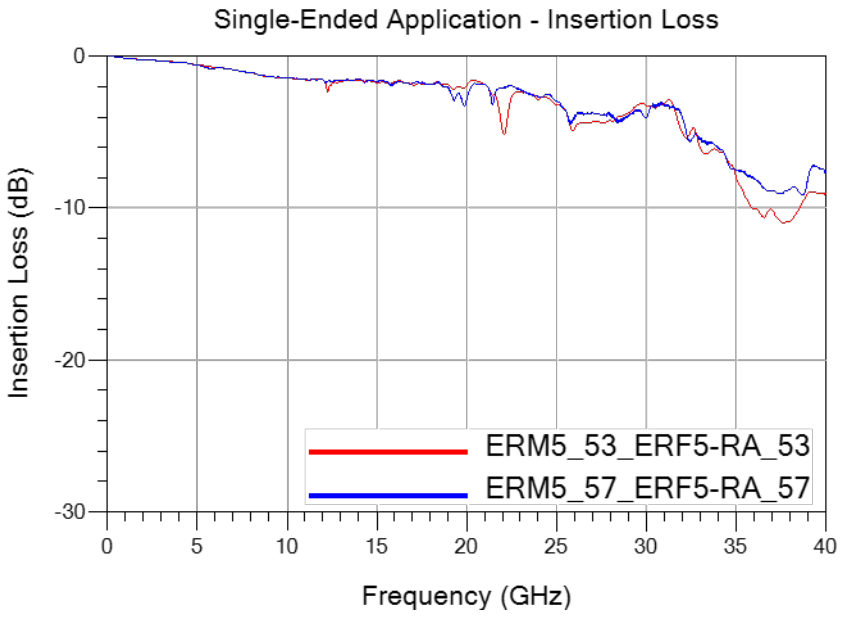

Figure 1

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

ERM5_ERF5-RA Connector Series – Long Row

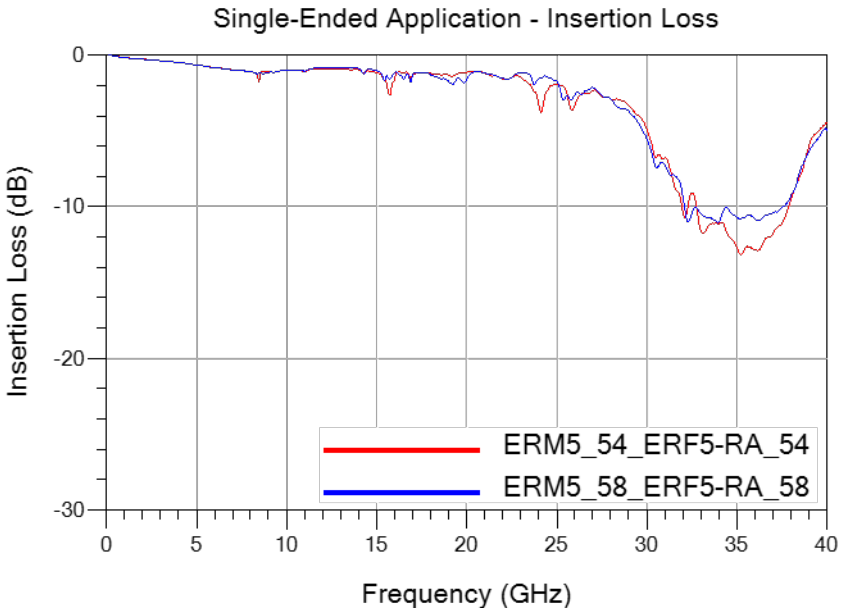

Figure 2

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Bandwidth Chart – Differential Insertion Loss

ERM5_ERF5-RA Connector Series – Short Row

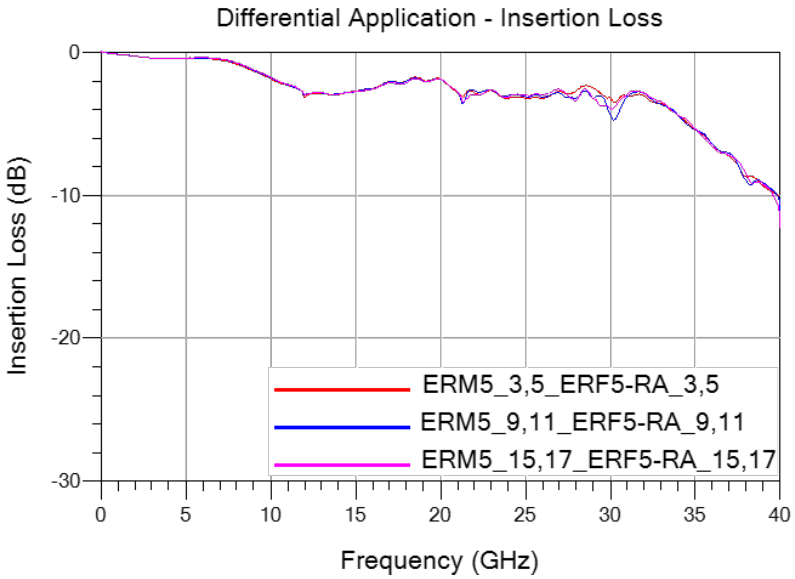

Figure 3

ERM5_ERF5-RA Connector Series – Long Row

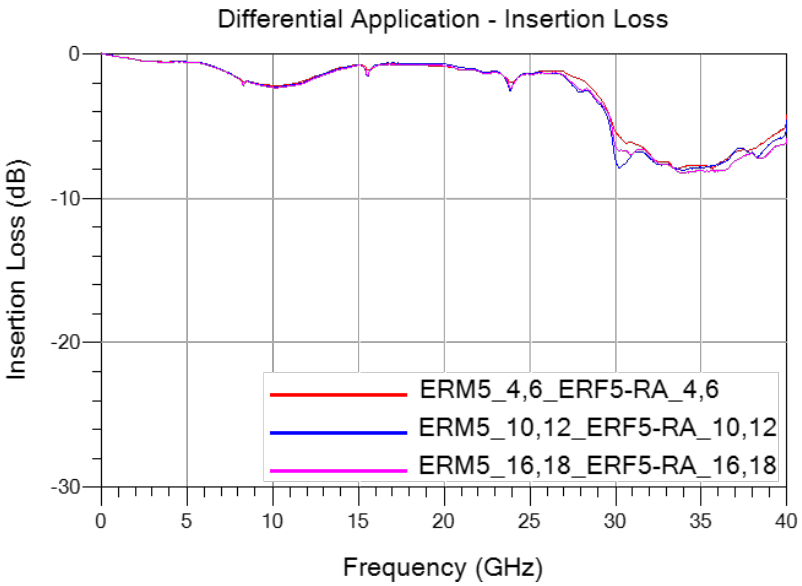

Figure 4

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Time Domain Data Summary

Table 1 – Single-Ended Impedance (Ω)				
Driver	**Signal Rise-time**	**30ps**	**50ps**	**100ps**
ERM5_53	Maximum Impedance	61.8	56.7	52.8
	Minimum Impedance	46.7	49.2	49.9
ERM5_54	Maximum Impedance	63.3	58.5	53.9
	Minimum Impedance	47.3	48.9	50.0
ERM5_57	Maximum Impedance	62.4	57.3	53.2
	Minimum Impedance	47.1	49.5	50.0
ERM5_58	Maximum Impedance	63.8	58.9	54.2
	Minimum Impedance	47.5	49.1	50.0

Table 2 - Differential Impedance (Ω)				
Driver	**Signal Rise-time**	**30ps**	**50ps**	**100ps**
ERM5_3,5	Maximum Impedance	103.0	101.9	101.5
	Minimum Impedance	74.7	81.9	86.7
ERM5_4,6	Maximum Impedance	103.3	102.1	101.7
	Minimum Impedance	74.4	81.5	86.1
ERM5_9,11	Maximum Impedance	103.3	102.2	101.7
	Minimum Impedance	74.7	81.7	86.2
ERM5_10,12	Maximum Impedance	103.1	102.2	101.7
	Minimum Impedance	68.8	75.3	82.9
ERM5_15,17	Maximum Impedance	103.2	102.3	101.8
	Minimum Impedance	68.9	75.5	82.8
ERM5_16,18	Maximum Impedance	103.2	102.2	101.7
	Minimum Impedance	68.7	75.3	82.8

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Table 3 – Single Ended Crosstalk (%)					
Input(tr)	**Driver**	**Receiver**	**30ps**	**50ps**	**100ps**
NEXT	ERM5_53	ERM5_54	0.44	0.40	0.29
	ERM5_53	ERM5_57	2.50	2.11	1.37
	ERM5_53	ERM5_58	0.37	0.35	0.24
	ERM5_54	ERM5_58	2.74	2.37	1.70
	ERM5_57	ERM5_58	0.59	0.55	0.39
FEXT	ERM5_53	ERF5-RA_54	0.19	0.12	<0.1
	ERM5_53	ERF5-RA_57	1.47	1.07	0.64
	ERM5_53	ERF5-RA_58	0.22	0.15	0.11
	ERM5_54	ERF5-RA_58	1.37	0.92	0.56
	ERM5_57	ERF5-RA_58	0.26	0.18	0.14

Table 4 - Differential Crosstalk (%)					
Input(tr)	**Driver**	**Receiver**	**30ps**	**50ps**	**100ps**
NEXT	ERM5_4,6	ERM5_3,5	<0.1	<0.1	<0.1
	ERM5_4,6	ERM5_9,11	<0.1	<0.1	<0.1
	ERM5_4,6	ERM5_10,12	0.44	0.38	0.27
	ERM5_4,6	ERM5_16,18	<0.1	<0.1	<0.1
	ERM5_10,12	ERM5_16,18	0.43	0.37	0.26
	ERM5_15,17	ERM5_3,5	<0.1	<0.1	<0.1
	ERM5_15,17	ERM5_4,6	<0.1	<0.1	<0.1
	ERM5_15,17	ERM5_9,11	0.40	0.34	0.23
	ERM5_15,17	ERM5_10,12	<0.1	<0.1	<0.1
	ERM5_15,17	ERM5_16,18	<0.1	<0.1	<0.1
FEXT	ERM5_4,6	ERF5-RA_3,5	<0.1	<0.1	<0.1
	ERM5_4,6	ERF5-RA_9,11	<0.1	<0.1	<0.1
	ERM5_4,6	ERF5-RA_10,12	0.13	<0.1	<0.1
	ERM5_4,6	ERF5-RA_16,18	<0.1	<0.1	<0.1
	ERM5_10,12	ERF5-RA_16,18	0.14	<0.1	<0.1
	ERM5_15,17	ERF5-RA_3,5	<0.1	<0.1	<0.1
	ERM5_15,17	ERF5-RA_4,6	<0.1	<0.1	<0.1
	ERM5_15,17	ERF5-RA_9,11	0.13	<0.1	<0.1
	ERM5_15,17	ERF5-RA_10,12	<0.1	<0.1	<0.1
	ERM5_15,17	ERF5-RA_16,18	<0.1	<0.1	<0.1

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Table 5 - Propagation Delay (Mated Connector)	
ERM5_53_ERF5-RA_53	80 ps
ERM5_54_ERF5-RA_54	96 ps
ERM5_57_ERF5-RA_57	80 ps
ERM5_58_ERF5-RA_58	97 ps
ERM5_3,5_ERF5-RA_3,5	70 ps
ERM5_4,6_ERF5-RA_4,6	87 ps
ERM5_9,11_ERF5-RA_9,11	70 ps
ERM5_10,12_ERF5-RA_10,12	88 ps
ERM5_15,17_ERF5-RA_15,17	69 ps
ERM5_16,18_ERF5-RA_16,18	87 ps

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differentially and single-ended driven scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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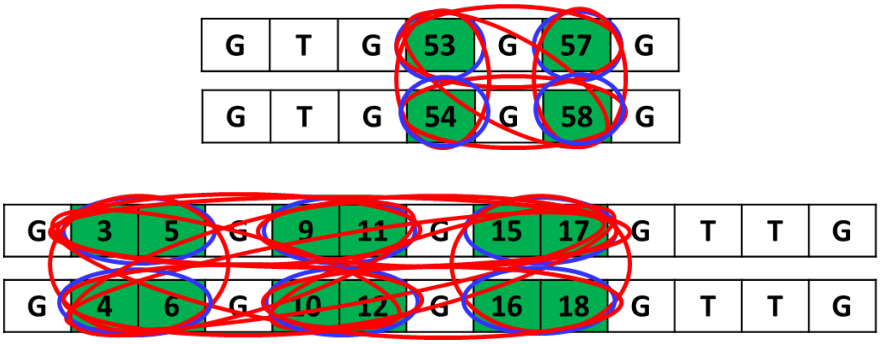
For this connector, the following configurations were evaluated:



Single-Ended and Differential Impedance (denoted by blue circles):

- GSG (Ground-Signal-Ground)
- GSSG (Ground-positive Signal-negative Signal-Ground)

Single-Ended and Differential Crosstalk (denoted by red circles):

- In row: from the terminals to the other terminals on the same row.
- Across row: from one row of terminals to the other row of terminals.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 100 ps.

For this report, measured rise times were at 20%-80% signal levels.

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Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Keysight Advanced Design System to obtain the time domain response. Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 1.9 mm for Single-Ended both ends and 1.95 mm for Differential ERM5, 1.5 mm for Differential ERF5-RA of PCB trace. Delay is measured at 100 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

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Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: ERM5 / ERF5-RA
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Appendix A – Frequency Domain Responses

Single-Ended Application – Insertion Loss

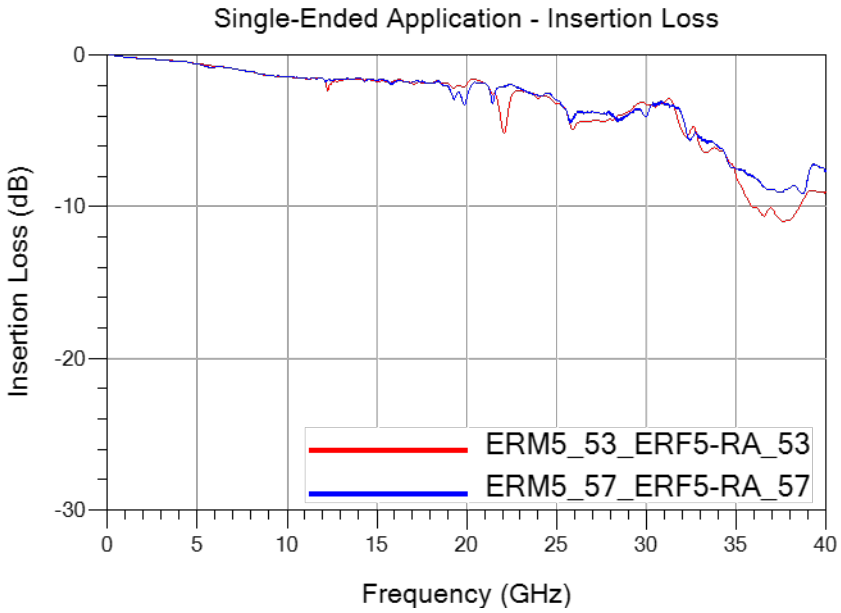

Figure 5

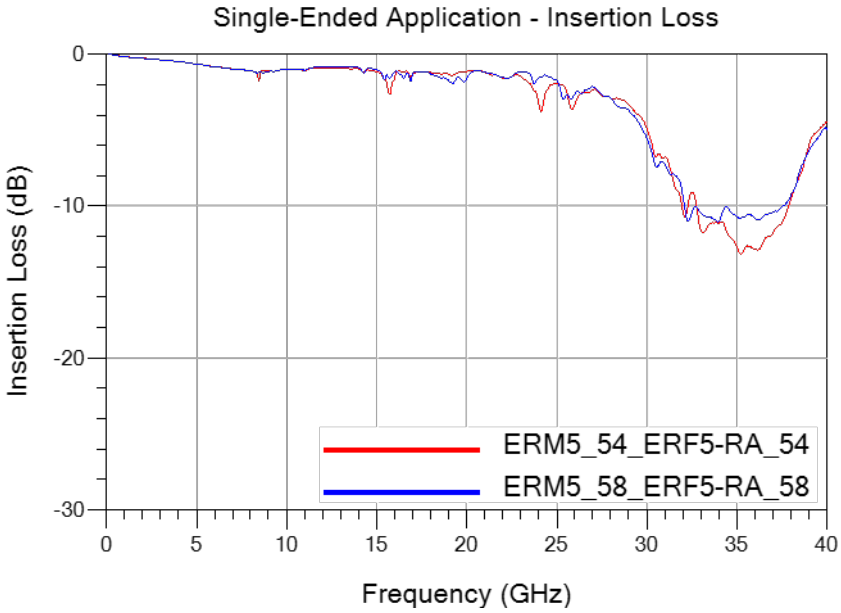

Figure 6

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Single-Ended Application – Return Loss

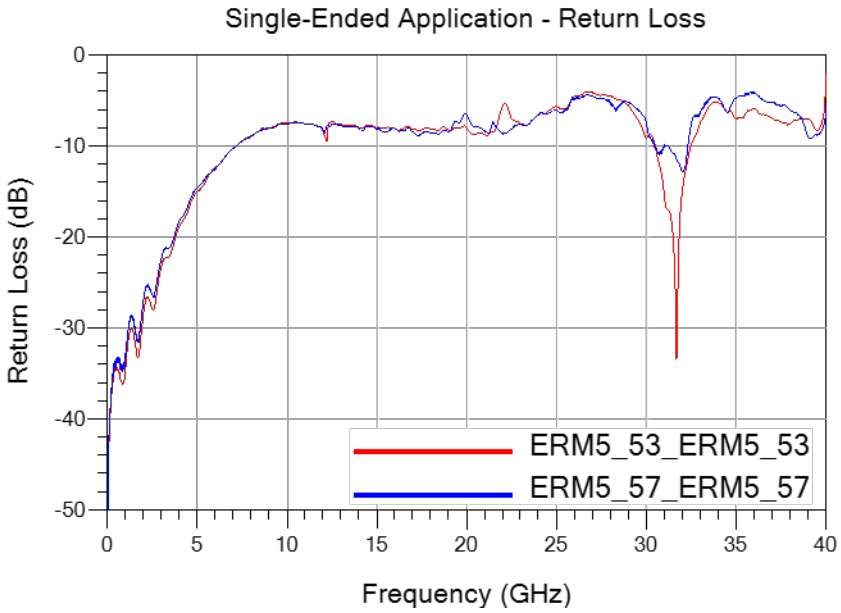

Figure 7

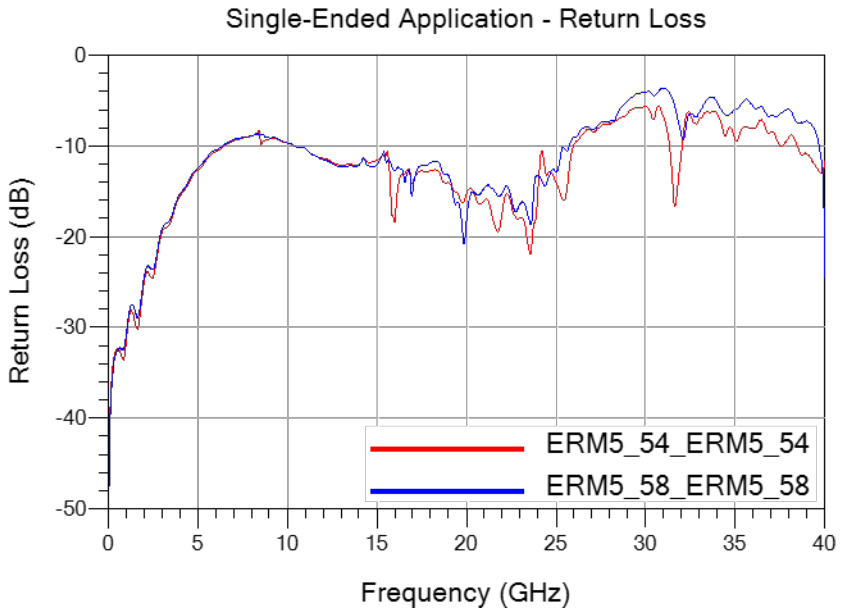

Figure 8

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Single-Ended Application – NEXT Configurations

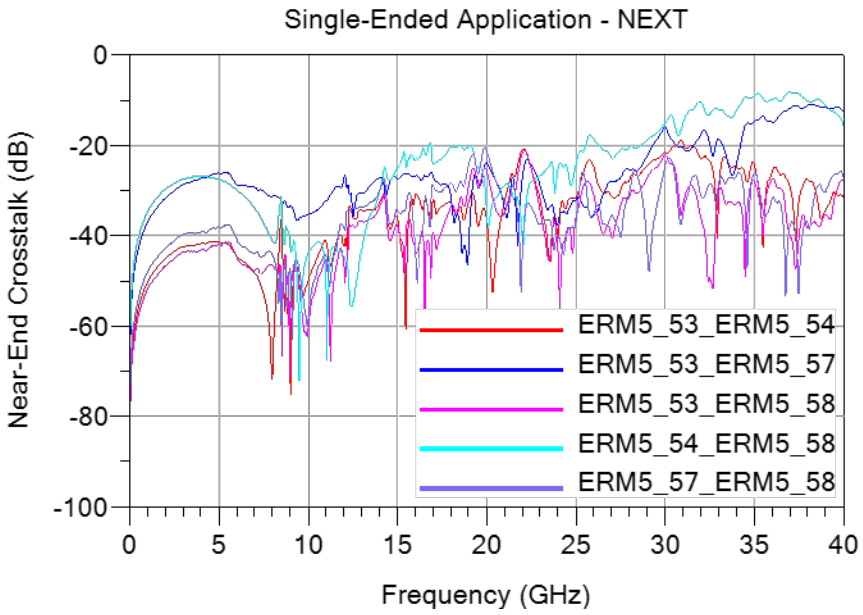

Figure 9

Single-Ended Application – FEXT Configurations

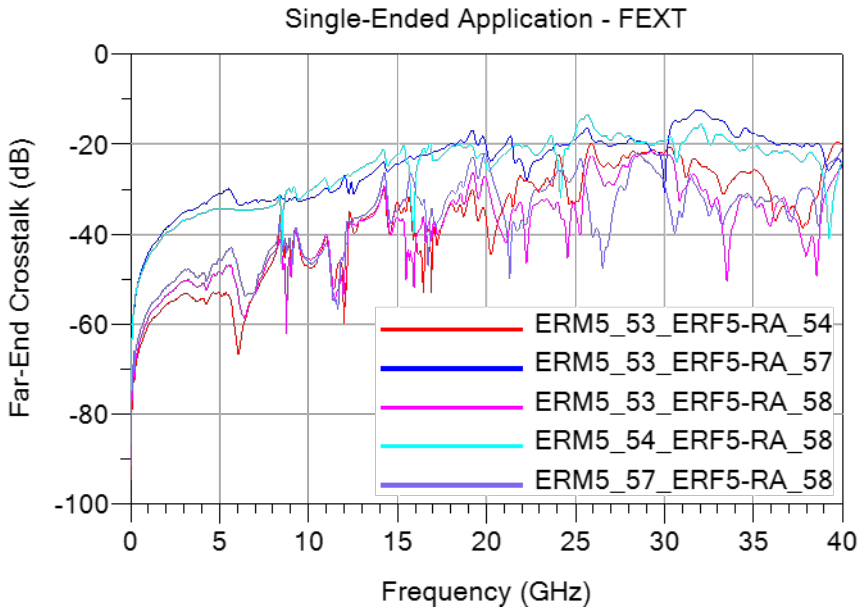

Figure 10

Series: ERM5 / ERF5-RA
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Differential Application – Insertion Loss

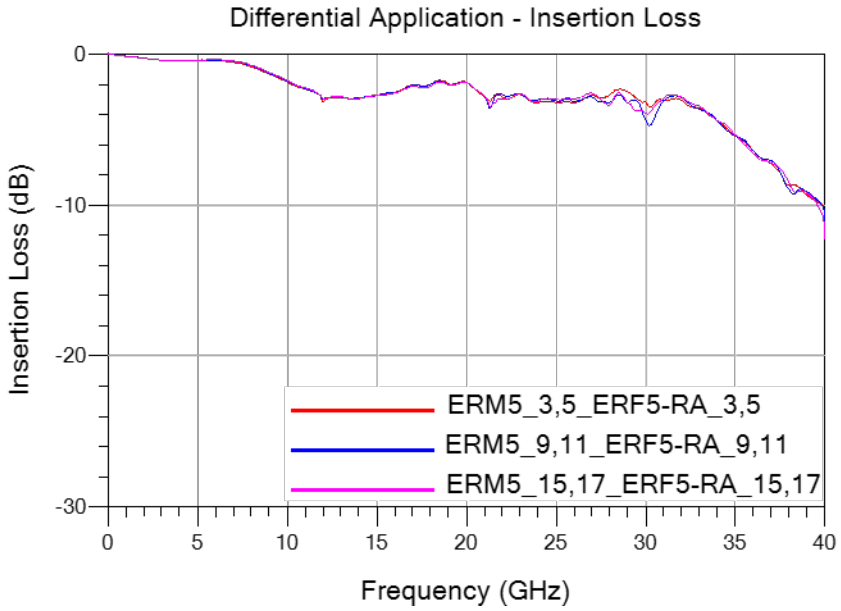

Figure 11

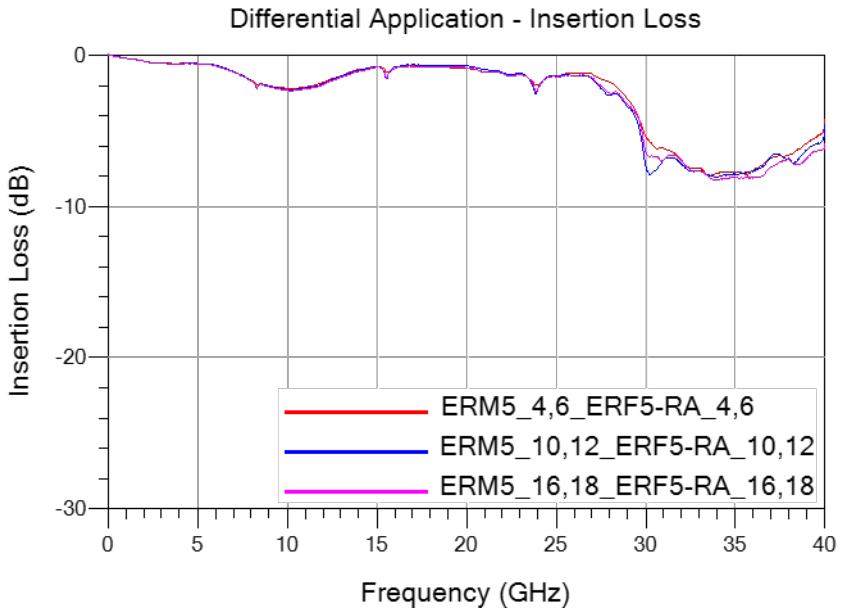

Figure 12

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Differential Application – Return Loss

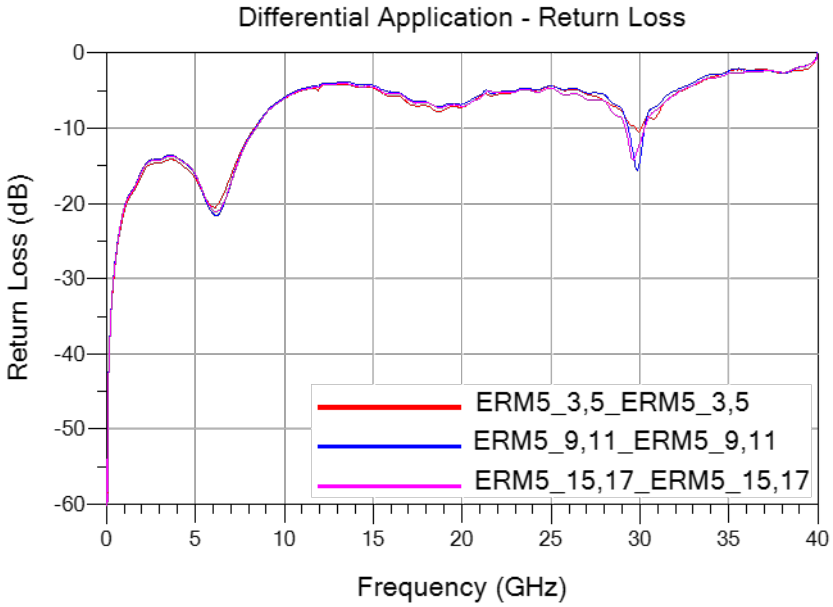

Figure 13

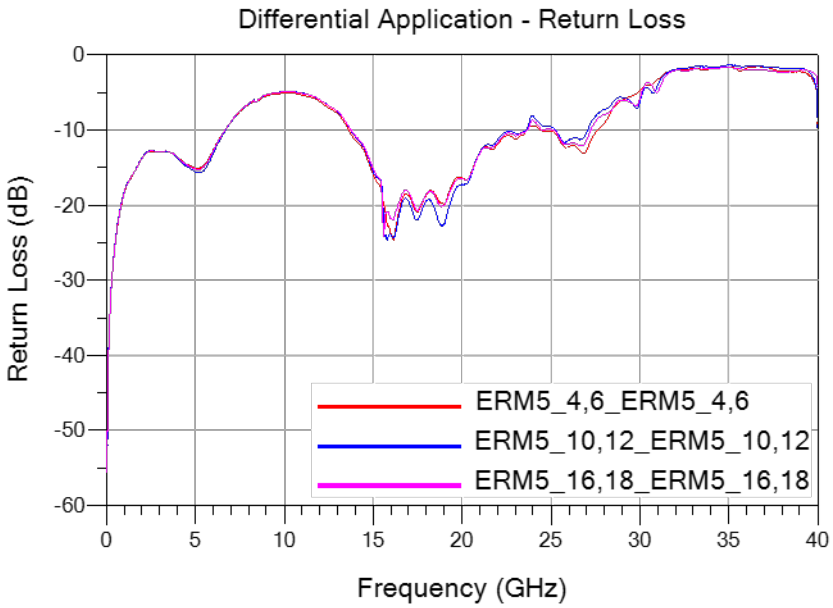

Figure 14

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Differential Application – NEXT Configurations

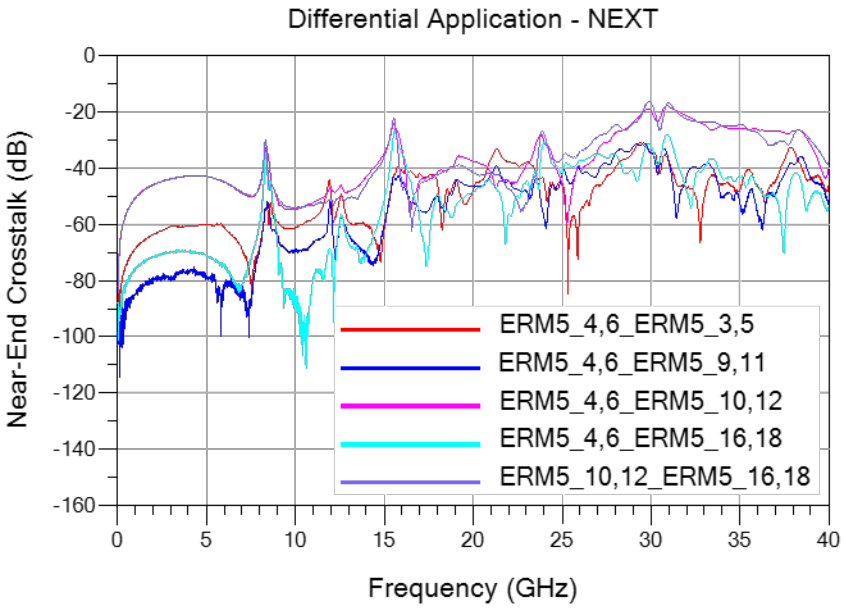

Figure 15

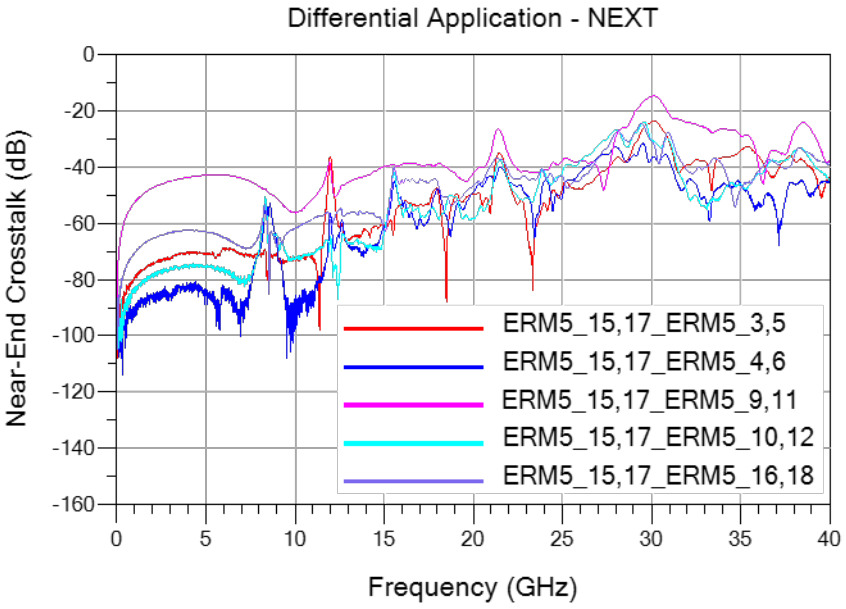

Figure 16

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Differential Application – FEXT Configurations

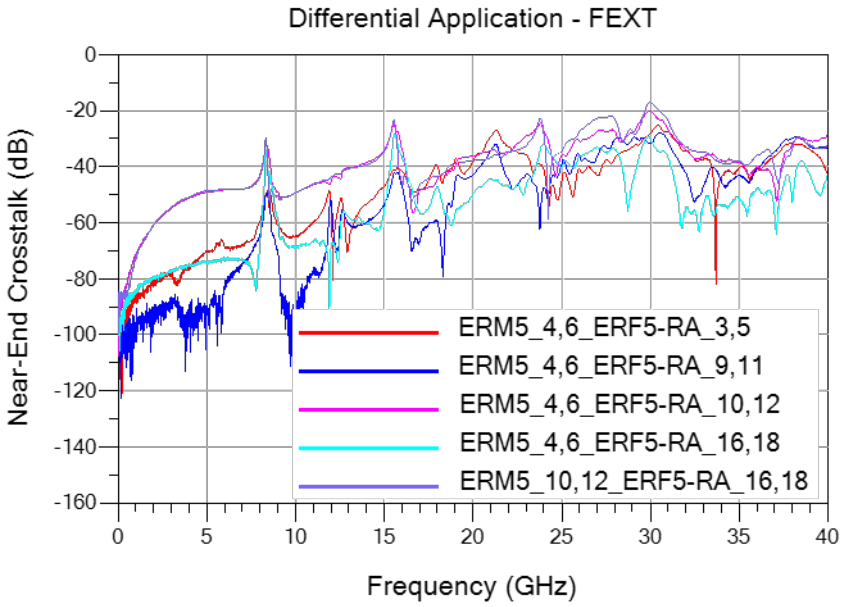

Figure 17

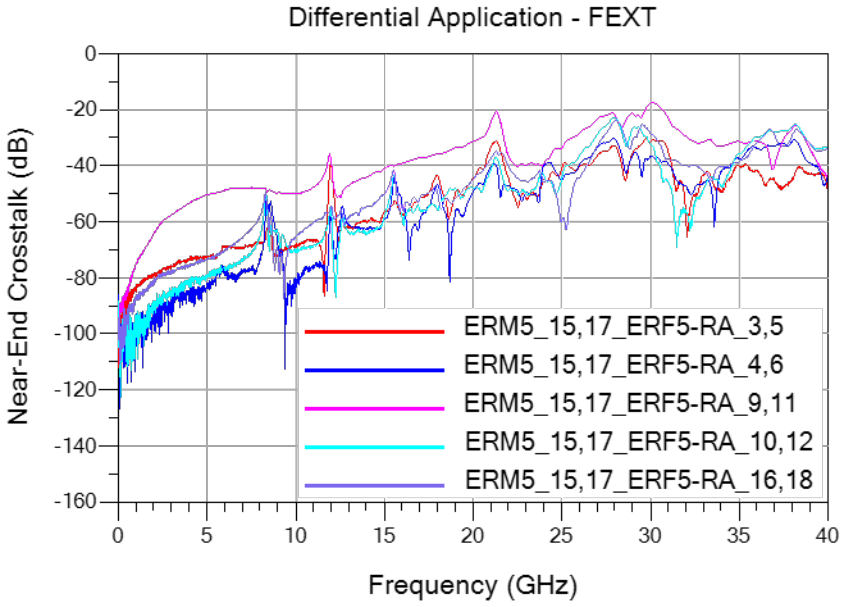

Figure 18

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Appendix B – Time Domain Responses

Single-Ended Application – Impedance

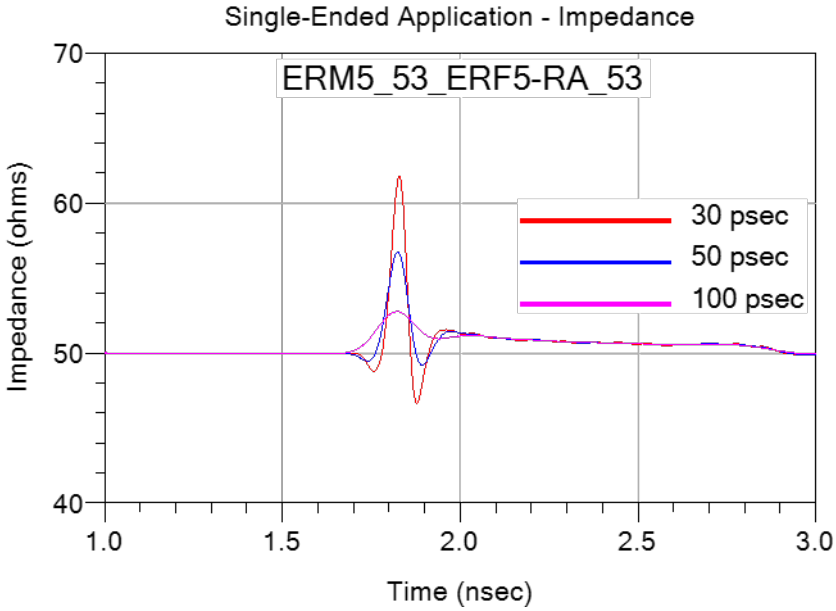

Figure 19

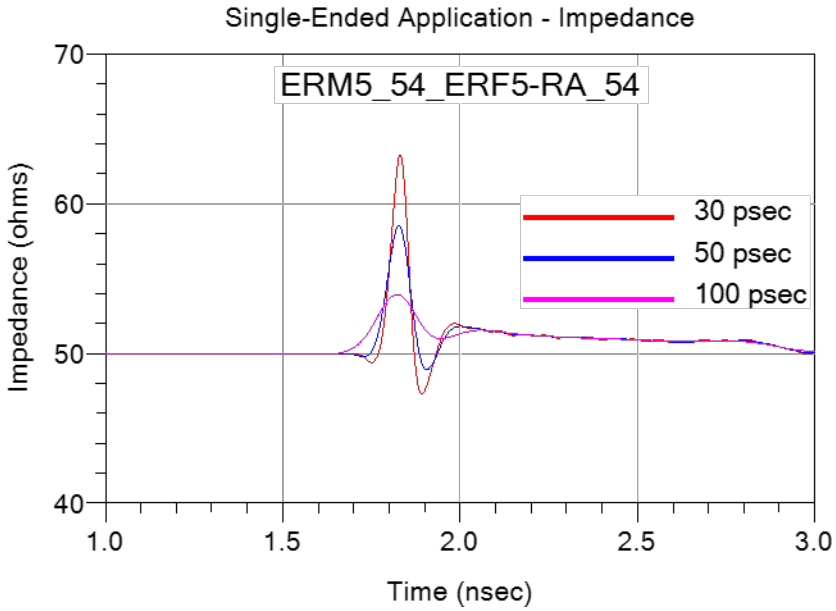

Figure 20

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

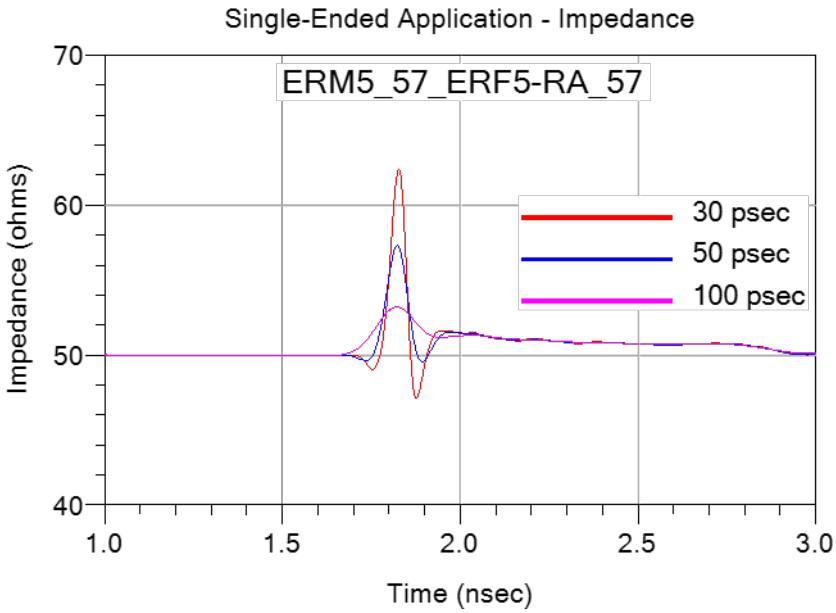

Figure 21

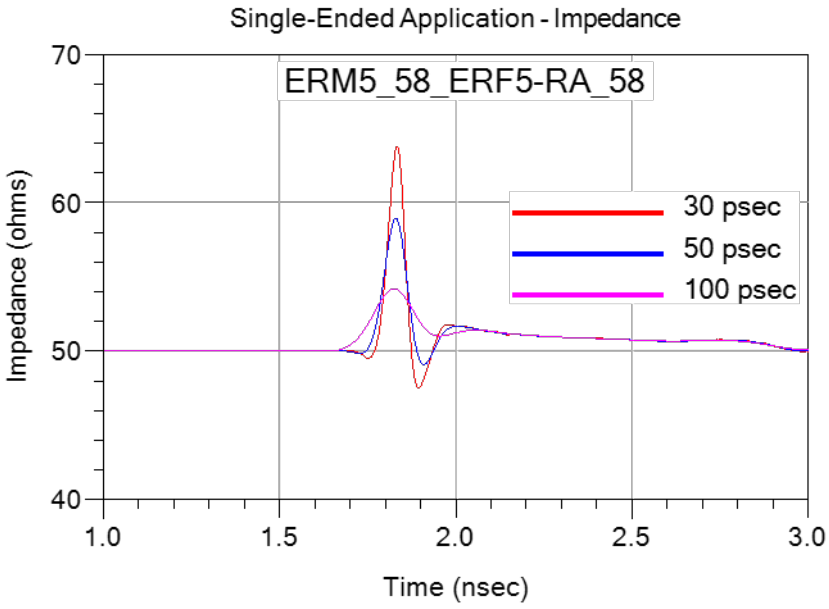

Figure 22

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Single-Ended Application – Propagation Delay

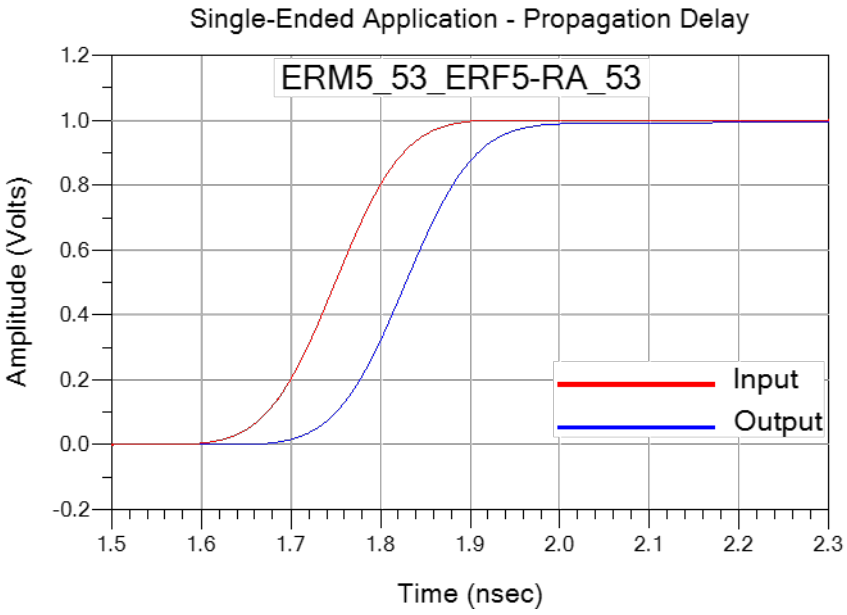

Figure 23

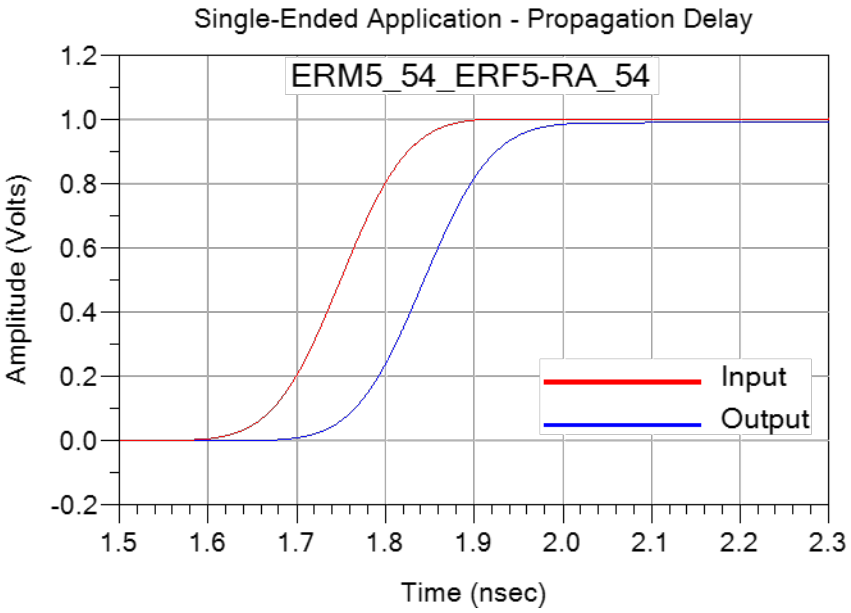

Figure 24

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

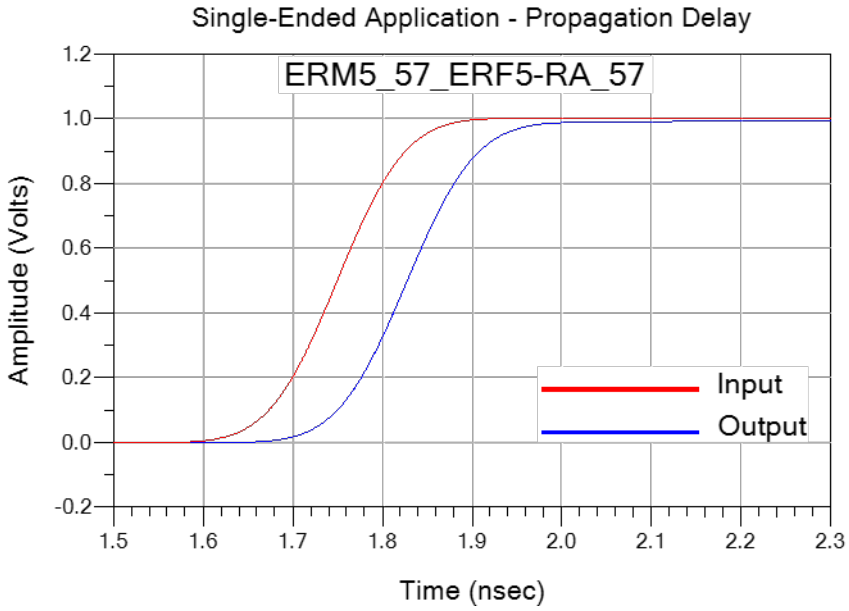

Figure 25

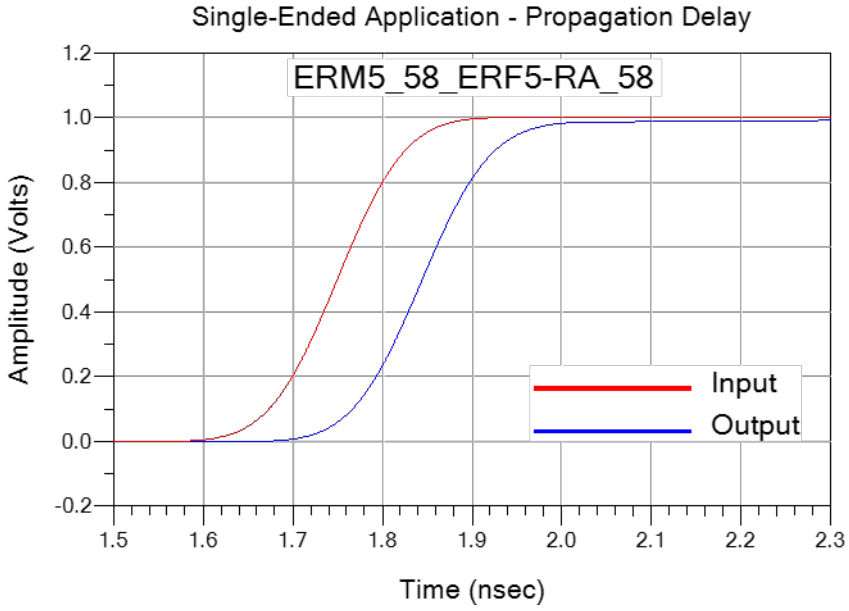

Figure 26

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Differential Application – Impedance

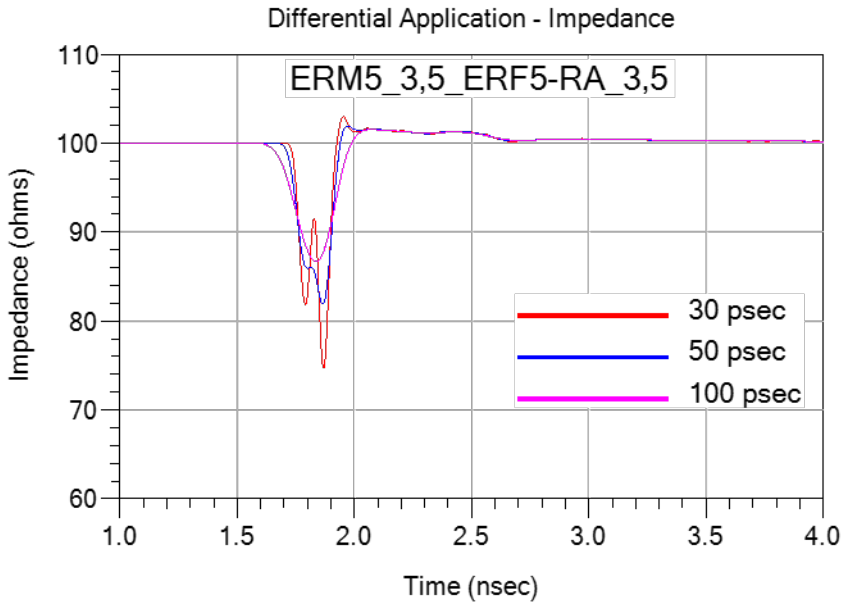

Figure 27

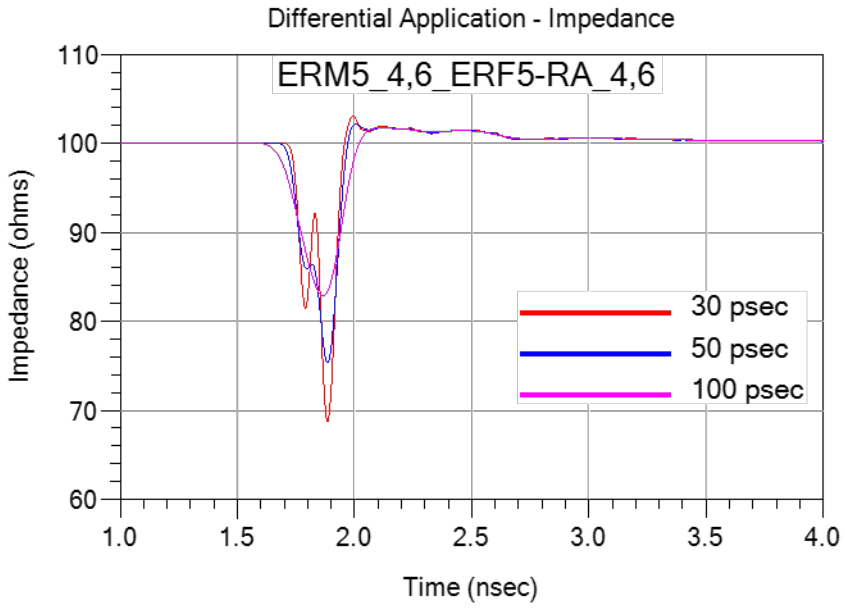

Figure 28

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

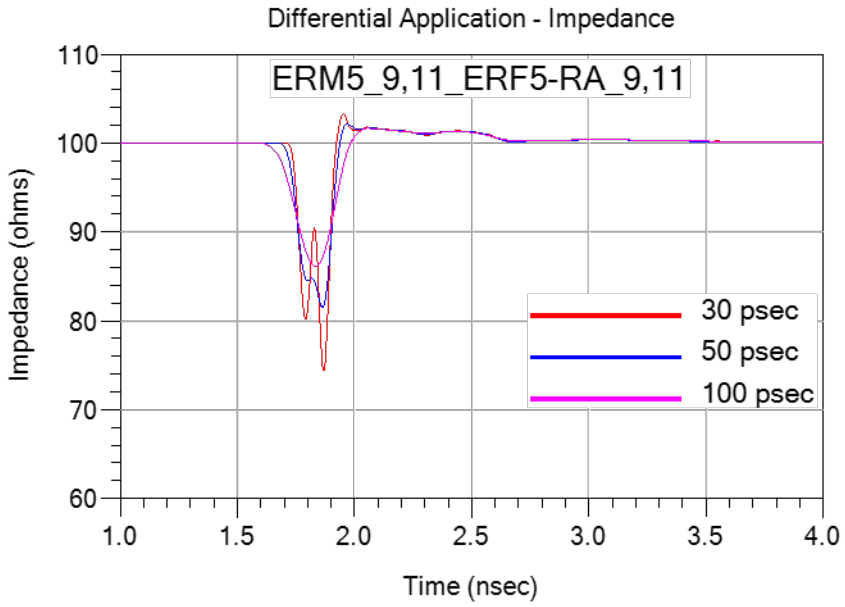

Figure 29

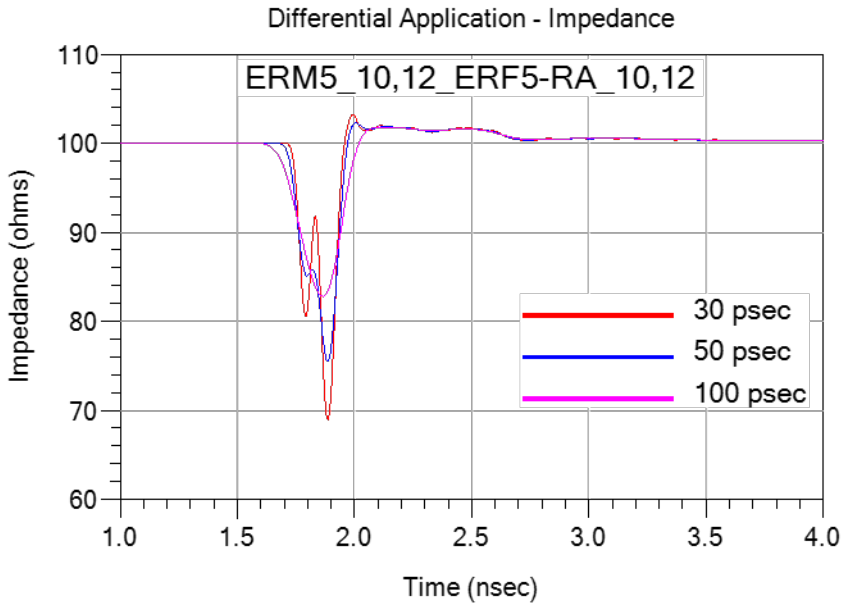

Figure 30

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

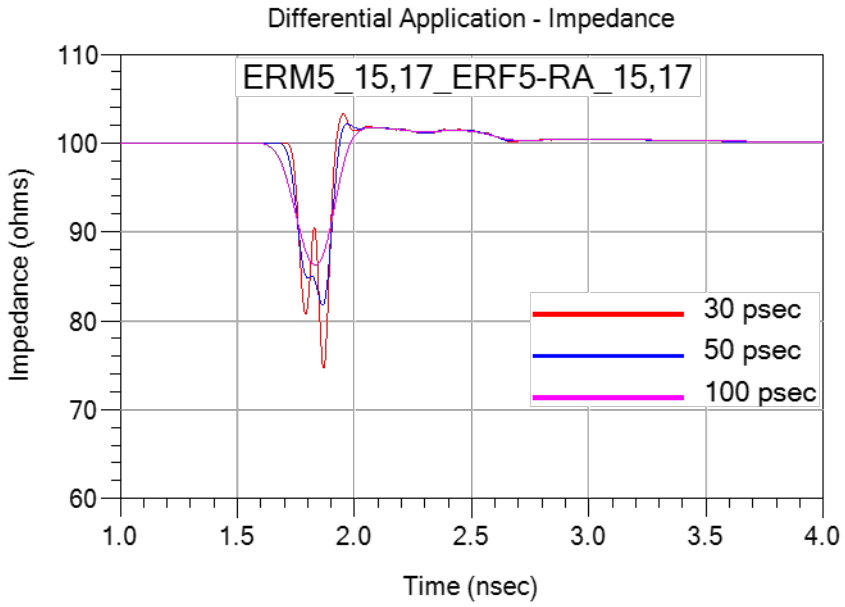

Figure 31

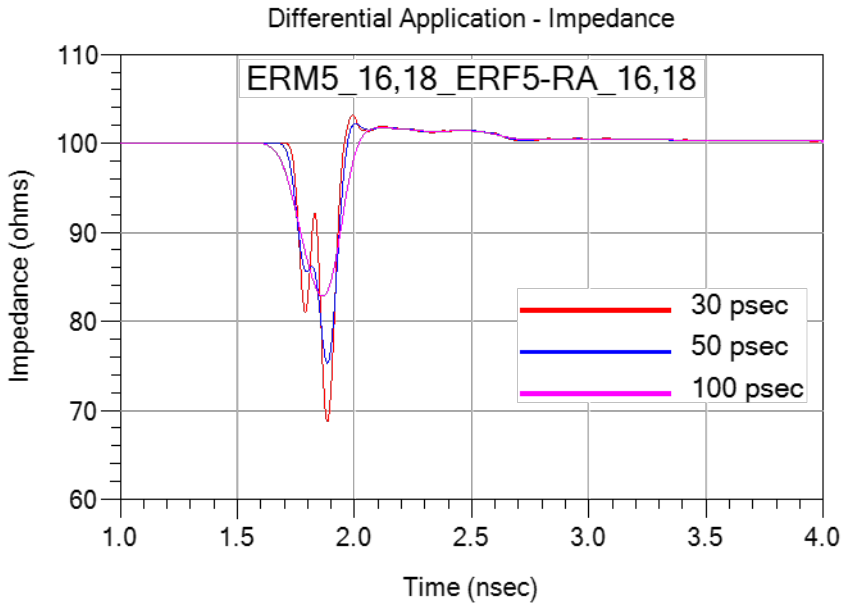

Figure 32

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Differential Application – Propagation Delay

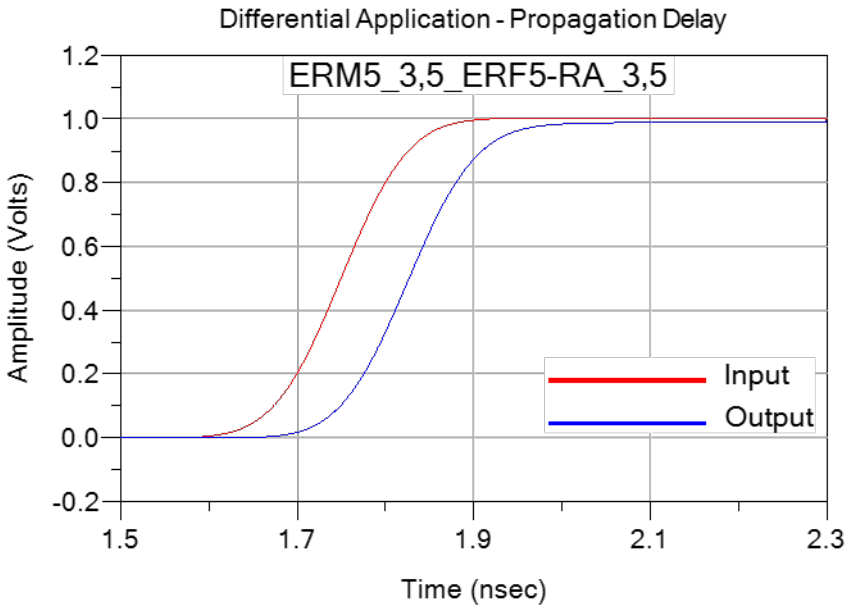

Figure 33

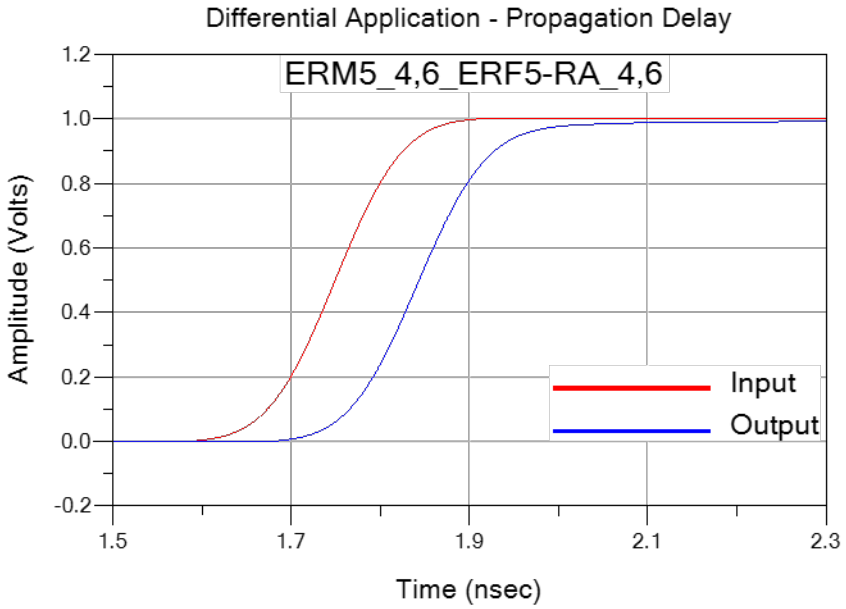

Figure 34

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

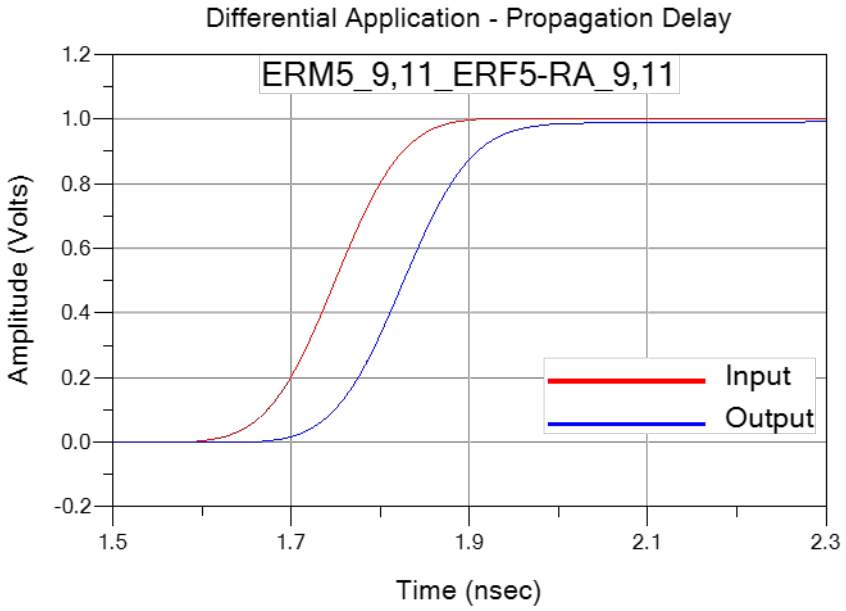

Figure 35

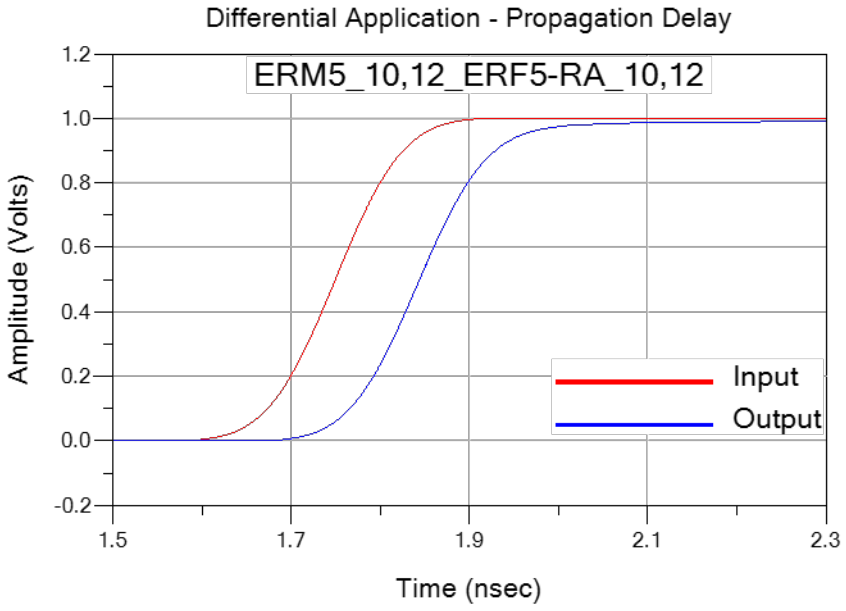

Figure 36

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

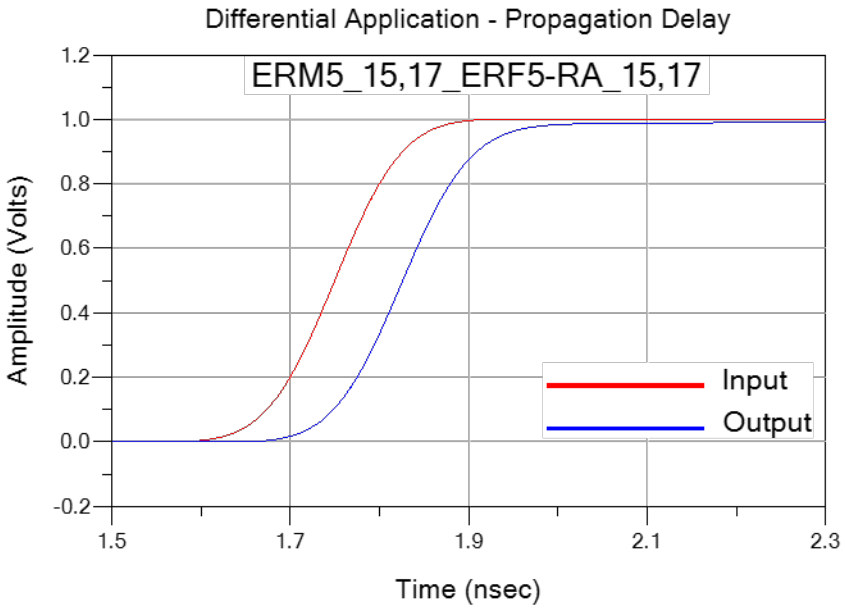

Figure 37

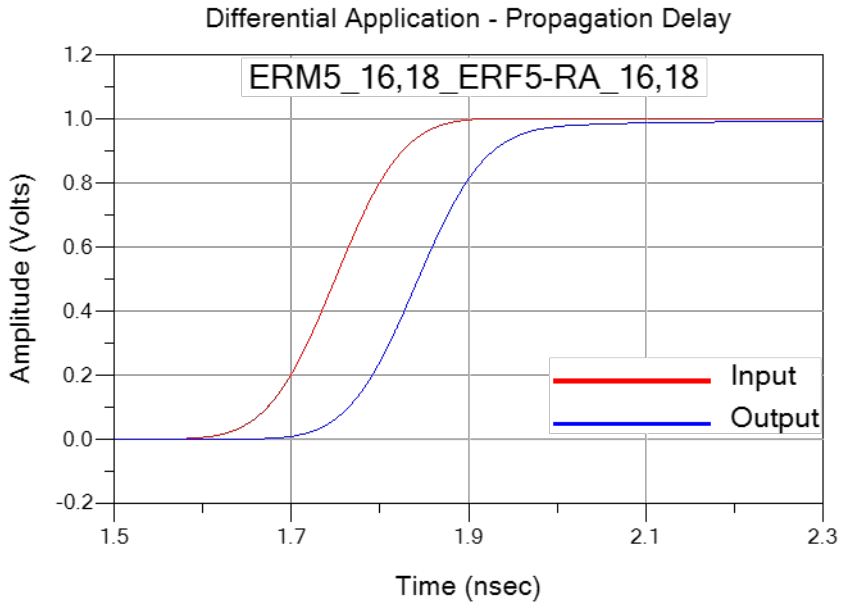

Figure 38

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Appendix C – Product and Test System Descriptions

Product Description

Product test samples are ERx5 Series connectors. The part number is ERM5-030-02.0-L-DV-X-X and ERF5-030-01-L-D-RA-X. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of six-layer MT40 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount 2.4mm connector is used to interface the PNA test cables to the test fixtures. Optimization of the 2.4mm launch was performed using full wave simulation tools to minimize reflections. The test fixtures and calibration kit are specific to the ERx5 series connector set and identified by part number PNL-ERX5-111301-SIG-0.

PNL-ERX5-111301-SIG-0 Test Fixtures

Shown below is photograph of the test board set.

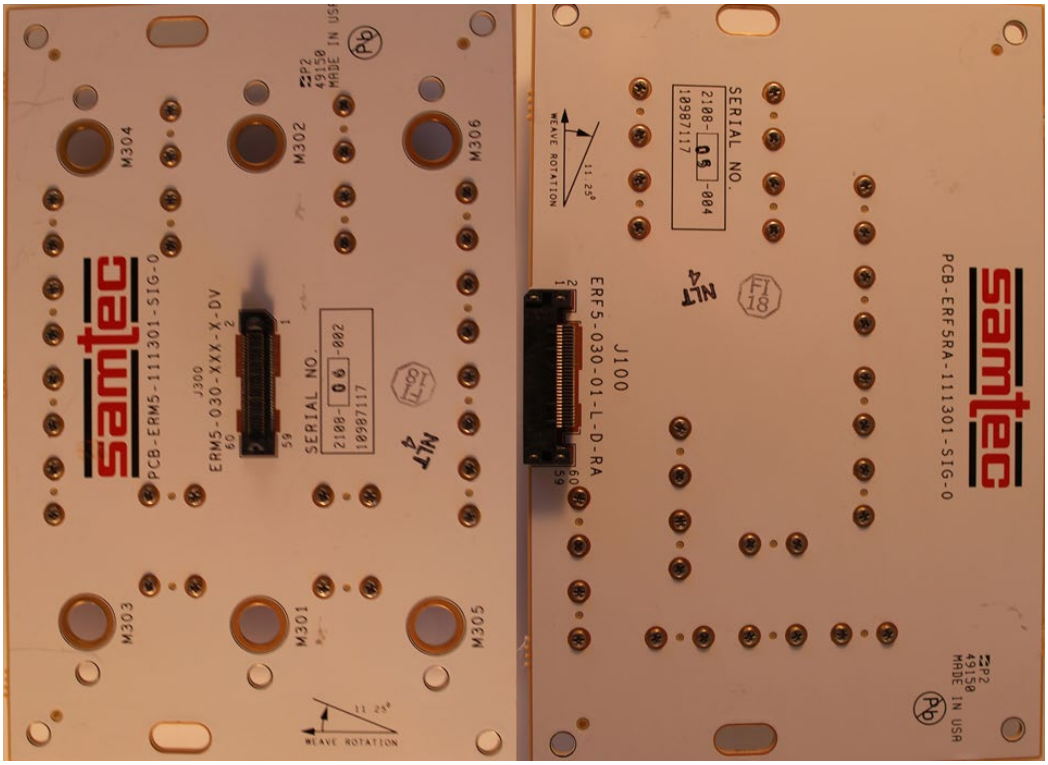

Figure 39

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

PCB Fixtures

The test fixtures used are as follows:

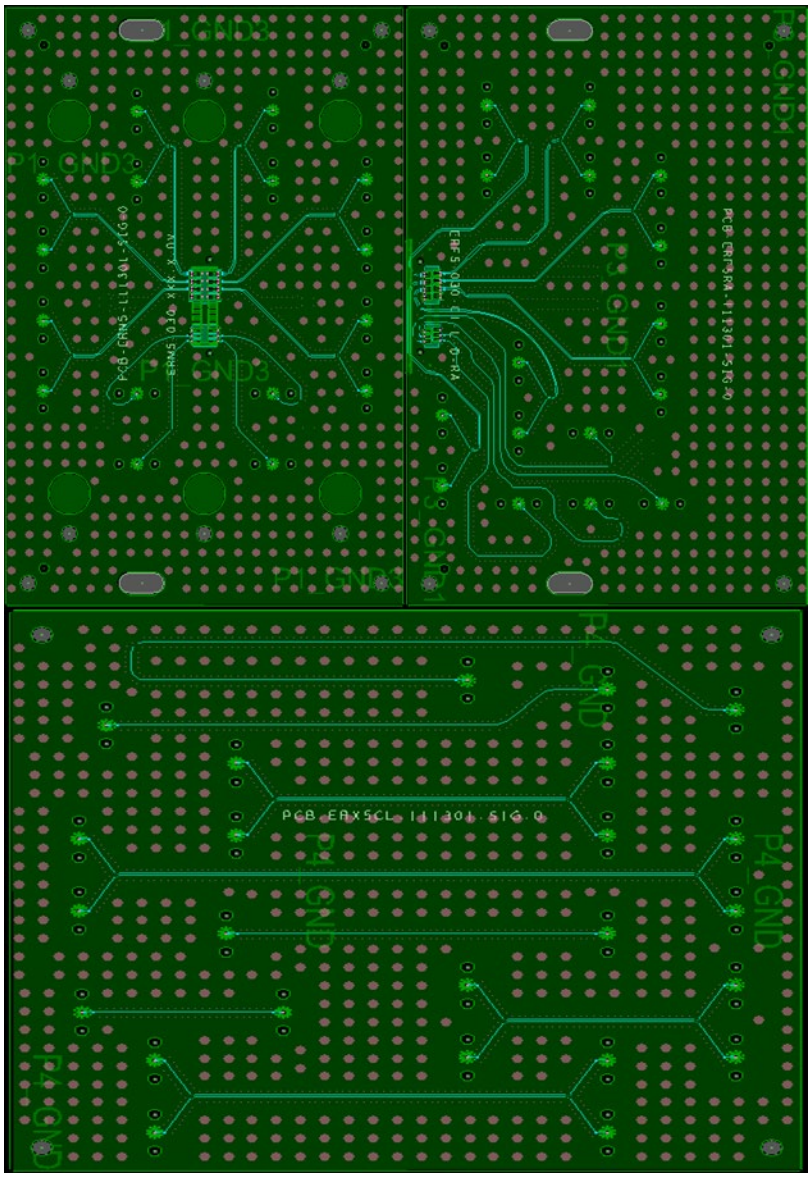

Figure 40

All traces on the test boards are length matched to 29.8 mm for Single-Ended ERM5, 76.36 mm for Single- Ended ERF5-RA and 39.05 mm for Differential ERM5, 53.55 mm for Differential ERM5 measured from the edge of the pad to the 2.4mm connector. The

Series: ERM5 / ERF5-RA
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AFR calibration effectively removes 27.9 mm of Single- Ended ERM5, 74.46 mm of Single- Ended ERF5-RA and 37.1 mm of Differential ERM5, 52.05 mm of Differential ERF5-RA test board trace effects. This means that 1.9 mm of Single- Ended both ends and 1.95 mm of Differential ERM5, 1.5 mm of Differential ERF5-RA test board trace length effects are included in the both sides of test boards in the measurement. The S-Parameter measurement includes:

A- The ERx5 Series connector set
B- Test board vias, pads (footprint effects) for the ERM5 connector side.
C- 1.9 mm Single- Ended of 0.151 mm wide microstrip trace.
D- 1.95 mm Differential of 0.151 mm wide microstrip trace
E- Test board vias, pads (footprint effects) for the ERF5-RA side.
F- 1.9 mm Single- Ended of 0.151 mm wide microstrip trace
G- 1.5 mm Differential of 0.151 mm wide microstrip trace

The figure below shows the location of the measurement reference plane.

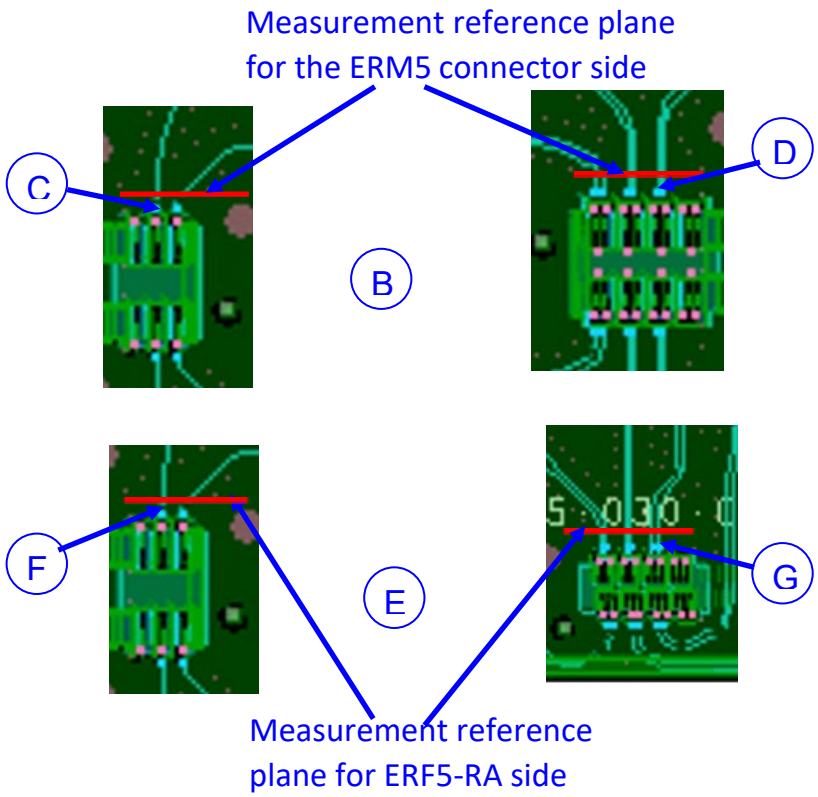

Figure 41

Series: ERM5 / ERF5-RA
Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Keysight N5225A PNA-L network analyzer. Frequency domain data are obtained directly from the instrument and figures are generated by Keysight ADS. The network analyzer is configured as follows:

Start Frequency – 10 MHz
Stop Frequency – 50 GHz
Number of points – 5000
IFBW – 1 KHz

N5225A Measurement Setup

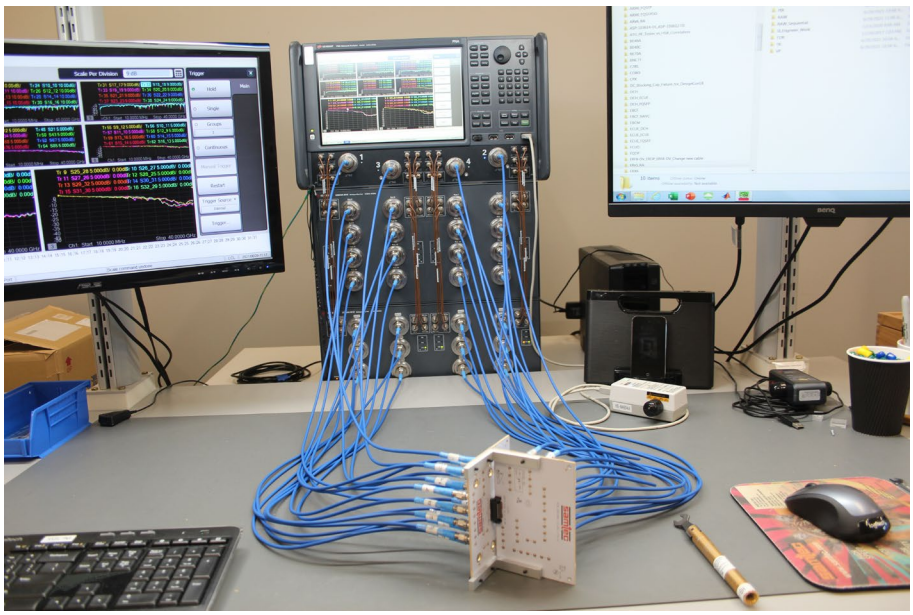

Figure 42

Test Instruments

QTY	Description
1	Keysight N5225A PNA Network Analyzer (10 MHz to 50 GHz)
1	Keysight 85056A M-Cal (10 MHz to 50 GHz)

Test Cables & Adapters

QTY	Description
4	Gore 0F0CAB036.0-LF (DC to 67 GHz)

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Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the through calibration standards, the SI test boards, and the selection of the PCB vendor.

A coaxial SOLT calibration is performed using 85056A M-Cal module. Then DUT measurements are performed under SOLT calibration. The measurements include the effect of test fixture. The measurements of the 2X THRU line standards are required to remove the test fixture effect.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2017. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)
A step pulse is applied to the touchstone model of the connector and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

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Description: 0.50 mm Edge Rate® Rugged High-Speed Interconnect

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
Z – Impedance (expressed in ohms)