



High Speed Characterization Report

HSEC8-1XX-01-L-DP-A-WT-K



Description:

**0.80 mm Edge Rate® High Speed Edge Card Connector,
Differential Pair, Accepts 1.60mm (.062") thick card**

Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
Differential Pair, Accepts 1.60mm (.062”) thick card

Table of Contents

Connector Overview	1
Frequency Domain Data Summary	1
Bandwidth Chart – Differential Insertion Loss	1
Time Domain Data Summary	2
Table 1 - Differential Impedance (Ω)	2
Table 2 - Differential Crosstalk (%)	3
Table 3 - Propagation Delay (Mated Connector)	4
Characterization Details	5
Differential and Single-Ended Data	5
Connector Signal to Ground Ratio	5
Frequency Domain Data	6
Time Domain Data	7
Appendix A – Frequency Domain Responses	8
Differential Application – Insertion Loss	8
Differential Application – Return Loss	8
Differential Application – NEXT Configurations	9
Differential Application – FEXT Configurations	10
Appendix B – Time Domain Responses	11
Differential Application – Impedance	11
Differential Application – Propagation Delay	15
Appendix C – Product and Test System Descriptions	19
Product Description	19
Test System Description	19
PCB-HSEC8X-109266 Test Fixtures	19
PCB Fixtures	20
Appendix D – Test and Measurement Setup	22
N5225B Measurement Setup	22
Test Instruments	23
Test Cables & Adapters	23
Appendix E - Frequency and Time Domain Measurements	24
Frequency (S-Parameter) Domain Procedures	24
Time Domain Procedures	24
Impedance (TDR)	24
Propagation Delay (TDT)	25
Appendix F – Glossary of Terms	26

Series: HSEC8-DP

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Differential Pair, Accepts 1.60mm (.062") thick card

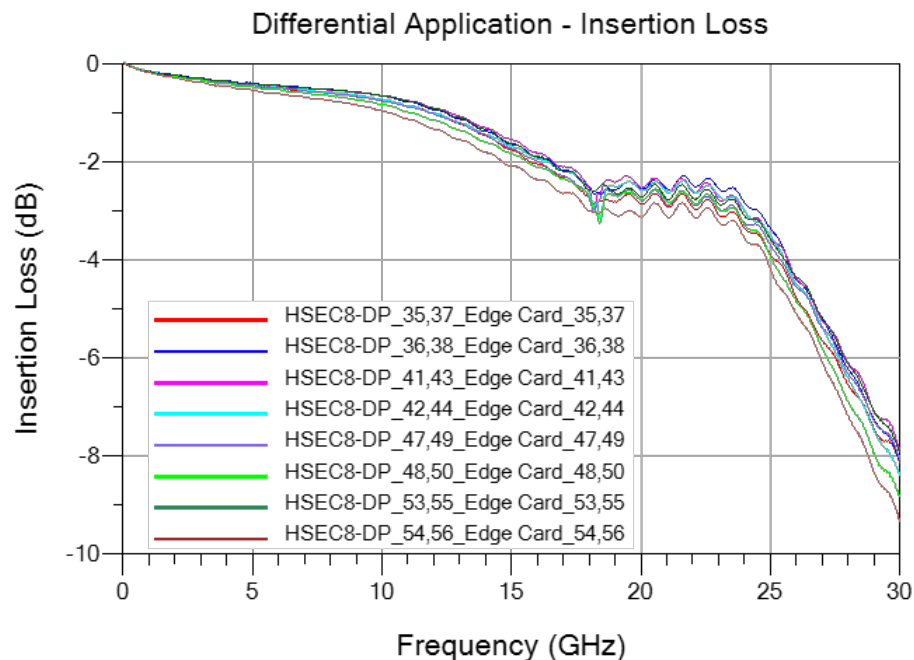
Connector Overview

The HSEC8-DP is a vertical mount 0.80 mm pitch edge card connector with dedicated differential pairs. Featuring Samtec's Edge Rate® contact system, this series is designed for applications requiring high-mating cycles and 28 Gbps performance. The HSEC8-DP is usable with a 1.60 mm (.062") card. Data in this report is applicable to a vertical surface mount to edge card application.

Frequency Domain Data Summary

Bandwidth Chart – Differential Insertion Loss

HSEC8-DP Connector Series



Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
Differential Pair, Accepts 1.60mm (.062") thick card**Time Domain Data Summary**

Table 1 - Differential Impedance (Ω)				
Driver	Signal Rise-time	30ps	50ps	100ps
HSEC8-DP_35,37	Maximum Impedance	106.51	106.26	105.89
	Minimum Impedance	94.71	97.31	98.39
HSEC8-DP_36,38	Maximum Impedance	107.94	107.71	107.48
	Minimum Impedance	95.17	97.81	98.74
HSEC8-DP_41,43	Maximum Impedance	101.74	107.10	106.98
	Minimum Impedance	94.82	97.59	98.72
HSEC8-DP_42,44	Maximum Impedance	107.62	107.55	107.44
	Minimum Impedance	94.85	97.52	98.93
HSEC8-DP_47,49	Maximum Impedance	106.52	106.26	105.76
	Minimum Impedance	94.84	97.41	98.51
HSEC8-DP_48,50	Maximum Impedance	107.15	106.84	106.49
	Minimum Impedance	94.79	97.41	98.57
HSEC8-DP_53,55	Maximum Impedance	107.26	107.00	106.92
	Minimum Impedance	95.00	97.72	98.83
HSEC8-DP_54,56	Maximum Impedance	106.96	106.67	106.09
	Minimum Impedance	94.52	97.23	98.78

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Table 2 - Differential Crosstalk (%)

Input(tr)	Driver	Receiver	30ps	50ps	100ps
NEXT	HSEC8-DP_35,37	HSEC8-DP_41,43	0.35	0.26	0.15
	HSEC8-DP_35,37	HSEC8-DP_47,49	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	HSEC8-DP_53,55	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	HSEC8-DP_36,38	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	HSEC8-DP_42,44	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	HSEC8-DP_48,50	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	HSEC8-DP_54,56	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	HSEC8-DP_36,38	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	HSEC8-DP_42,44	0.34	0.25	0.15
	HSEC8-DP_48,50	HSEC8-DP_54,56	0.34	0.25	0.15
	HSEC8-DP_48,50	HSEC8-DP_35,37	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	HSEC8-DP_41,43	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	HSEC8-DP_47,49	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	HSEC8-DP_53,55	<0.1	<0.1	<0.1
FEXT	HSEC8-DP_35,37	Edge Card_41,43	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	Edge Card_47,49	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	Edge Card_53,55	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	Edge Card_36,38	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	Edge Card_42,44	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	Edge Card_48,50	<0.1	<0.1	<0.1
	HSEC8-DP_35,37	Edge Card_54,56	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_36,38	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_42,44	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_54,56	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_35,37	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_41,43	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_47,49	<0.1	<0.1	<0.1
	HSEC8-DP_48,50	Edge Card_53,55	<0.1	<0.1	<0.1

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Table 3 - Propagation Delay (Mated Connector)

HSEC8-DP 35,37 Edge Card 35,37	70 ps
HSEC8-DP 36,38 Edge Card 36,38	70 ps
HSEC8-DP 41,43 Edge Card 41,43	70 ps
HSEC8-DP 42,44 Edge Card 42,44	70 ps
HSEC8-DP 47,49 Edge Card 47,49	70 ps
HSEC8-DP 48,50 Edge Card 48,50	71 ps
HSEC8-DP 53,55 Edge Card 53,55	71 ps
HSEC8-DP 54,56 Edge Card 54,56	72 ps

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Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for only differentially driven scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.



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2												G	T	T	G	36	38	G	42	44	G	48	50	G	54	56	G	T	T	G
1												G	T	T	G	35	37	G	41	43	G	47	49	G	53	55	G	T	T	G

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Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Keysight Advanced Design System to obtain the time domain response. Time Domain procedure is provided in [Appendix E](#) of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 5 mm of PCB trace on the HSEC8-DP and Edge Card side each. Delay is measured at 100 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

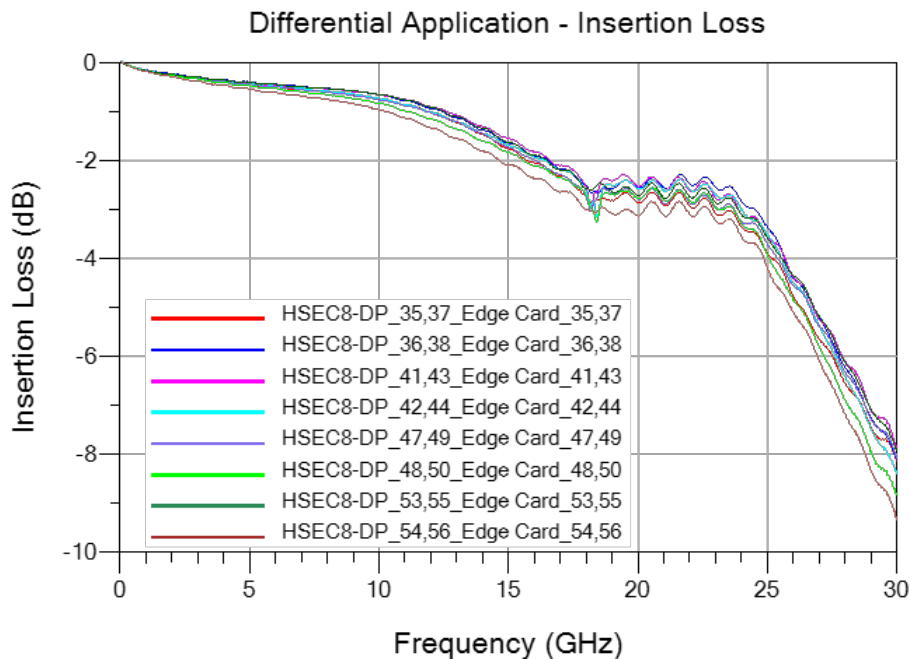
As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

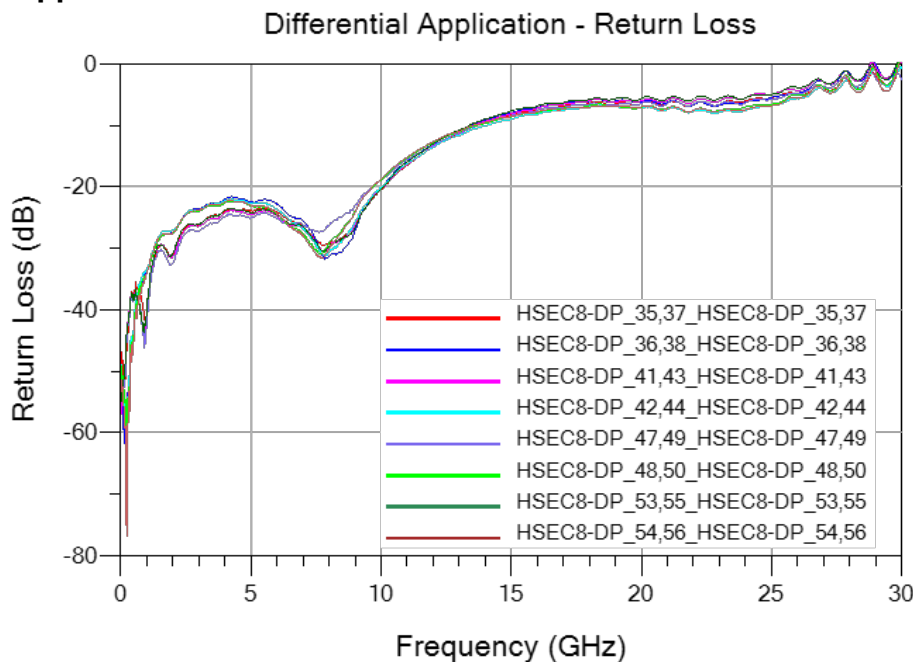
Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
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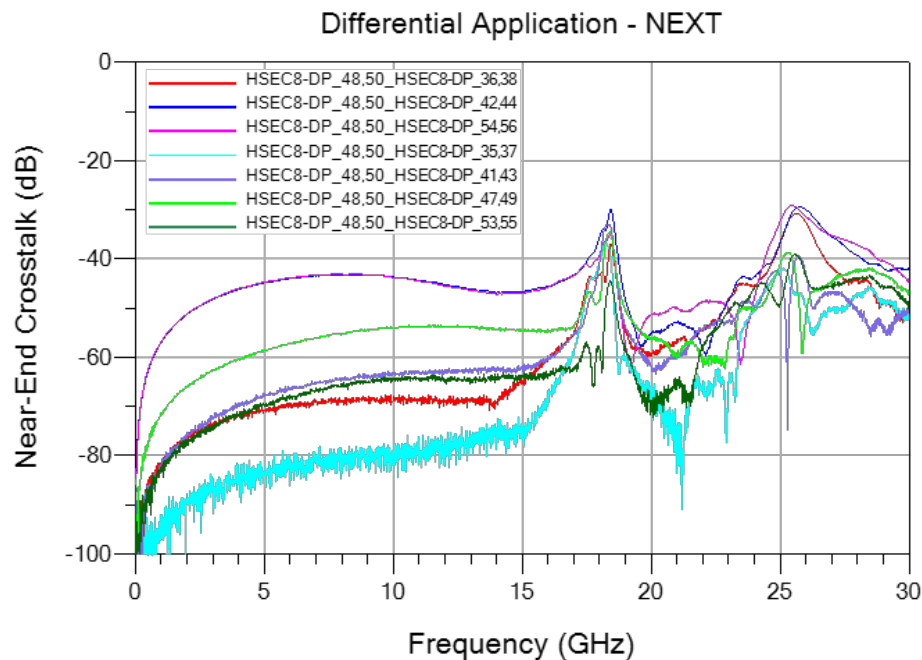
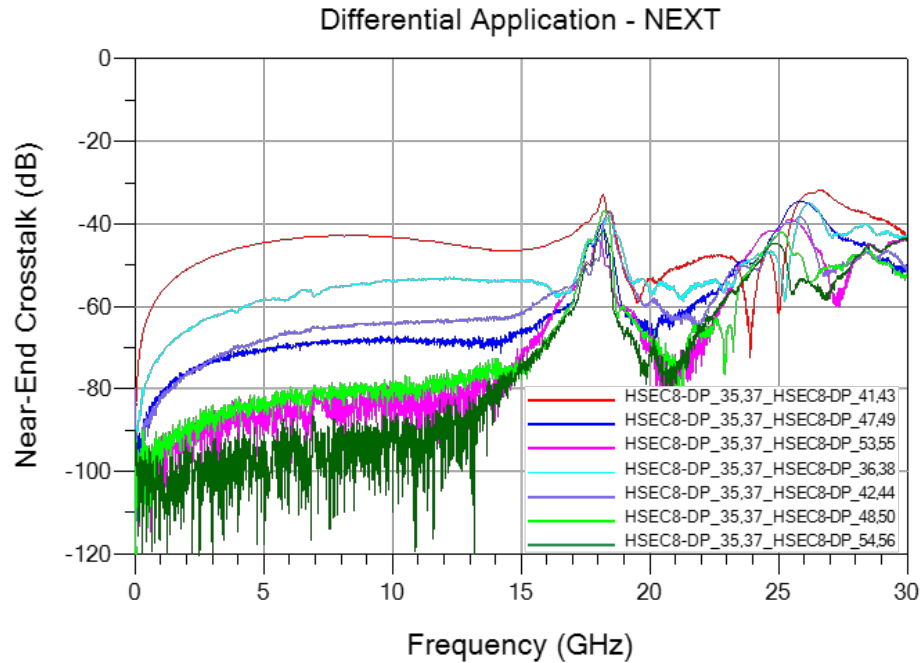
Appendix A – Frequency Domain Responses

Differential Application – Insertion Loss



Differential Application – Return Loss

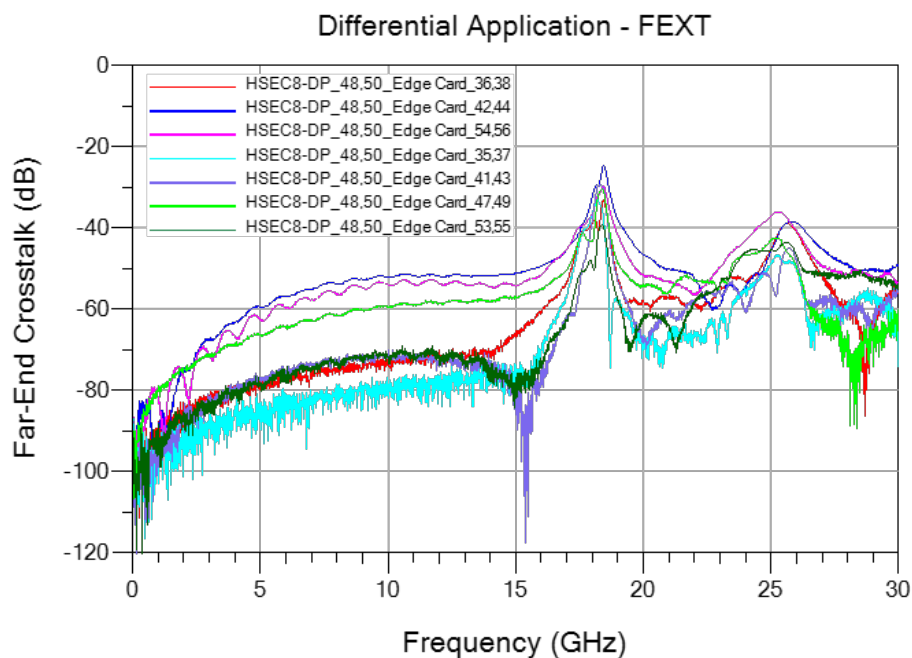
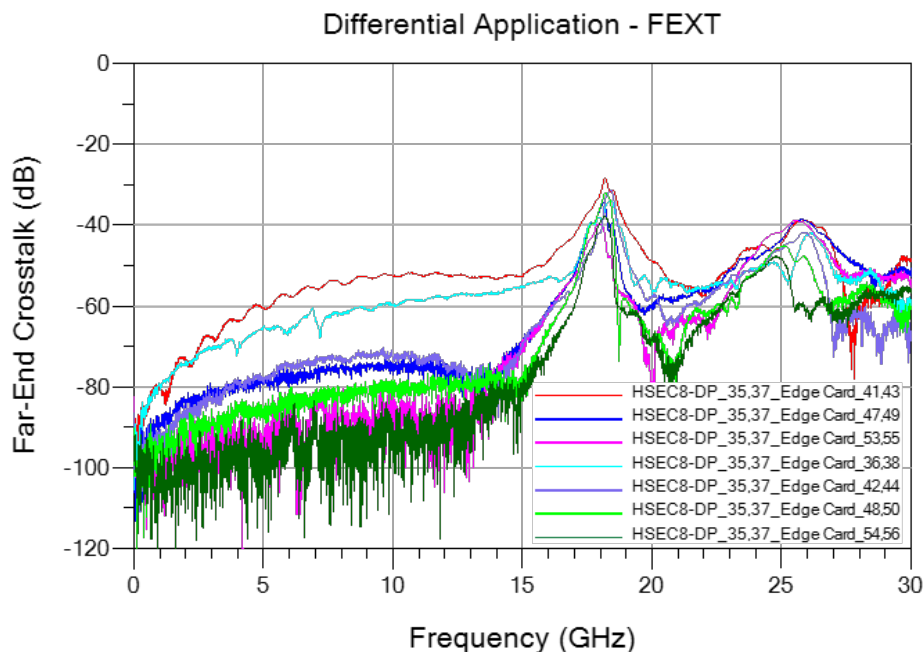


Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
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Series: HSEC8-DP

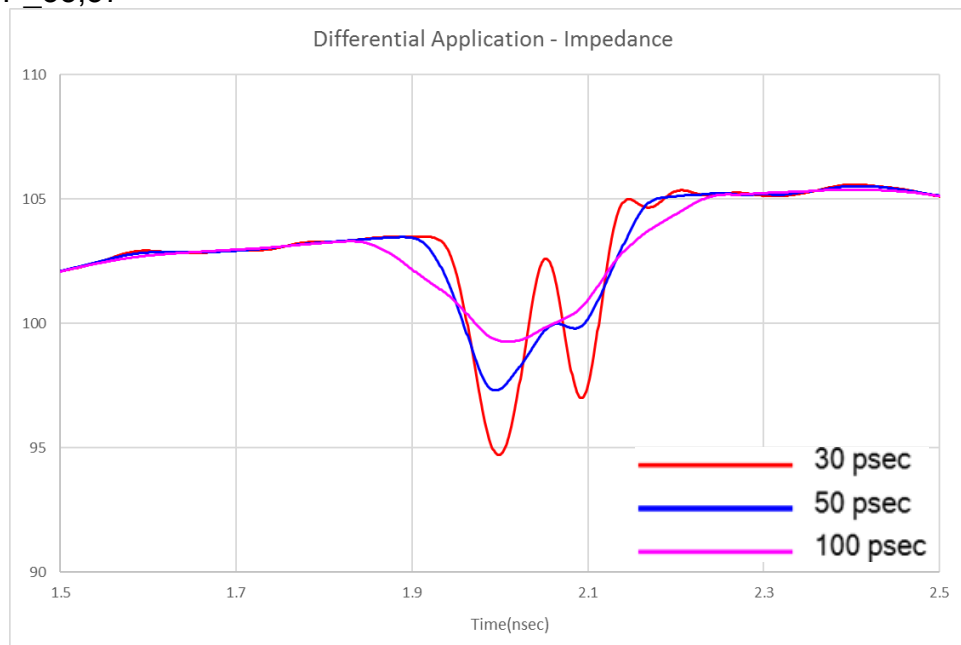
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Differential Application – FEXT Configurations

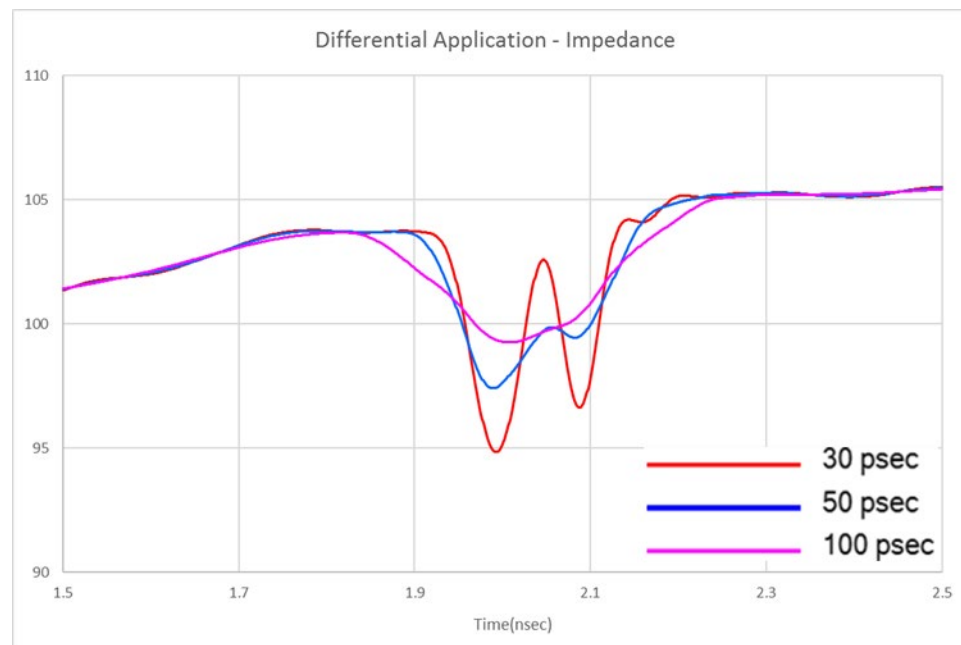


Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
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HSEC8-DP_35,37

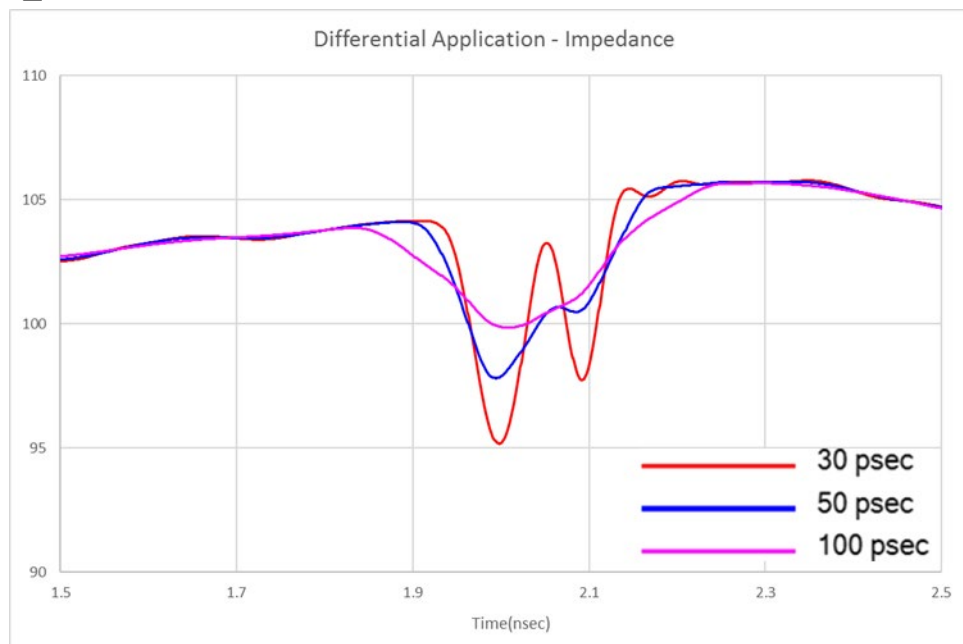


HSEC8-DP_36,38

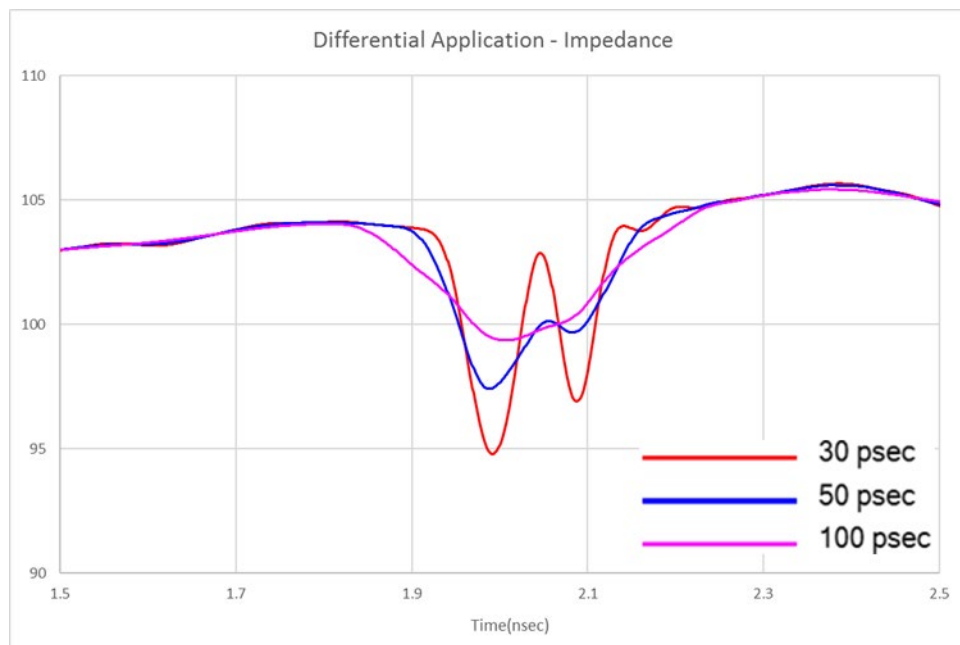


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HSEC8-DP_41,43

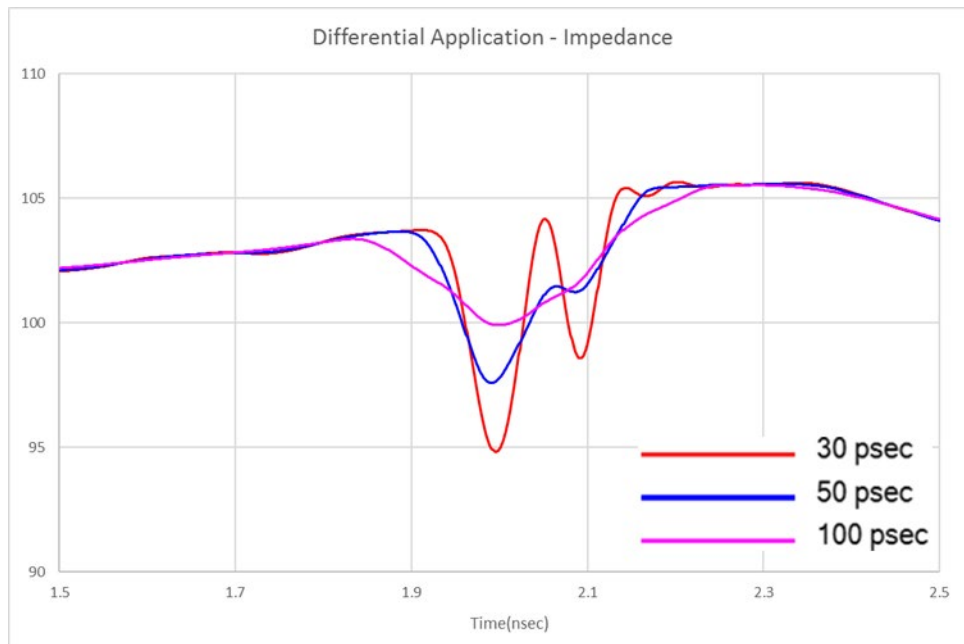


HSEC8-DP_42,44

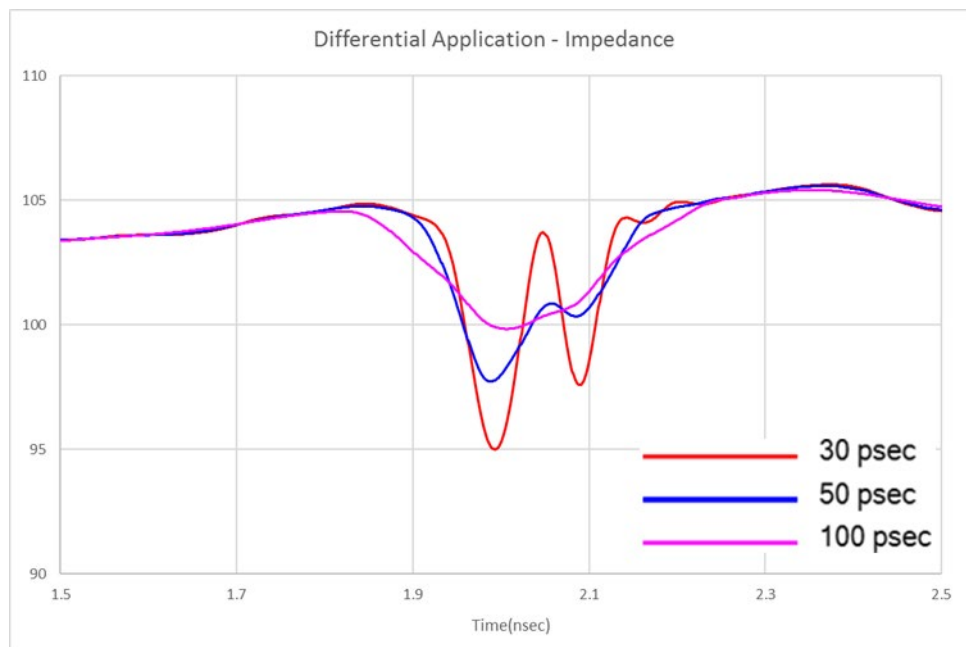


Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
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HSEC8-DP_47,49

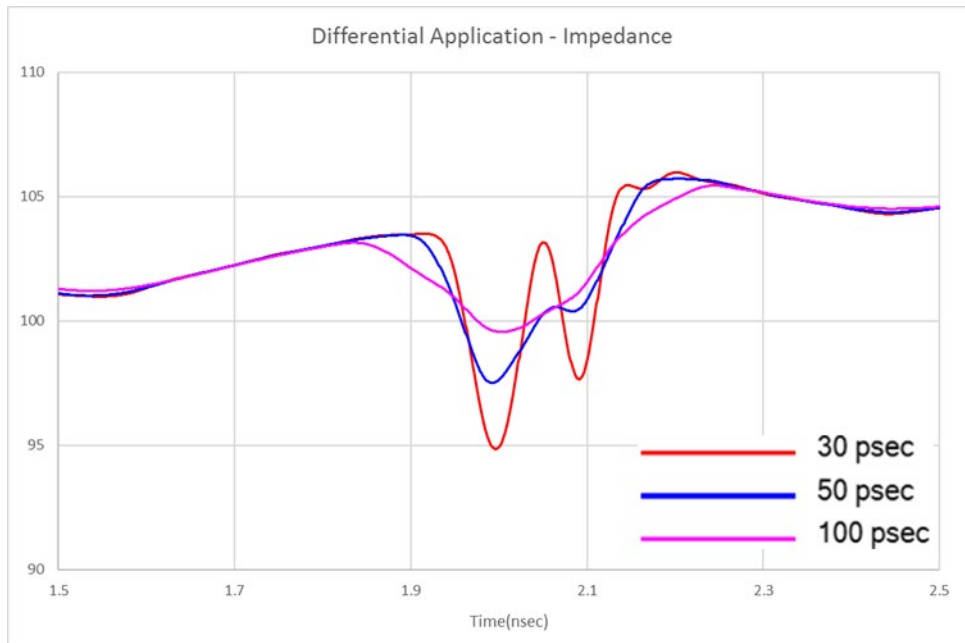


HSEC8-DP_48,50

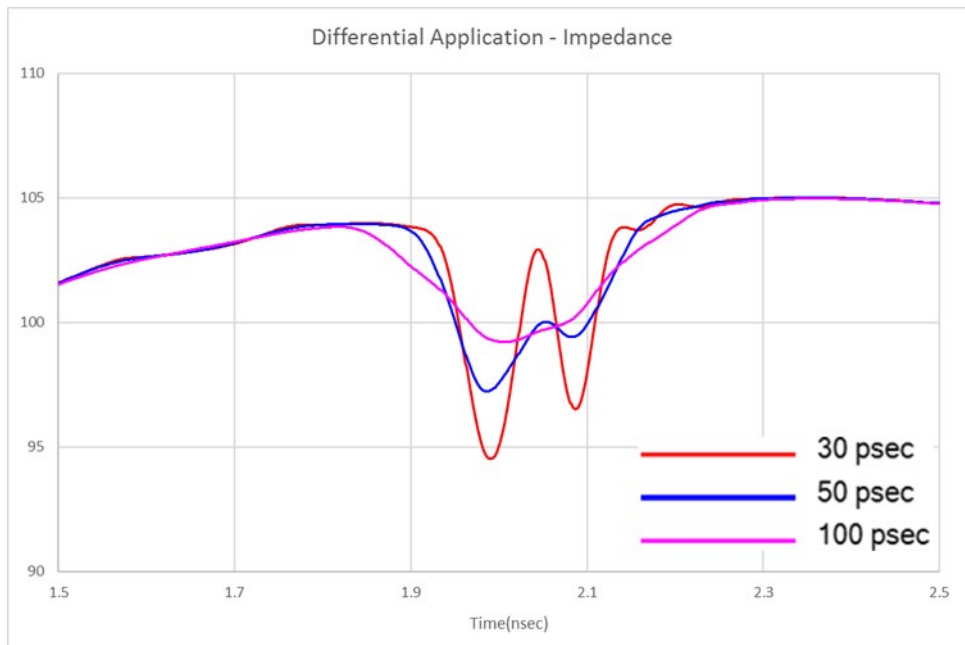


Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
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HSEC8-DP_53,55



HSEC8-DP_54,56

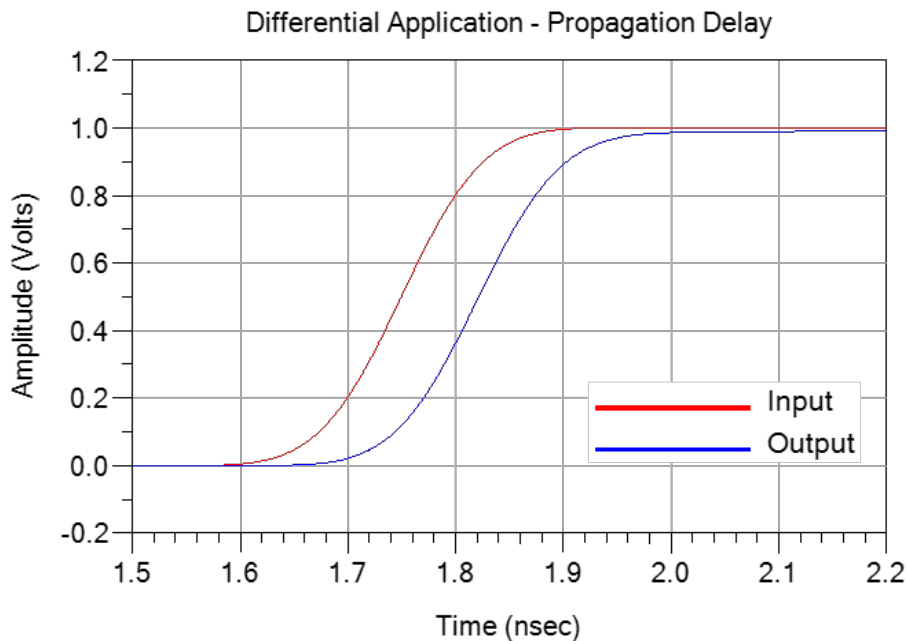


Series: HSEC8-DP

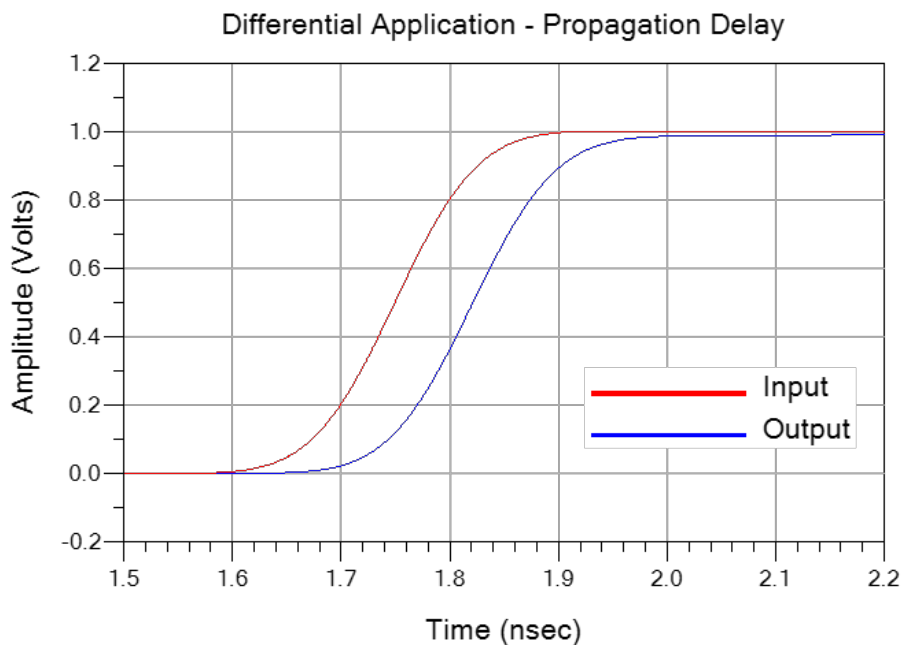
Description: 0.80 mm Edge Rate® High Speed Edge Card Connector,
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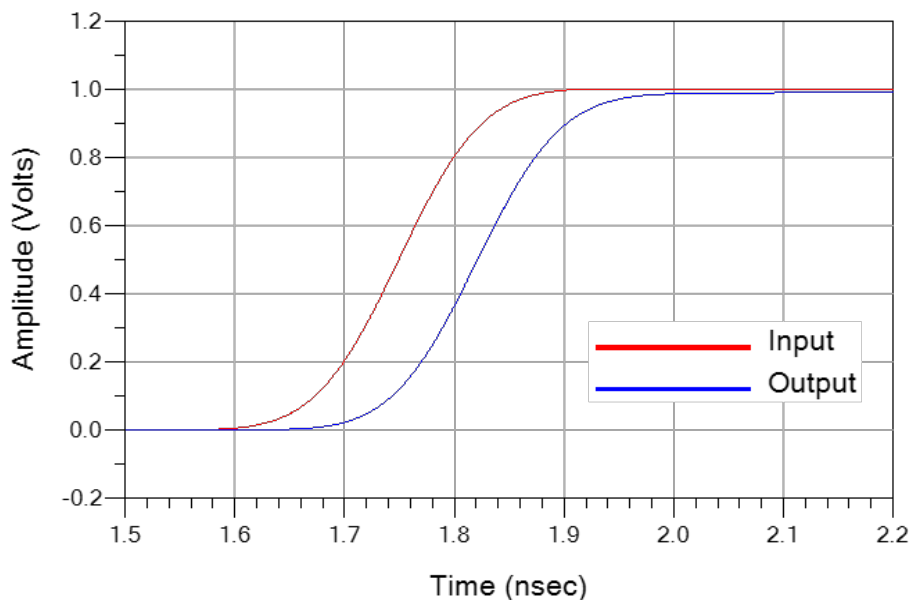
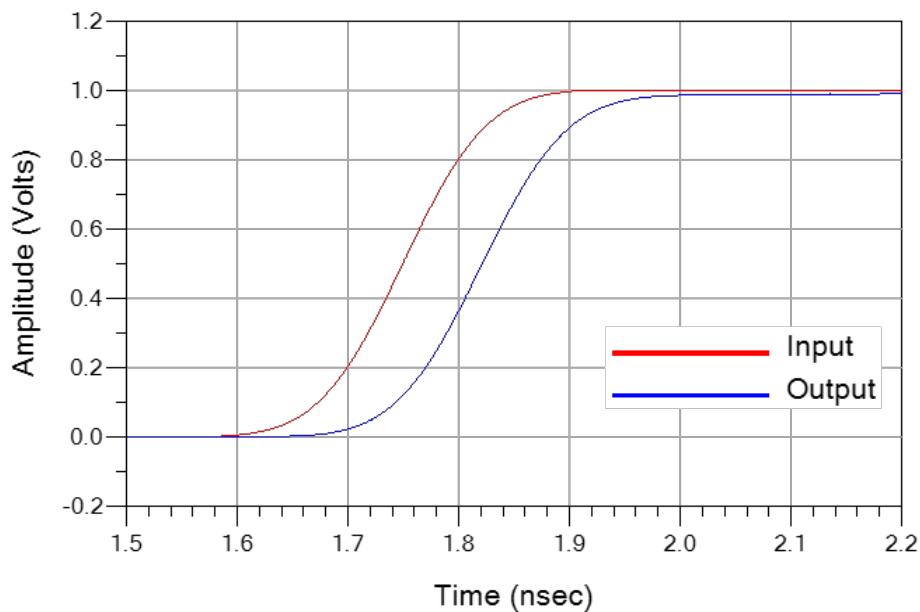
Differential Application – Propagation Delay

HSEC8-DP_35,37_Edge Card_35,37



HSEC8-DP_36,38_Edge Card_36,38

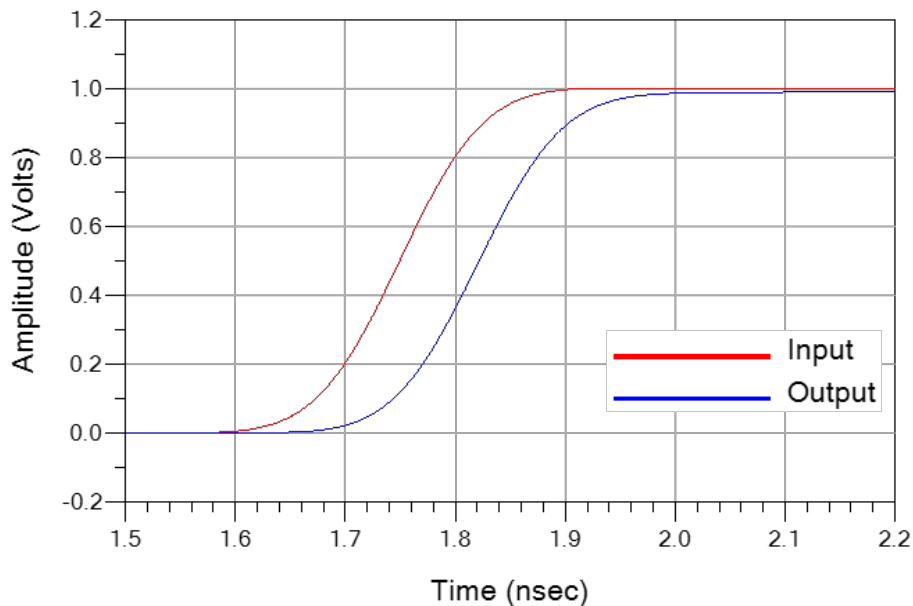


Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
Differential Pair, Accepts 1.60mm (.062") thick card**HSEC8-DP_41,43_Edge Card_41,43****Differential Application - Propagation Delay****HSEC8-DP_42,44_Edge Card_42,44****Differential Application - Propagation Delay**

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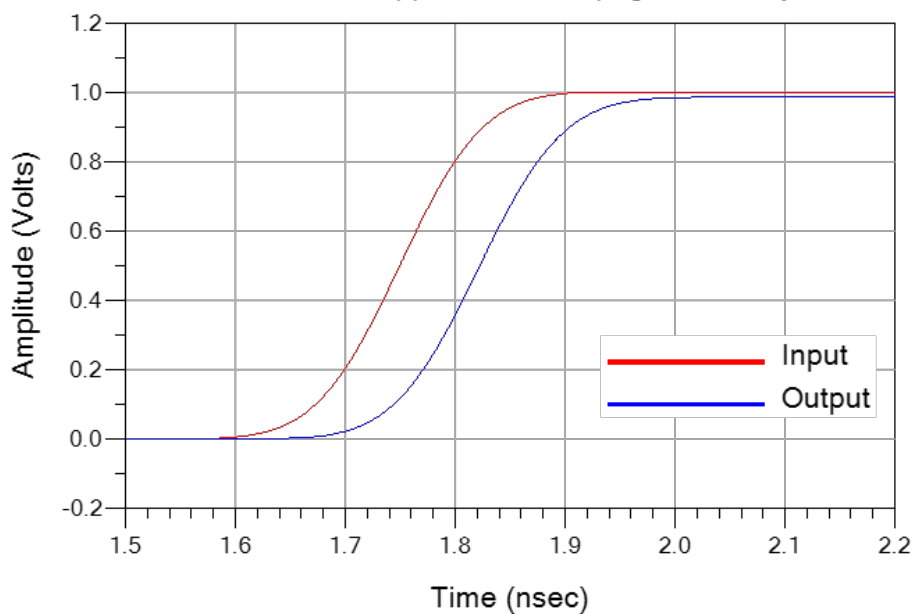
HSEC8-DP_47,49_Edge Card_47,49

Differential Application - Propagation Delay



HSEC8-DP_48,50_Edge Card_48,50

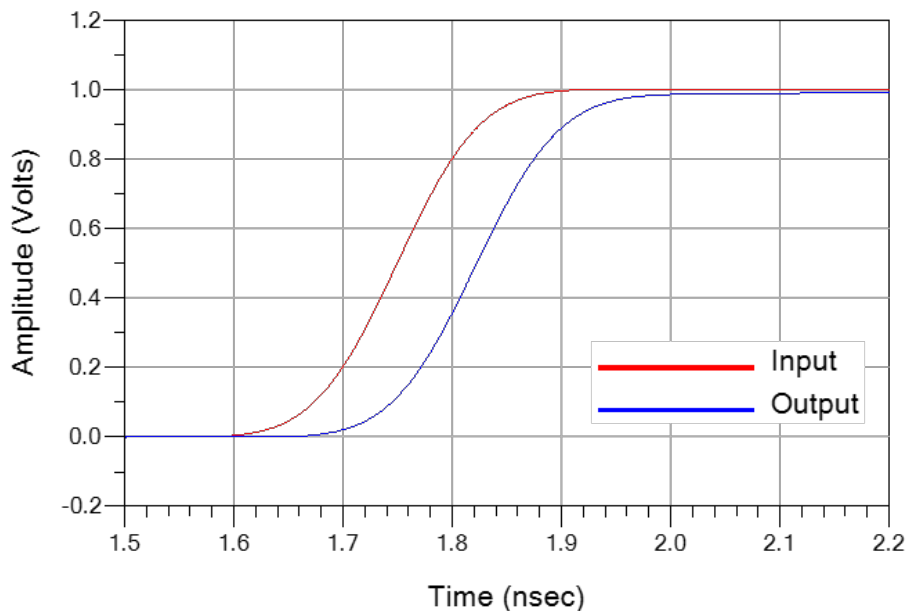
Differential Application - Propagation Delay



Series: HSEC8-DP**Description:** 0.80 mm Edge Rate® High Speed Edge Card Connector,
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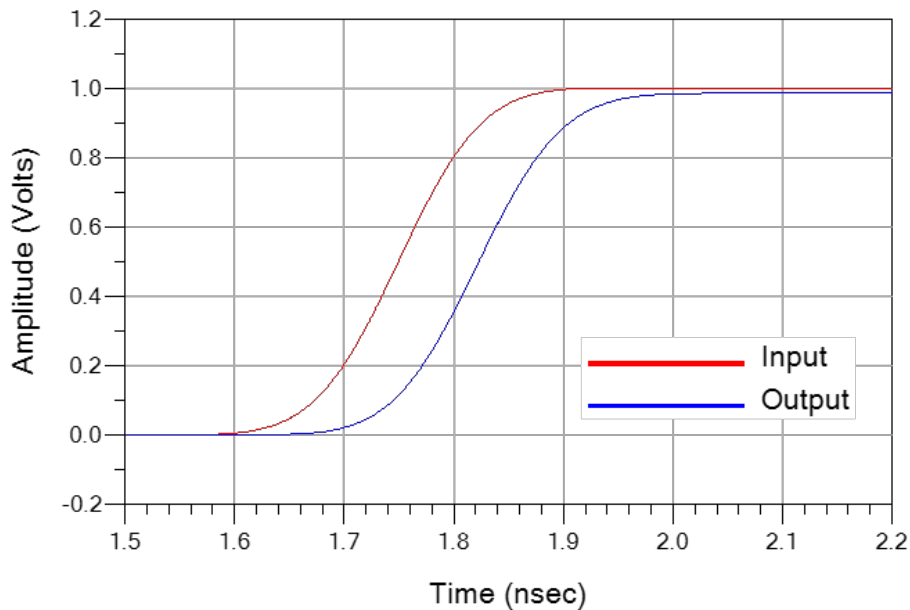
HSEC8-DP_53,55_Edge Card_53,55

Differential Application - Propagation Delay



HSEC8-DP_54,56_Edge Card_54,56

Differential Application - Propagation Delay



Series: HSEC8-DP

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Appendix C – Product and Test System Descriptions

Product Description

Product test samples are HSEC8-DP Series connectors. The part number is HSEC8-120-01-L-DP-A-WT-K. The HSEC8-DP Series connector are surface mount products. Each connector has two rows of contacts evenly spaced on a 0.8mm (0.0315") pitch. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of eight-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount SMA connector is used to interface the PNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. One fixture is specific to the HSEC8-DP series connector set and identified by part numbers PCB-HSEC8F-109266-SIG and PCB-HSEC8E-109266-SIG. Calibration standards specific to the HSEC8-DP series are located on the calibration boards PCB-HSEC8C-109266-SIG.

PCB-HSEC8X-109266 Test Fixtures

Shown below is a photograph of the one of the three test board sets.



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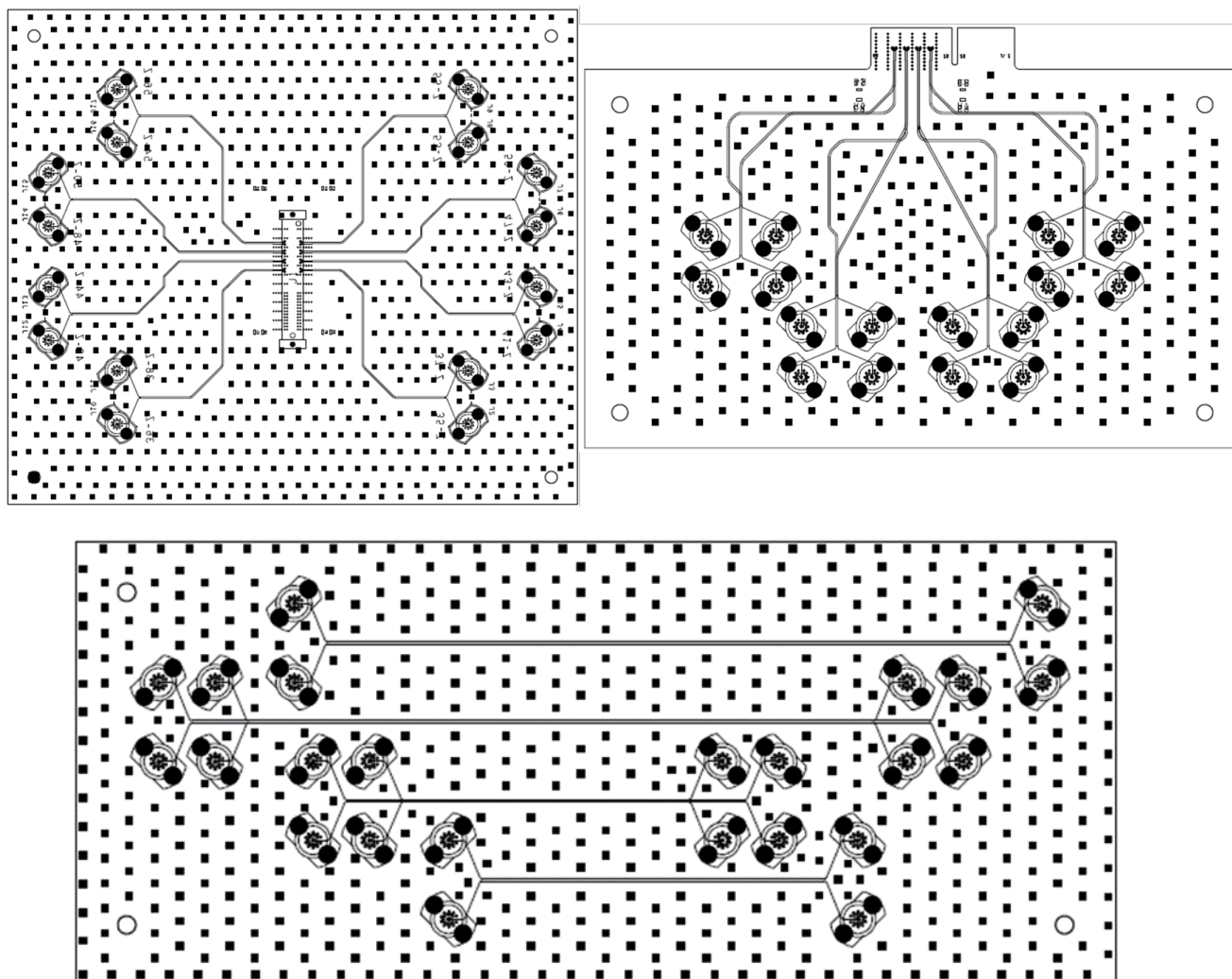
PCB Fixtures

The test fixtures used are as follows:

PCB-HSEC8F-109266-SIG – HSEC8-DP Series Test Board

PCB-HSEC8E-109266-SIG – Edge Card Test Board

PCB-HSEC8C-109266-SIG – Calibration Board



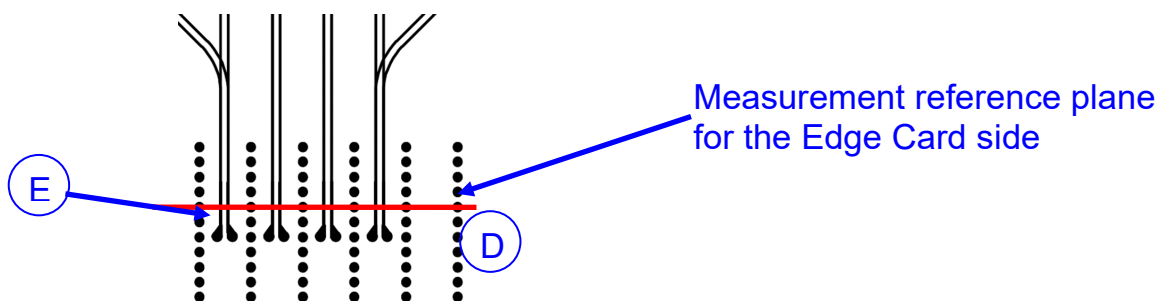
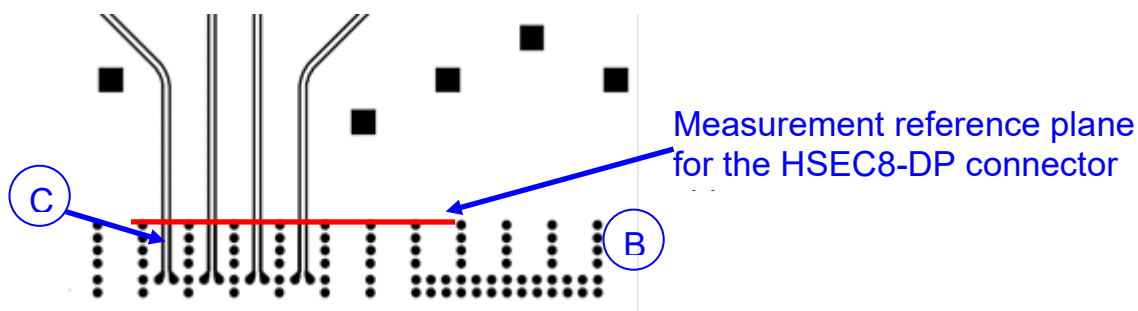
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All traces on the test boards are length matched to 75 mm measured from the edge of the pad to the SMA. The TRL calibration effectively removes 70 mm of test board trace effects. This means that 5 mm of test board trace length effects are included in both sides of test boards in the measurement. The S-Parameter measurement includes:

- A- The HSEC8-DP Series connector set
- B- Test board vias, pads (footprint effects) for the HSEC8-DP connector side.
- C- 5 mm of 5 mil wide microstrip trace.
- D- Test board vias, pads (footprint effects) for the Edge Card side.
- E- 5 mm of 5 mil wide microstrip trace.

The figure below shows the location of the measurement reference plane.



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Appendix D – Test and Measurement Setup

The test instrument is the Keysight N5225B PNA network analyzer with Keysight U3044A M16 Multiport Test set and Keysight U3044A M12 Multiport Test set. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Keysight ADS. The network analyzer is configured as follows:

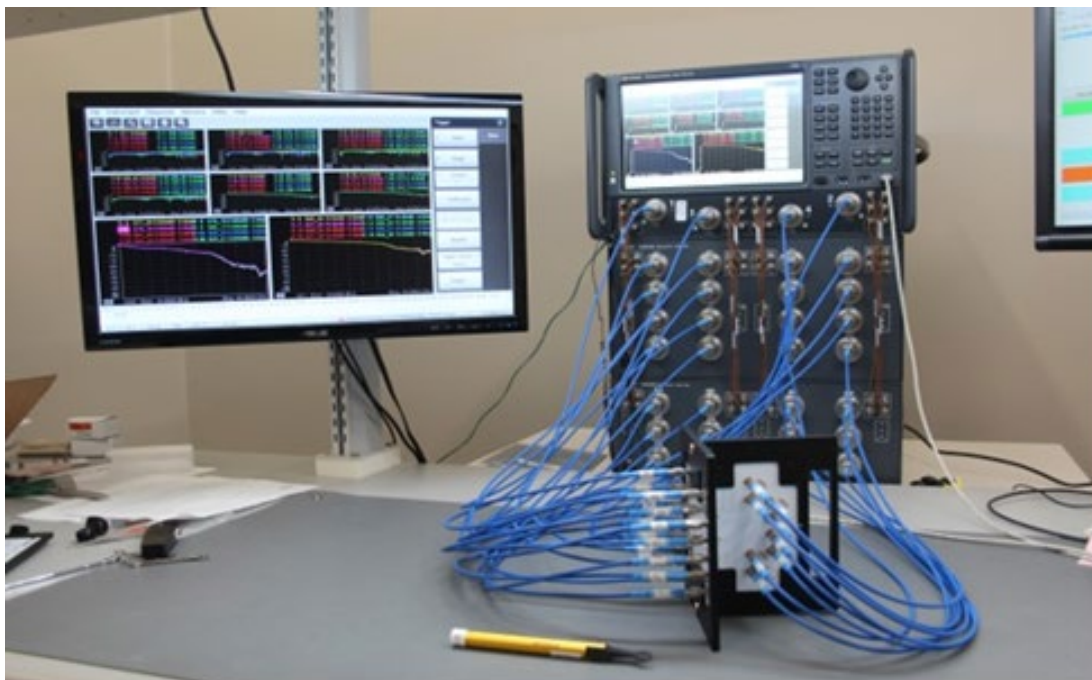
Start Frequency – 10 MHz

Stop Frequency – 50 GHz

Step – 10 MHz

IFBW – 200 Hz

N5225B Measurement Setup



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Test Instruments

<u>QTY</u>	<u>Description</u>
1	Keysight N5225A PNA Network Analyzer (10 MHz to 50 GHz)
1	Keysight N4433A U3044A M16 Multiport Test Set (10 MHz to 40 GHz)
1	Keysight N4433A U3044A M12 Multiport Test Set (10 MHz to 40 GHz)
1	Keysight N4694-60003 E-Cal Module (10 MHz to 67 GHz)

Test Cables & Adapters

<u>QTY</u>	<u>Description</u>
4	Junkosha 2.92mm Cables (DC to 40 GHz)

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Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the LRM calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the LRM calibration standards. A coaxial SOLT calibration is performed using an N4694 ecal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the reflect and 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the HSEC8-DP Series test boards, this is greater than 30 GHz.

From the LRM calibration standard measurements, a user defined calibration kit is developed and stored in the network analyzer. Calibration is then performed on all 4 ports following the calibration wizard within the Keysight N5225B. This calibration is saved and can be recalled at any time. Calibration takes roughly 30 minutes to perform.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2017. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.

http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)

A step pulse is applied to the touchstone model of the connector and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

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Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Series: HSEC8-DP

Description: 0.80 mm Edge Rate® High Speed Edge Card Connector,
Differential Pair, Accepts 1.60mm (.062") thick card

Appendix F – Glossary of Terms

ADS – Advanced Design Systems

FD – Frequency domain

FEXT – Far-End Crosstalk

GSG – Ground–Signal–Ground; geometric configuration

GSSG - Ground–Signal–Signal–Ground; geometric configuration

NEXT – Near-End Crosstalk

PCB – Printed Circuit Board

SE – Single-Ended

SI – Signal Integrity

SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards

TD – Time Domain

TDA – Time Domain Analysis

TDR – Time Domain Reflectometry

TDT – Time Domain Transmission

Z – Impedance (expressed in ohms)