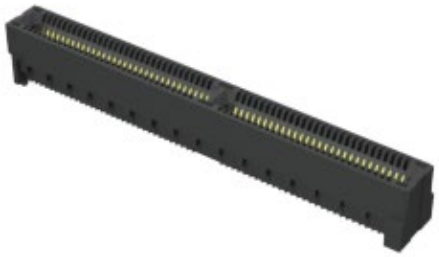
High Speed Characterization Report

HTEC8-1XX-01-X-DV-A-XX



Description:
0.80 mm Rugged High-Speed Edge Card Socket, Mates with1.60mm (.062”) thick cards

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

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Report Revision: 1/5/2024

Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

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Connector Overview

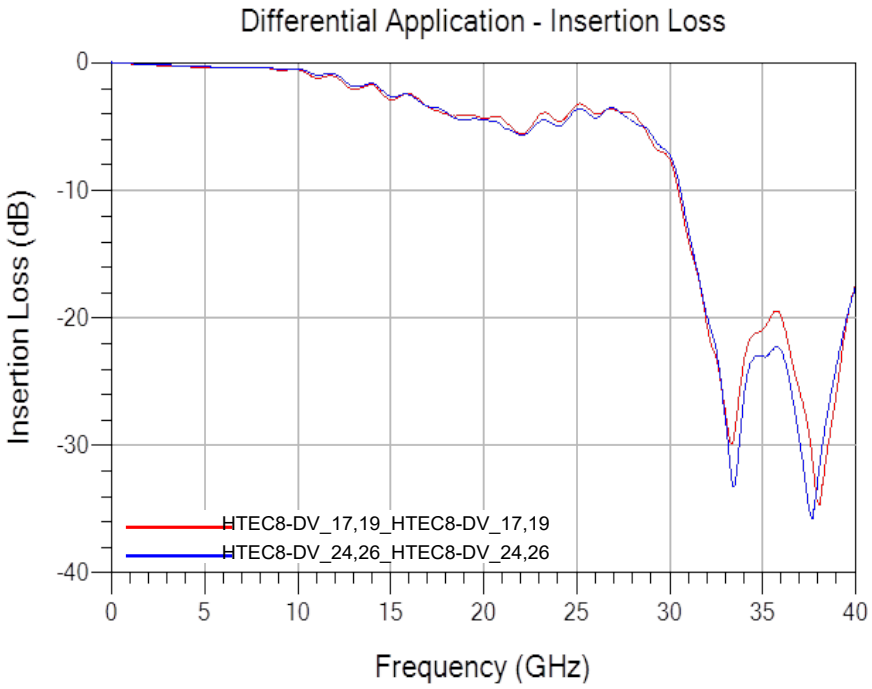
0.8mm (.0315”) pitch interfaces (HTEC8 Series) are double row structures with up to 100 contacts per row. The HTEC8 connector is modified from HSEC8, most of the geometric of terminal designs are same except adding preload, and it is vertical surface mount style, accepts non-chamfered edge cards for cost optimization. Data in this report is applicable to a vertical surface mount to edge card application.

Frequency Domain Data Summary

Bandwidth Chart – Differential Insertion Loss

HTEC8 Connector Series

10GbE



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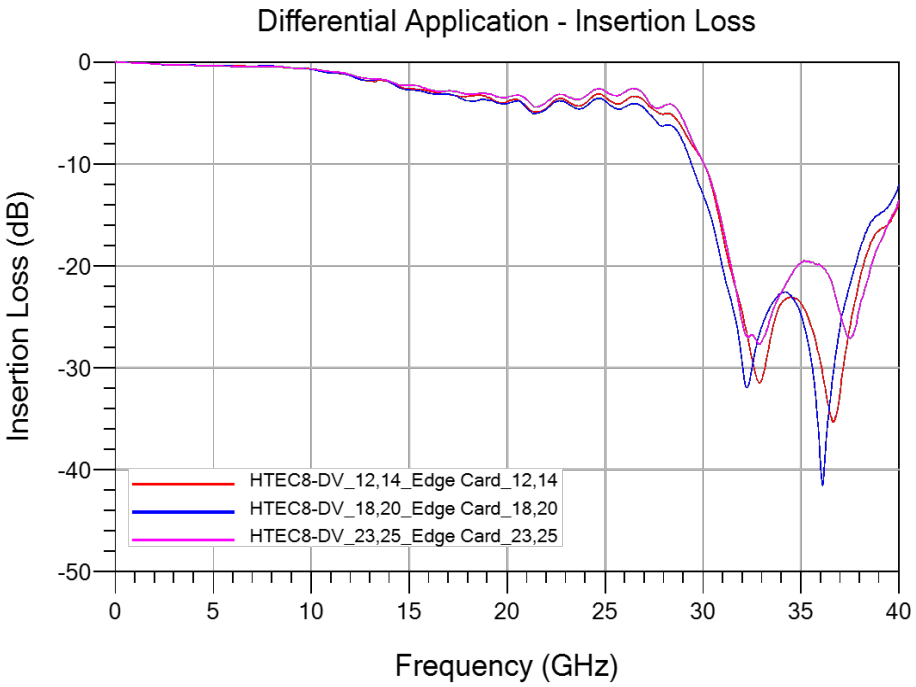
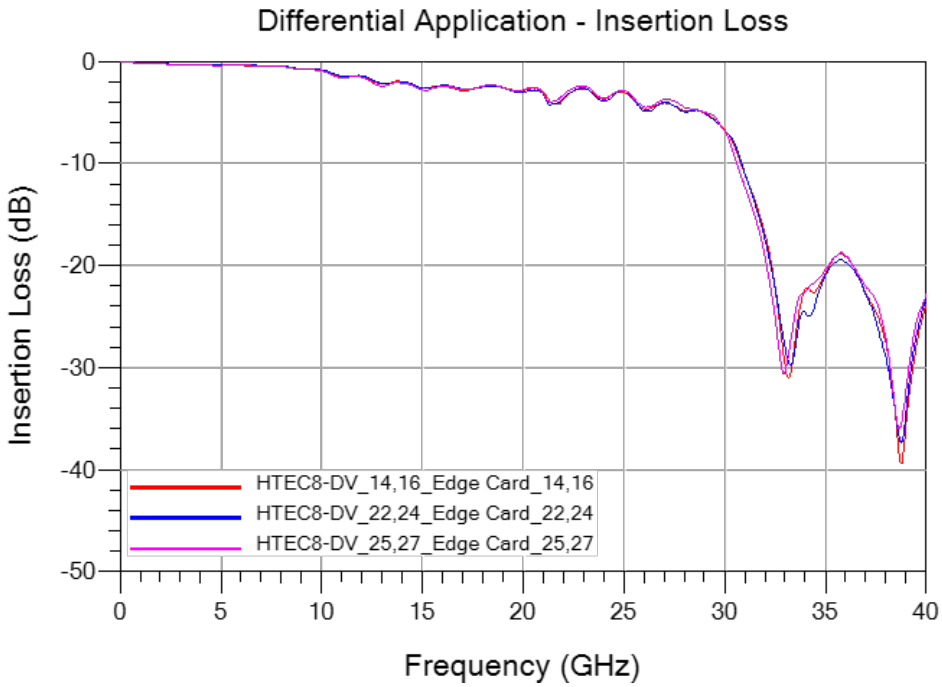
10GbE (GSSG)



PCIe



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Time Domain Data Summary

Table 1 - Differential Impedance (Ω)					
Configuration	**Driver**	**Signal Rise-time**	**30ps**	**50ps**	**100ps**
10GbE	HTEC8-DV_17,19	Maximum Impedance	108.5	109.2	109.6
		Minimum Impedance	86.9	91.1	93.5
	HTEC8-DV_24,26	Maximum Impedance	107.4	108.6	108.5
		Minimum Impedance	87.5	91.6	93.8
10GbE (GSSG)	HTEC8-DV_12,14	Maximum Impedance	106.5	107.8	107.6
		Minimum Impedance	85.7	89.7	92.3
	HTEC8-DV_18,20	Maximum Impedance	106.8	108.4	108.2
		Minimum Impedance	85.8	90.2	92.6
	HTEC8-DV_23,25	Maximum Impedance	105.5	107.3	107.2
		Minimum Impedance	85.3	89.1	91.9
PCIe	HTEC8-DV_14,16	Maximum Impedance	89.2	91.3	91.2
		Minimum Impedance	71.5	75.6	77.7
	HTEC8-DV_22,24	Maximum Impedance	91.3	92.5	92.9
		Minimum Impedance	71.7	75.7	77.7
	HTEC8-DV_25,27	Maximum Impedance	91.0	91.7	91.6
		Minimum Impedance	70.6	74.8	77.1

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Table 2 - Differential Crosstalk (%)						
Input(tr)	**Configuration**	**Driver**	**Receiver**	**30ps**	**50ps**	**100ps**
NEXT	10GbE	HTEC8-DV_17,19	HTEC8-DV_5,7	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	HTEC8-DV_12,14	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	HTEC8-DV_24,26	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	HTEC8-DV_29,31	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	HTEC8-DV_36,38	<0.1	<0.1	<0.1
	10GbE (GSSG)	HTEC8-DV_18,20	HTEC8-DV_12,14	0.37	0.26	0.16
		HTEC8-DV_18,20	HTEC8-DV_17,19	0.50	0.34	0.18
		HTEC8-DV_18,20	HTEC8-DV_23,25	<0.1	<0.1	<0.1
		HTEC8-DV_18,20	HTEC8-DV_24,26	0.40	0.29	0.18
	PCIe	HTEC8-DV_22,24	HTEC8-DV_14,16	<0.1	<0.1	<0.1
		HTEC8-DV_22,24	HTEC8-DV_17,19	0.15	0.10	<0.1
		HTEC8-DV_22,24	HTEC8-DV_25,27	0.15	0.10	<0.1
		HTEC8-DV_22,24	HTEC8-DV_30,32	<0.1	<0.1	<0.1
FEXT	10GbE	HTEC8-DV_17,19	Edge Card_5,7	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	Edge Card _12,14	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	Edge Card _24,26	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	Edge Card _29,31	<0.1	<0.1	<0.1
		HTEC8-DV_17,19	Edge Card _36,38	<0.1	<0.1	<0.1
	10GbE (GSSG)	HTEC8-DV_18,20	Edge Card _12,14	0.42	0.26	0.13
		HTEC8-DV_18,20	Edge Card _17,19	<0.1	<0.1	<0.1
		HTEC8-DV_18,20	Edge Card _23,25	<0.1	<0.1	<0.1
		HTEC8-DV_18,20	Edge Card _24,26	0.37	0.23	0.11
	PCIe	HTEC8-DV_22,24	Edge Card _14,16	0.20	0.13	<0.1
		HTEC8-DV_22,24	Edge Card _17,19	<0.1	<0.1	<0.1
		HTEC8-DV_22,24	Edge Card _25,27	<0.1	<0.1	<0.1
		HTEC8-DV_22,24	Edge Card _30,32	0.19	0.12	<0.1

Table 3 - Propagation Delay (Mated Connector)		
10GbE	HTEC8-DV_17,19_Edge Card_17,19	58 ps
	HTEC8-DV_24,26_Edge Card_24,26	58 ps
10GbE (GSSG)	HTEC8-DV_12,14_Edge Card_12,14	56 ps
	HTEC8-DV_18,20_Edge Card_18,20	55 ps
	HTEC8-DV_23,25_Edge Card_23,25	56 ps
PCIe	HTEC8-DV_14,16_Edge Card_14,16	57 ps
	HTEC8-DV_22,24_Edge Card_22,24	57 ps
	HTEC8-DV_25,27_Edge Card_25,27	58 ps

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Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for differentially driven scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high-speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this connector, the following configurations were evaluated:

10GbE

1		5	7					17	19					29	31				39
T	G	S	S	G	T	T	G	S	S	G	T	T	G	S	S	G	T	T	G
T	G	T	T	G	S	S	G	T	T	G	S	S	G	T	T	G	S	S	T
2					12	14					24	26					36	38	40

10GbE (GSSG)

1								17	19		23	25							39
T	G	T	T	G	T	T	G	S	S	G	S	S	G	T	T	G	T	T	G
T	G	T	T	G	S	S	G	S	S	G	S	S	G	T	T	G	T	T	G
2					12	14		18	20		24	26							40

PCIe

1								17	19			25	27						39
T	T	G	G	T	T	G	G	S	S	G	G	S	S	G	G	T	T	G	G
G	G	T	T	G	G	S	S	G	G	S	S	G	G	S	S	G	G	T	T
2						14	16			22	24			30	32				40

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

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Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 100 ps.

For this report, measured rise times were at 20%-80% signal levels.

Frequency Domain Data
Frequency Domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data
Time Domain parameters indicate Impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Keysight Advanced Design System to obtain the time domain response. Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 50 mils of PCB trace on the HTEC8 and Edge Card side each. Delay is measured at 100 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio

Series: HTEC8
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is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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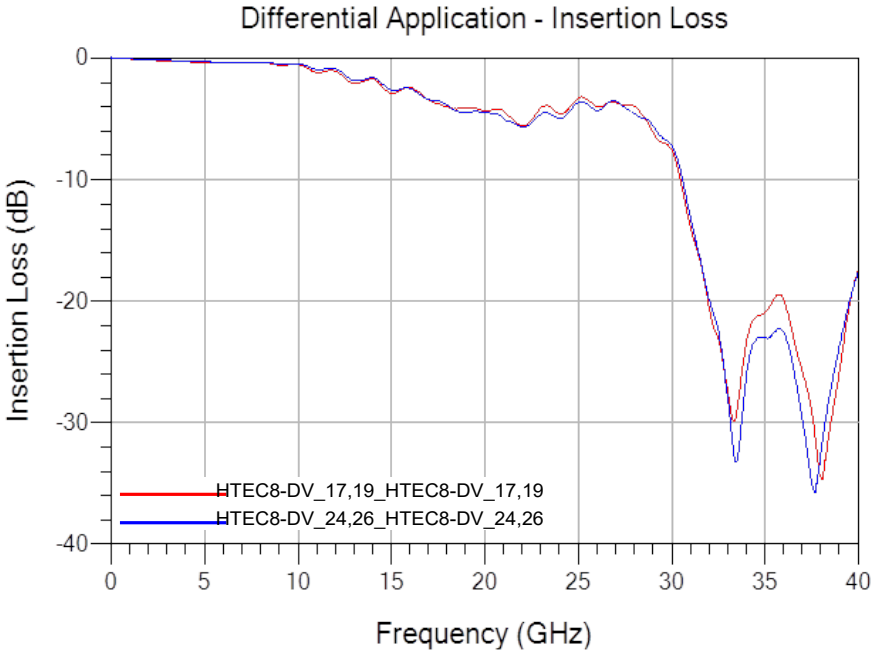
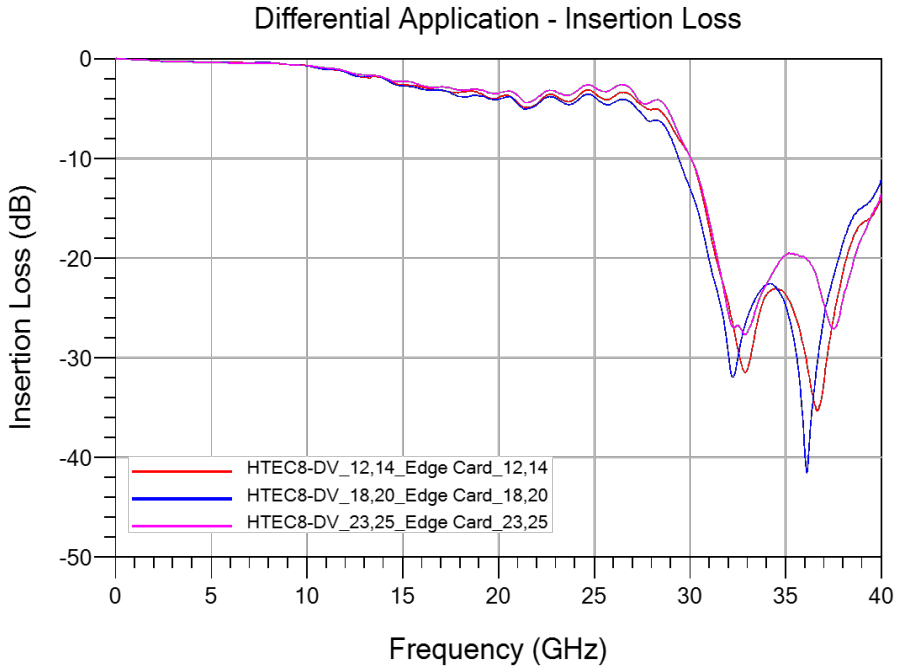
Appendix A – Frequency Domain Responses

Differential Application – Insertion Loss

10GbE



10GbE (GSSG)



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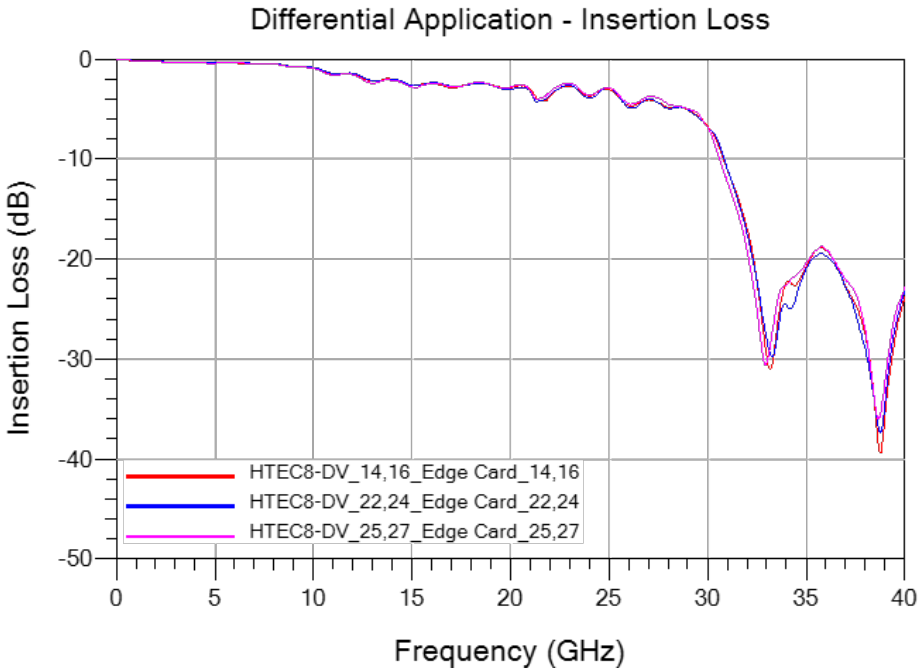
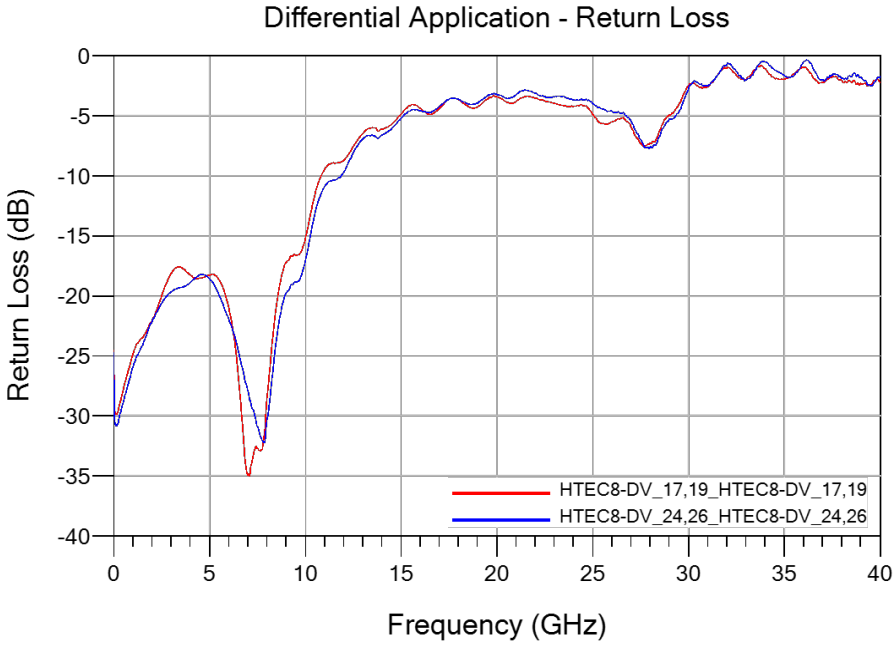
PCIe



Differential Application – Return Loss

10GbE



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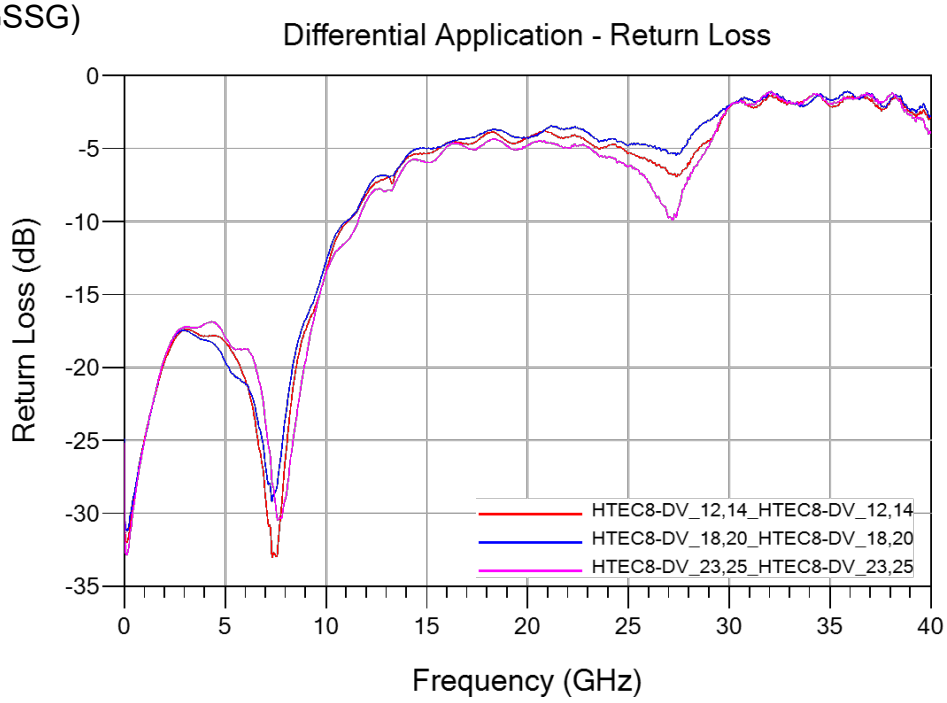
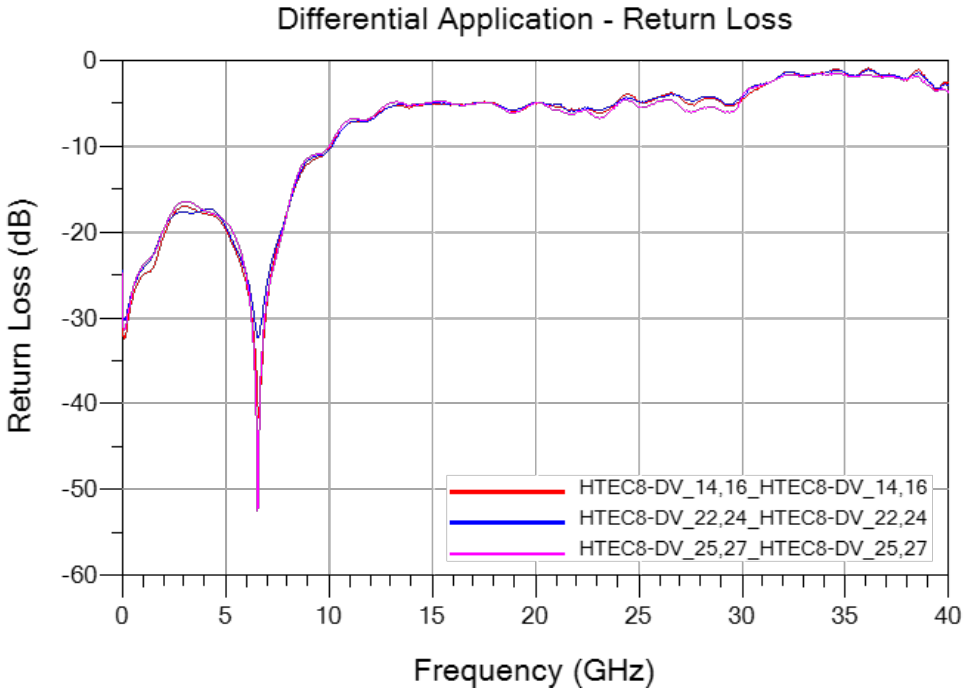
10GbE (GSSG)



PCIe



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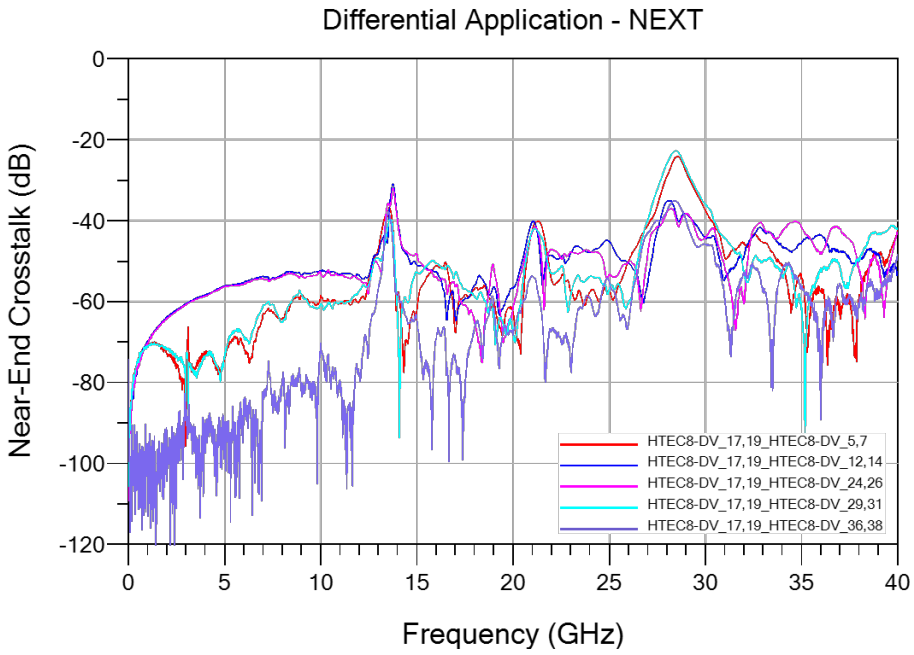
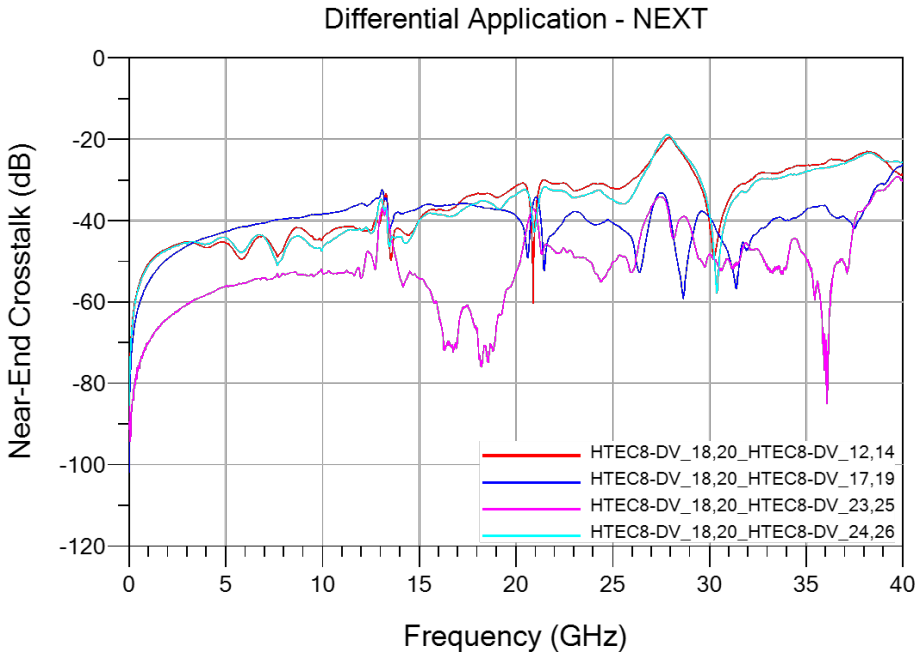
Differential Application – NEXT Configurations

10GbE



10GbE (GSSG)



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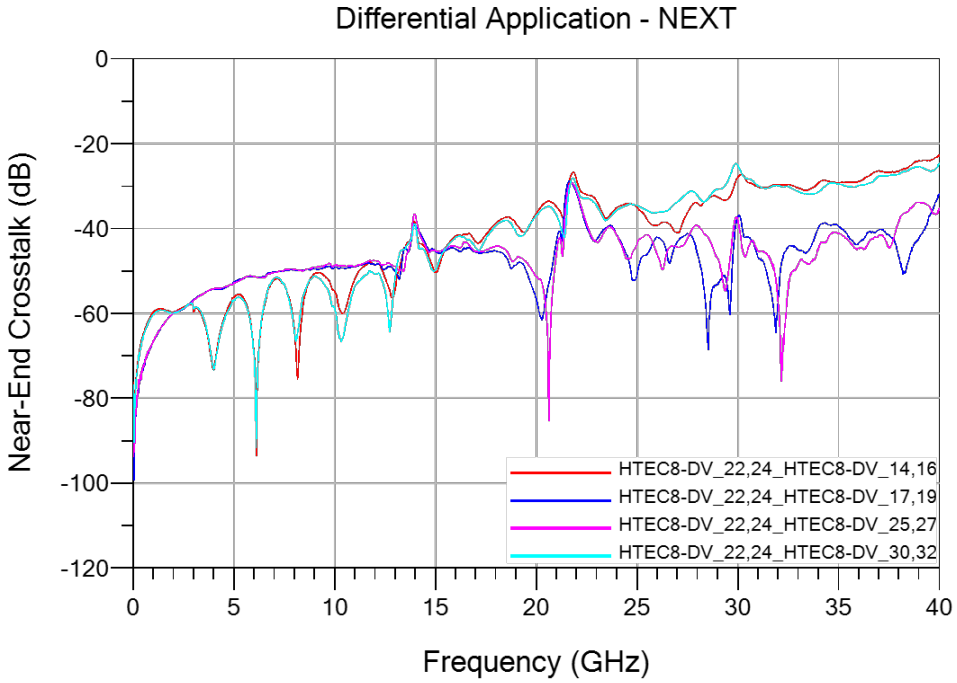
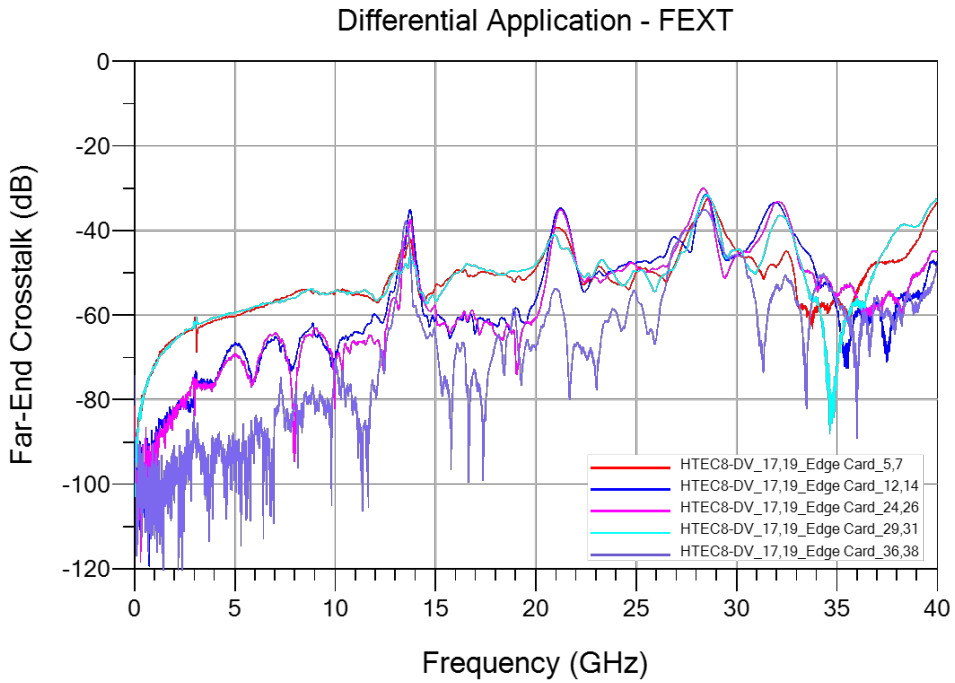
PCIe



Differential Application – FEXT Configurations
10GbE



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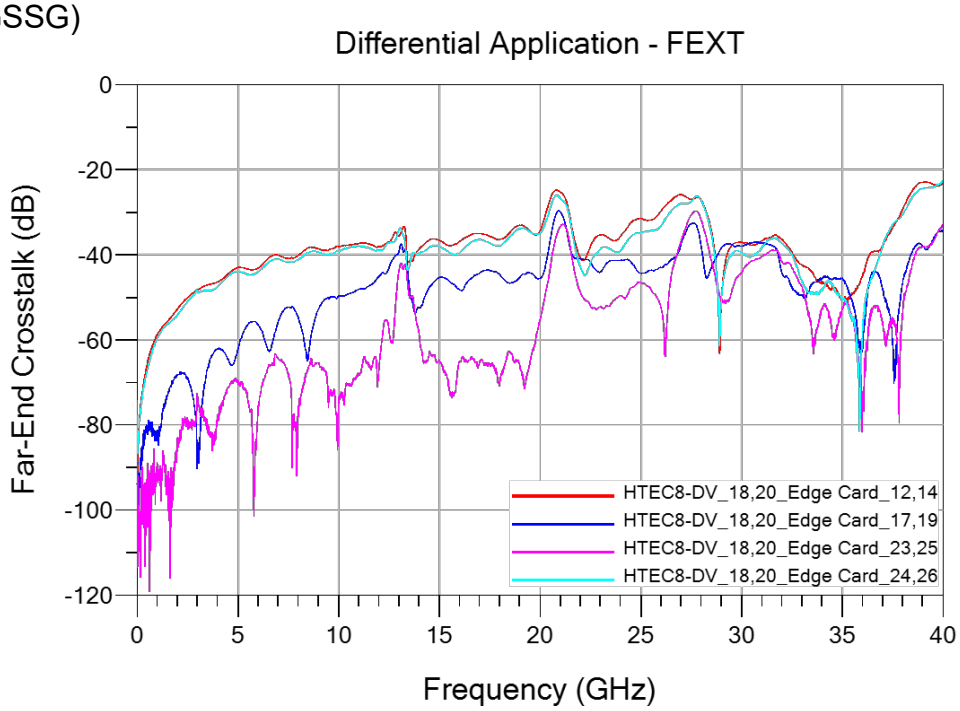
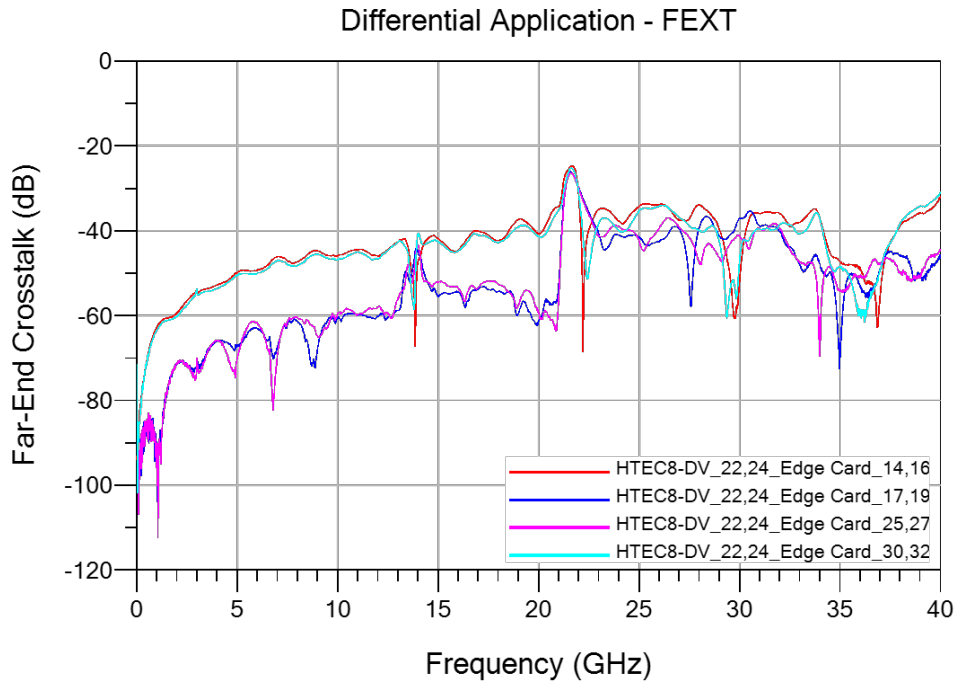
10GbE (GSSG)



PCIe



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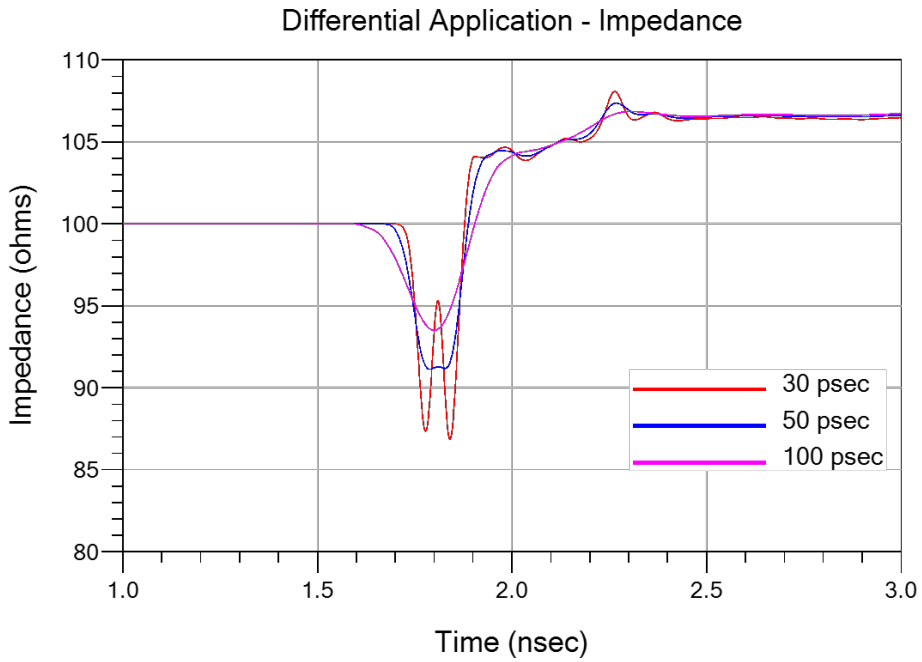
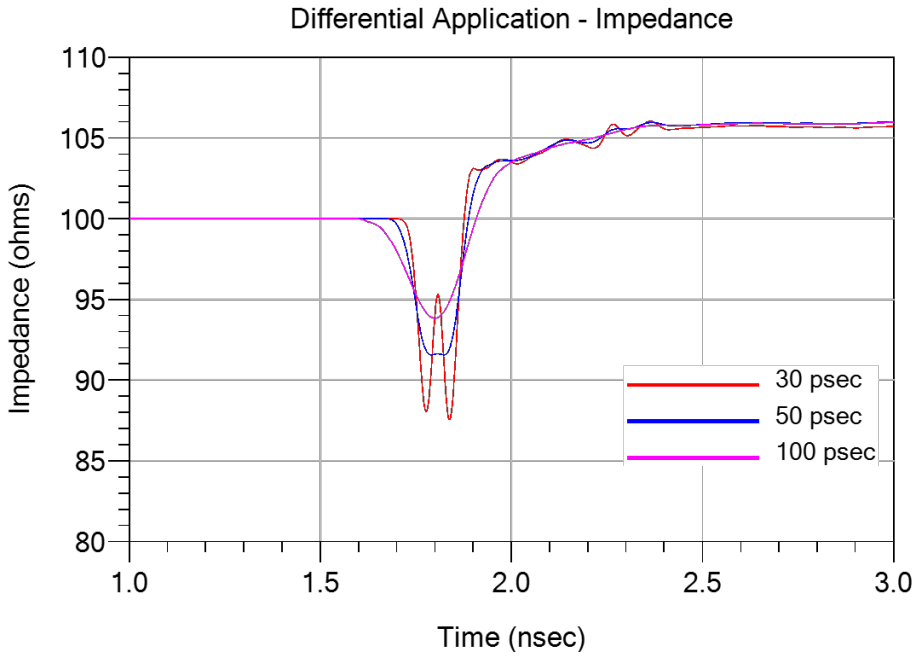
Appendix B – Time Domain Responses

Differential Application – Impedance

10GbE, HTEC8-DV_17,19



10GbE, HTEC8-DV_24,26



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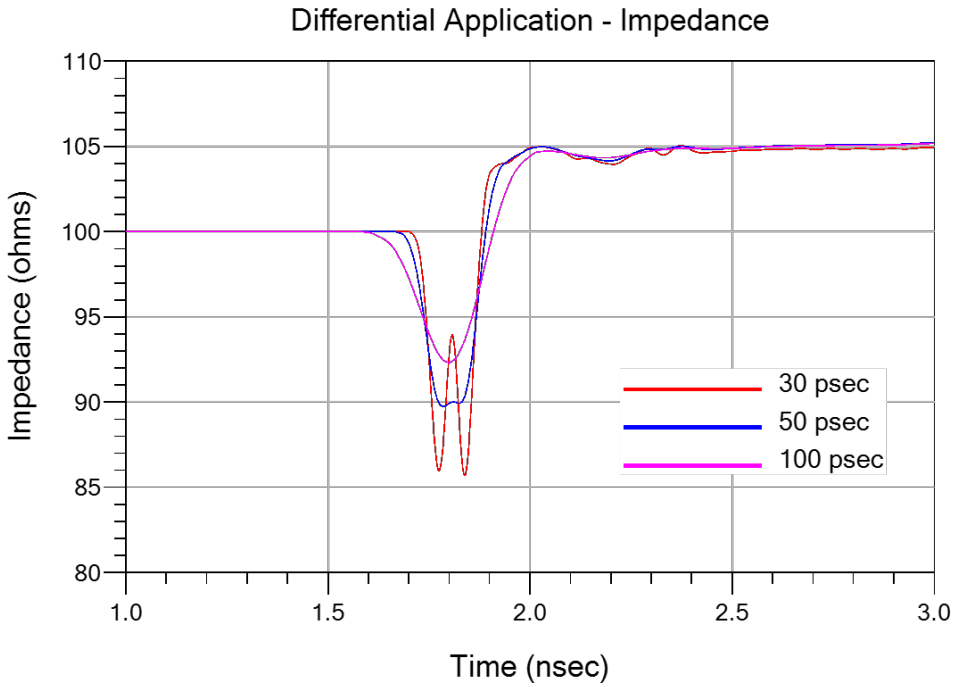
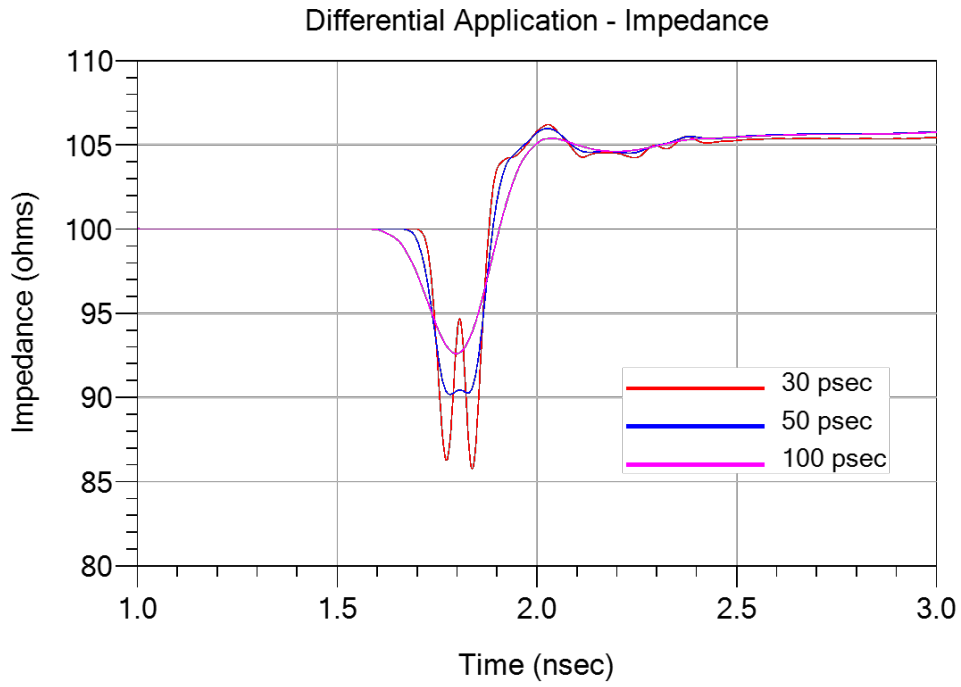
10GbE (GSSG), HTEC8-DV_12,14



10GbE (GSSG), HTEC8-DV_18,20



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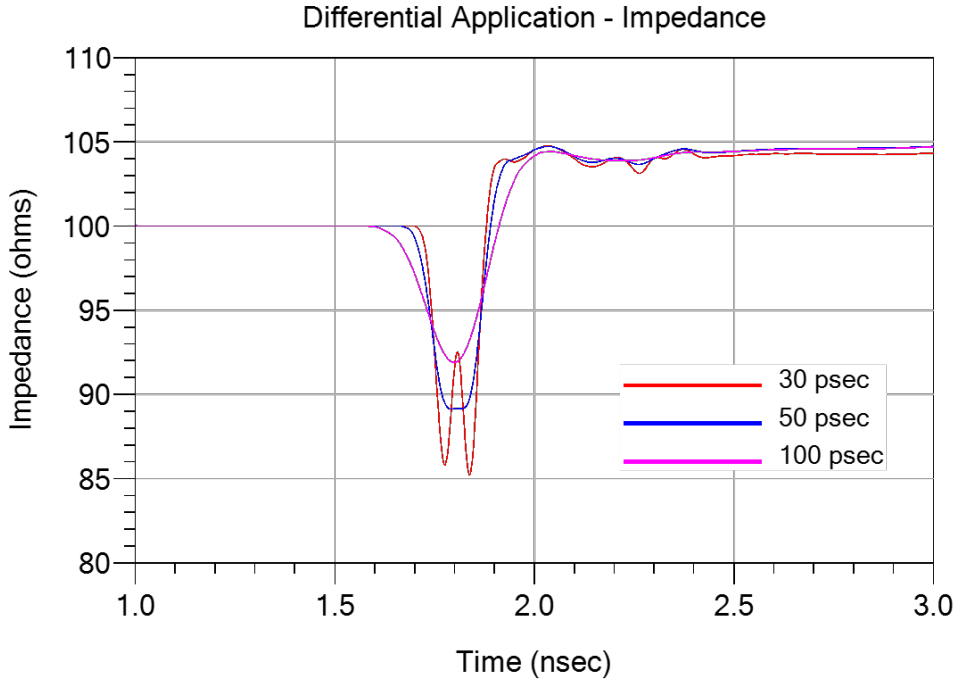
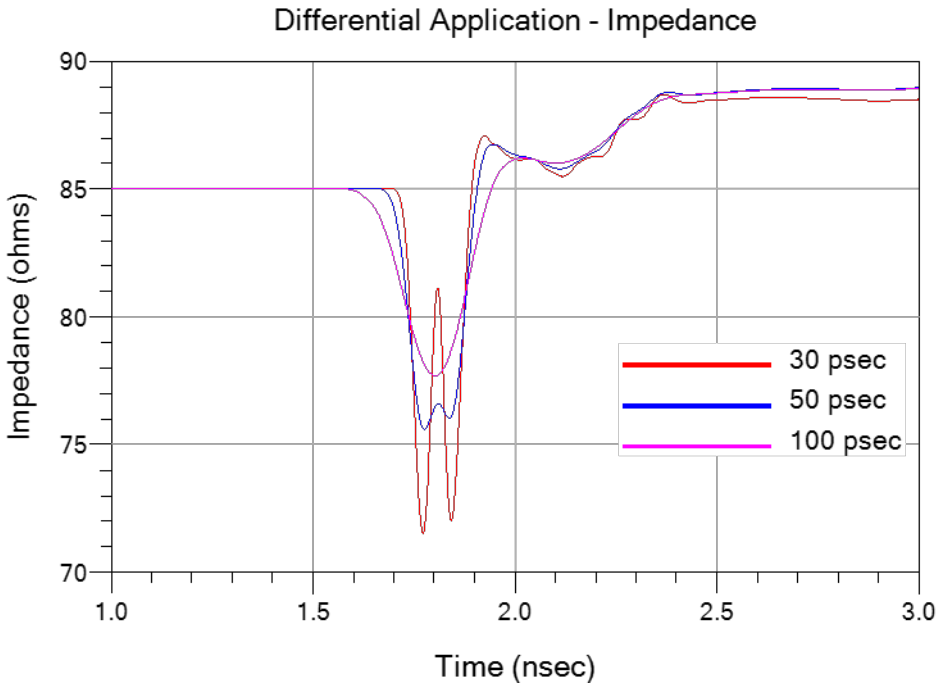
10GbE (GSSG), HTEC8-DV_23,25



PCIe, HTEC8-DV_14,16



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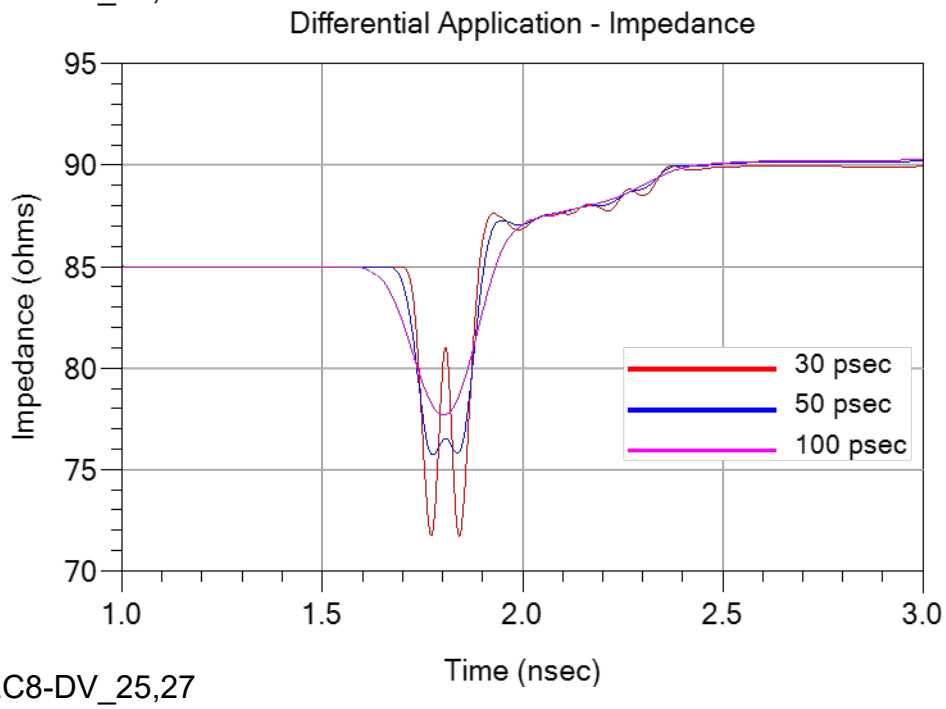
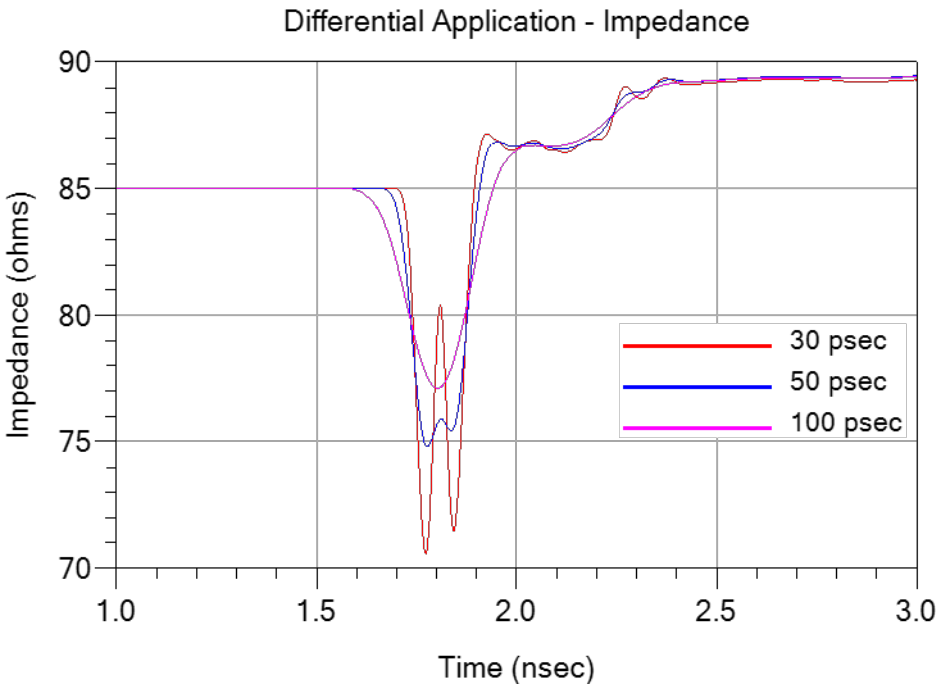
PCIe, HTEC8-DV_22,24



PCIe, HTEC8-DV_25,27



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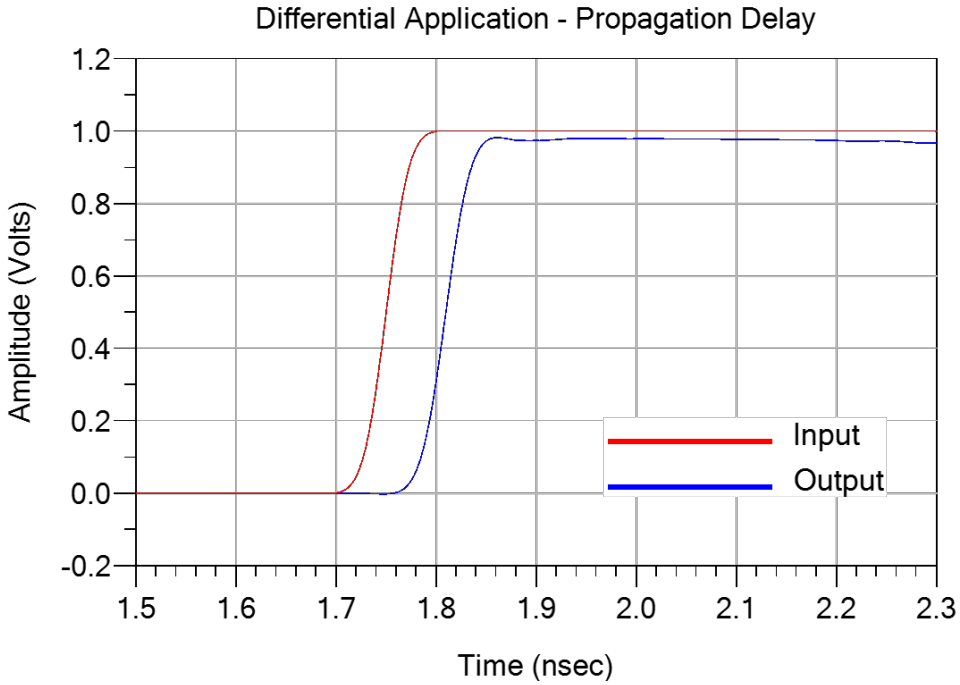
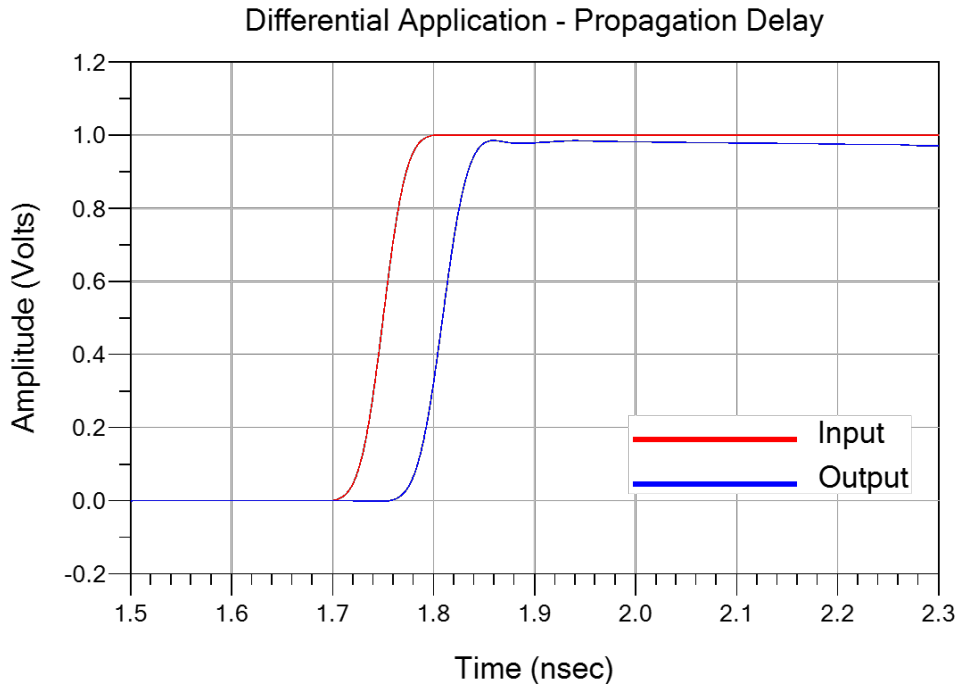
Differential Application – Propagation Delay

10GbE, HTEC8-DV_17,19_Edge Card_17,19



10GbE, HTEC8-DV_24,26_Edge Card_24,26



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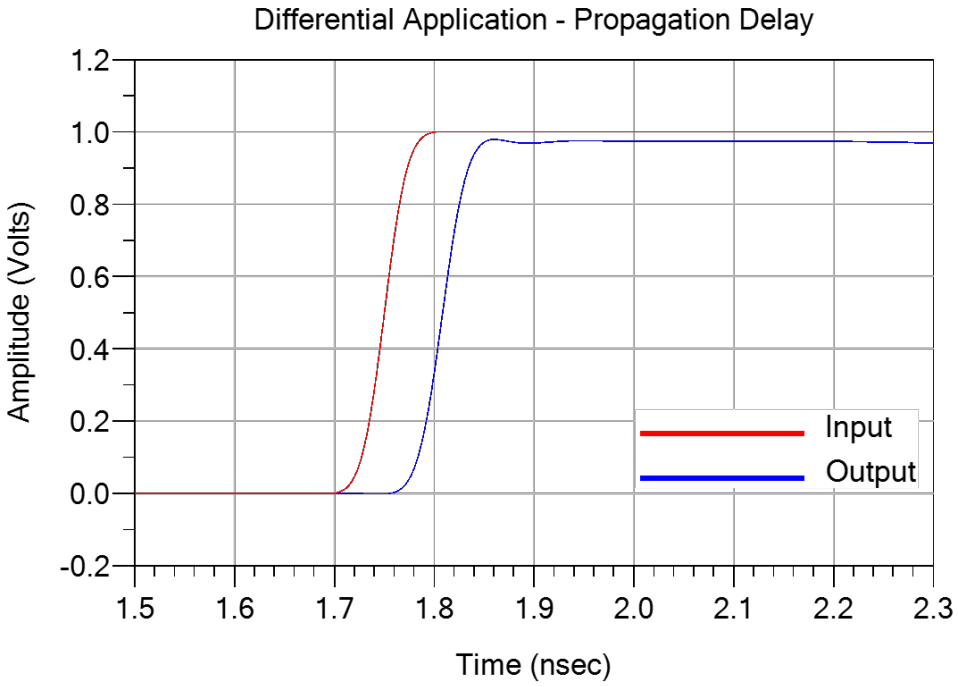
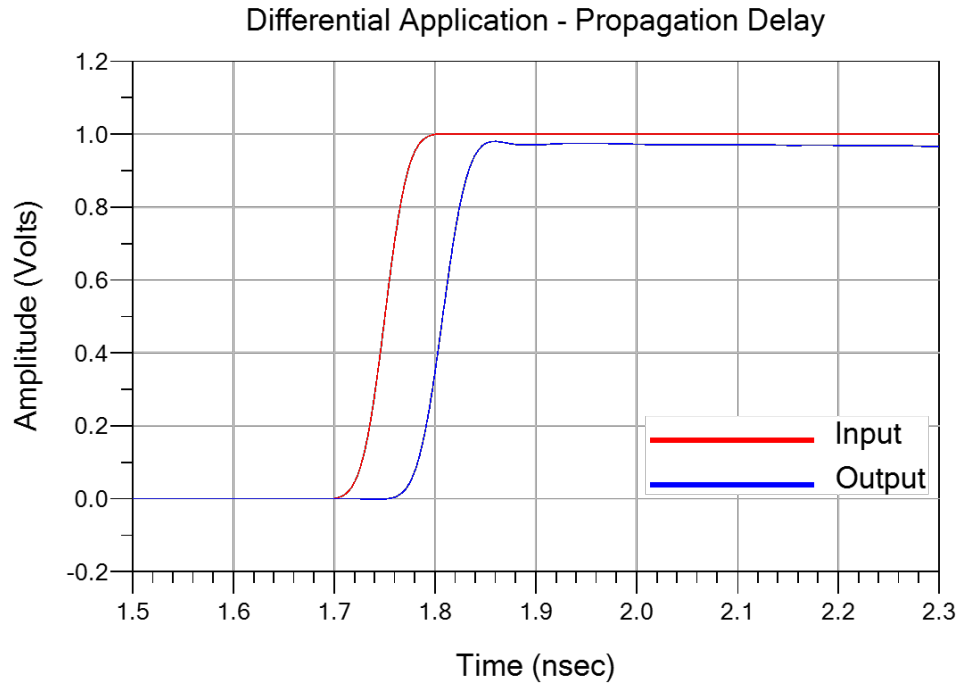
10GbE (GSSG), HTEC8-DV_12,14_Edge Card_12,14



10GbE (GSSG), HTEC8-DV_18,20_Edge Card_18,20



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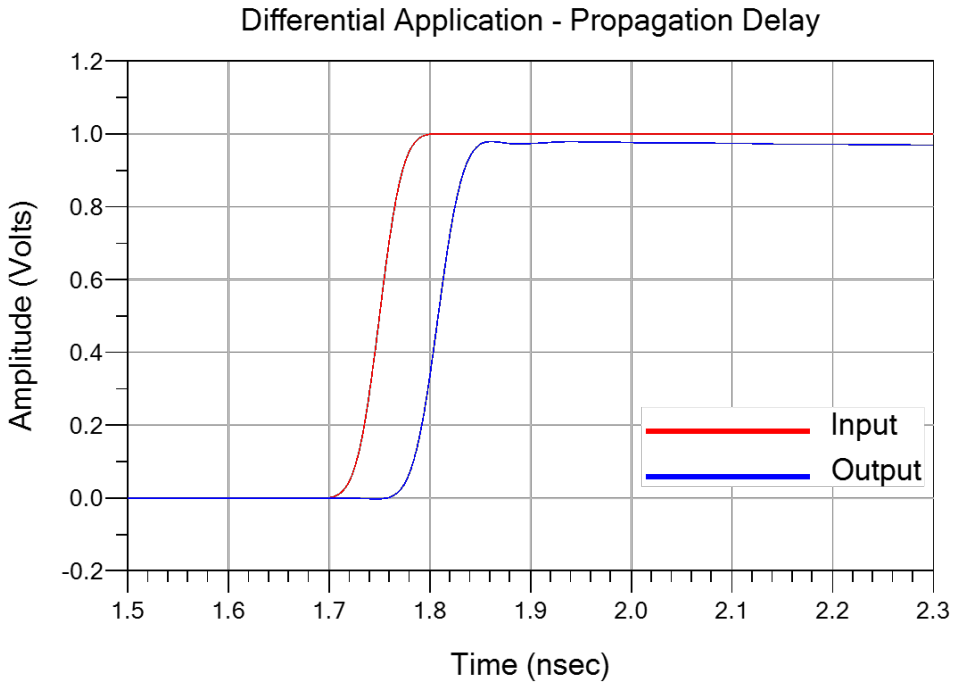
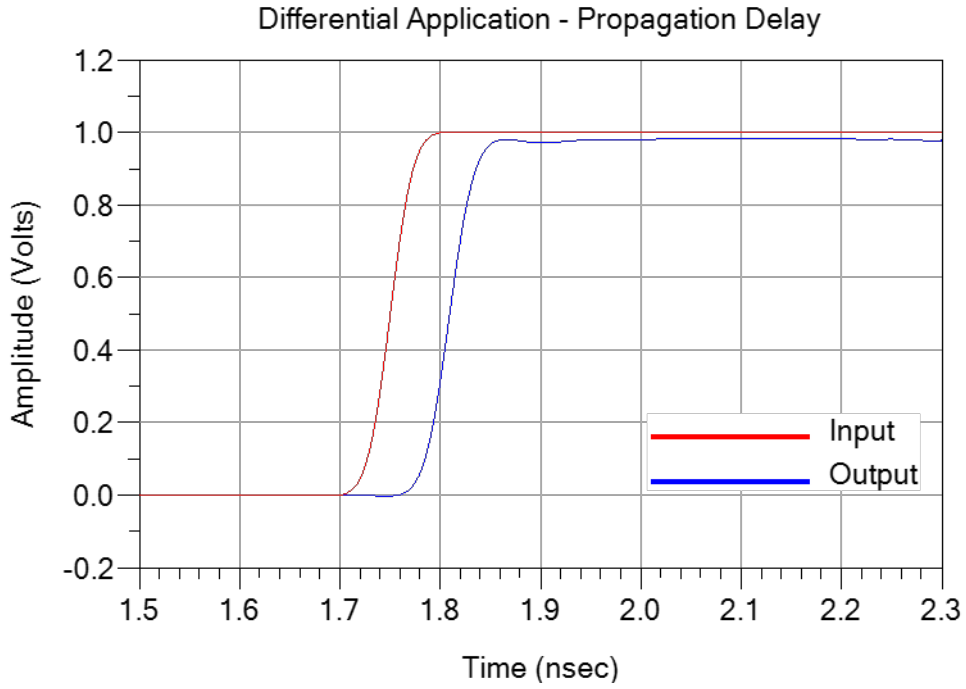
Description: 0.80 mm Rugged High-Speed Edge Card Connector

10GbE (GSSG), HTEC8-DV_23,25_Edge Card_23,25

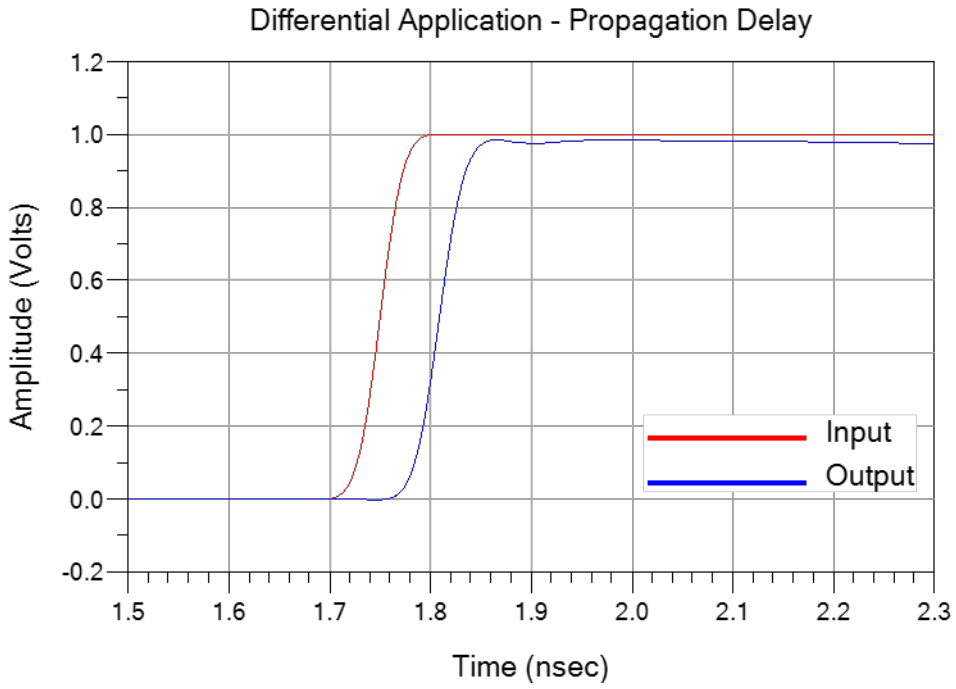


PCIe, HTEC8-DV_14,16_Edge Card_14,16

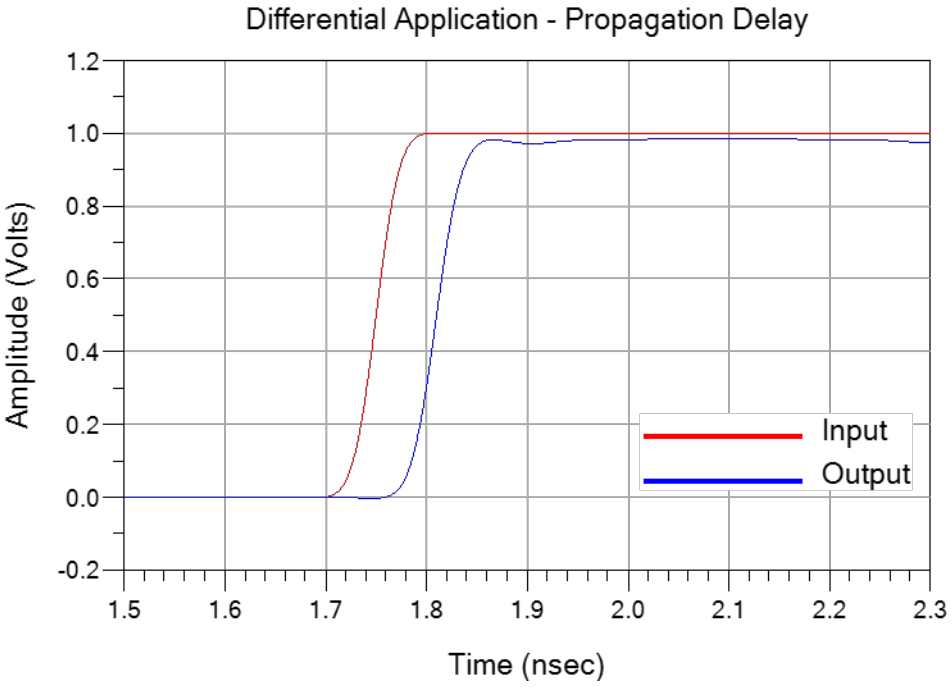


Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

PCIe, HTEC8-DV_22,24_Edge Card_22,24



PCIe, HTEC8-DV_25,27_Edge Card_25,27



Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

Appendix C – Product and Test System Descriptions

Product Description

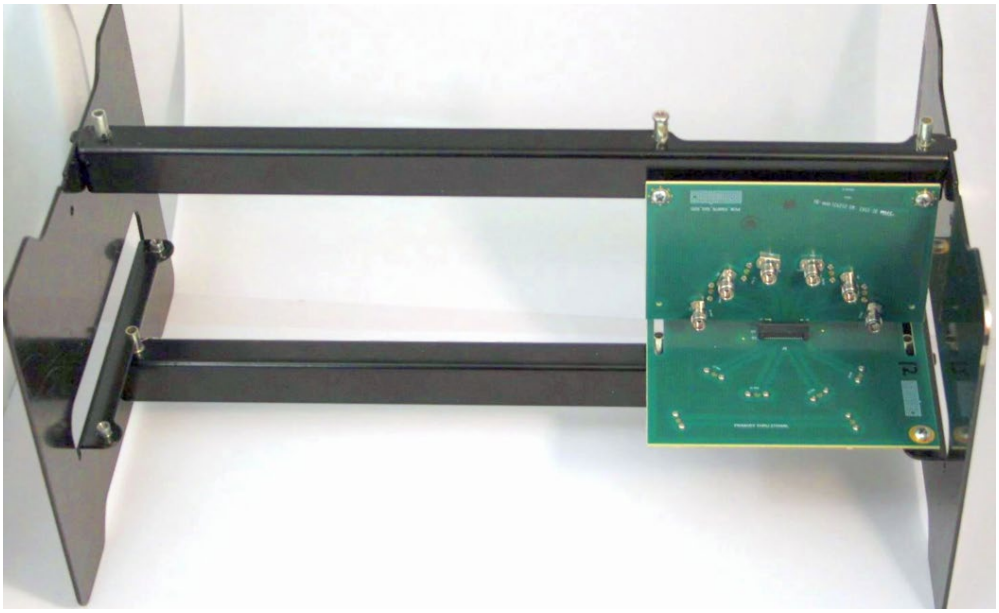
Product test samples are HTEC8 Series connectors. The part number is HTEC8-120-01-L-DV-A-WT. The HTEC8 Series connector are surface mount products. Each connector has two rows of contacts evenly spaced on a 0.8mm (0.0315") pitch.
A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of eight-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount SMA connector is used to interface the PNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. One fixture is specific to the HTEC8 series connector set and identified by part numbers PCB-106676-SIG-01A,B to PCB-106676-SIG-03A,B. Calibration standards specific to the HTEC8 series are located on the same boards.

PCB-106676-SIG-XX Test Fixtures

Shown below is a photograph of the one of the three test board sets.

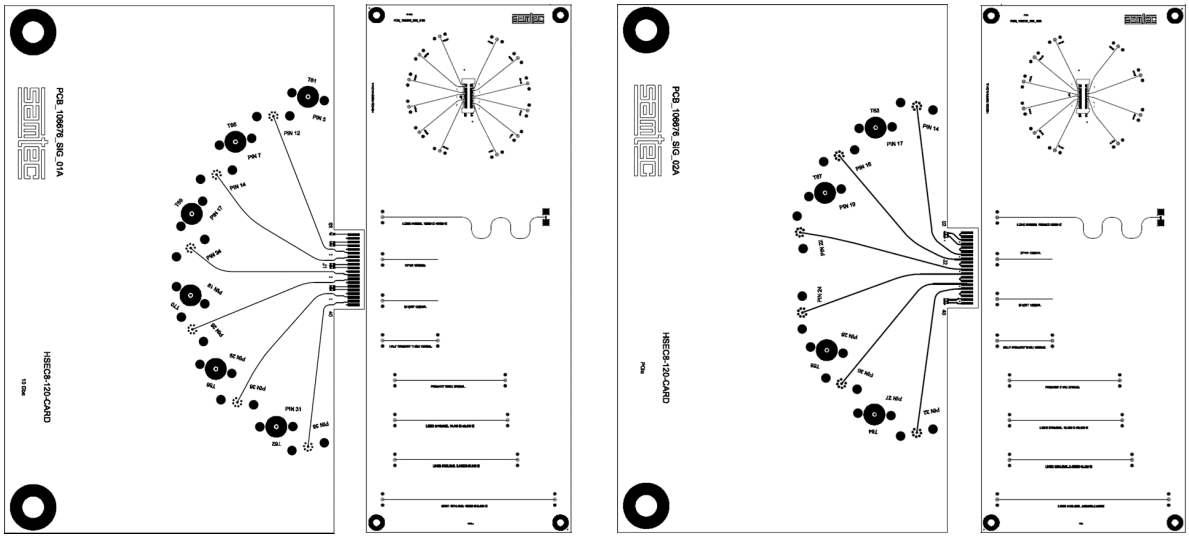


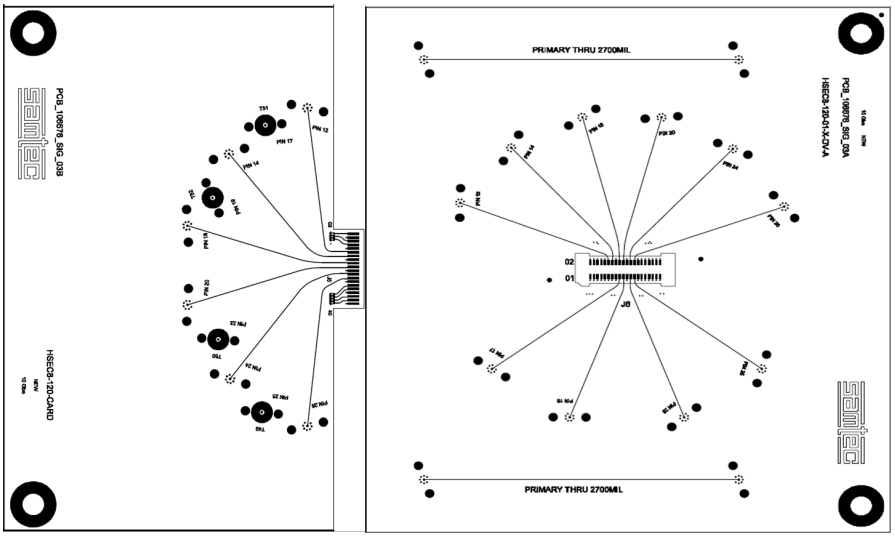
Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

PCB Fixtures

The test fixtures used are as follows:

PCB-106676-SIG-01A – Edge Card 10 GbE Test Board
PCB-106676-SIG-01B – HTEC8 Series 10 GbE Test Board
PCB-106676-SIG-02A – Edge Card PCIe Test Board
PCB-106676-SIG-02B – HTEC8 Series PCIe Test Board
PCB-106676-SIG-03A – HTEC8 Series 10 GbE (GSSG) Test Board
PCB-106676-SIG-03B – Edge Card 10 GbE (GSSG) Test Board



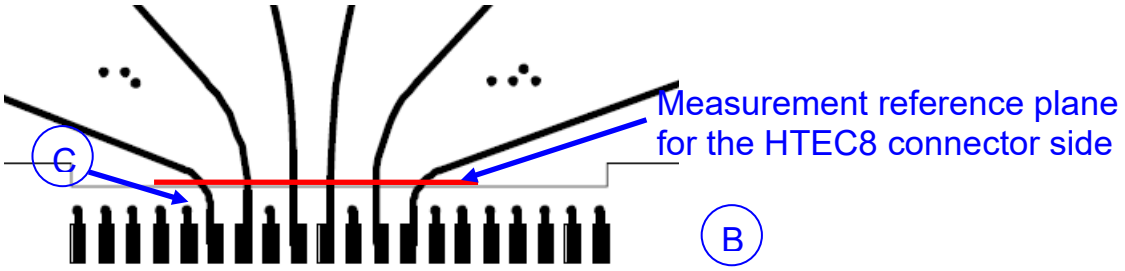


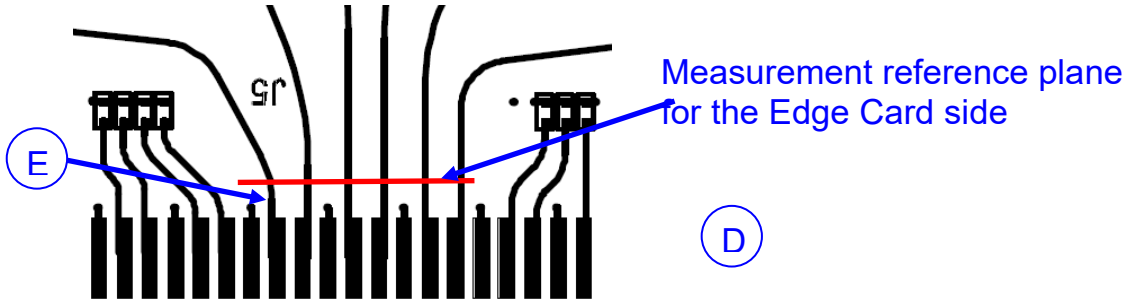
Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

All traces on the test boards are length matched to 2750 mils measured from the edge of the pad to the SMA. The TRL calibration effectively removes 2700 mils of test board trace effects. This means that 50 mils of test board trace length effects are included in both sides of test boards in the measurement. The S-Parameter measurement includes:

A- The HTEC8 Series connector set
B- Test board vias, pads (footprint effects) for the HTEC8 connector side.
C- 50 mils of 8.5 mil wide microstrip trace.
D- Test board vias, pads (footprint effects) for the Edge Card side.
E- 50 mils of 8.5 mil wide microstrip trace.

The figure below shows the location of the measurement reference plane.





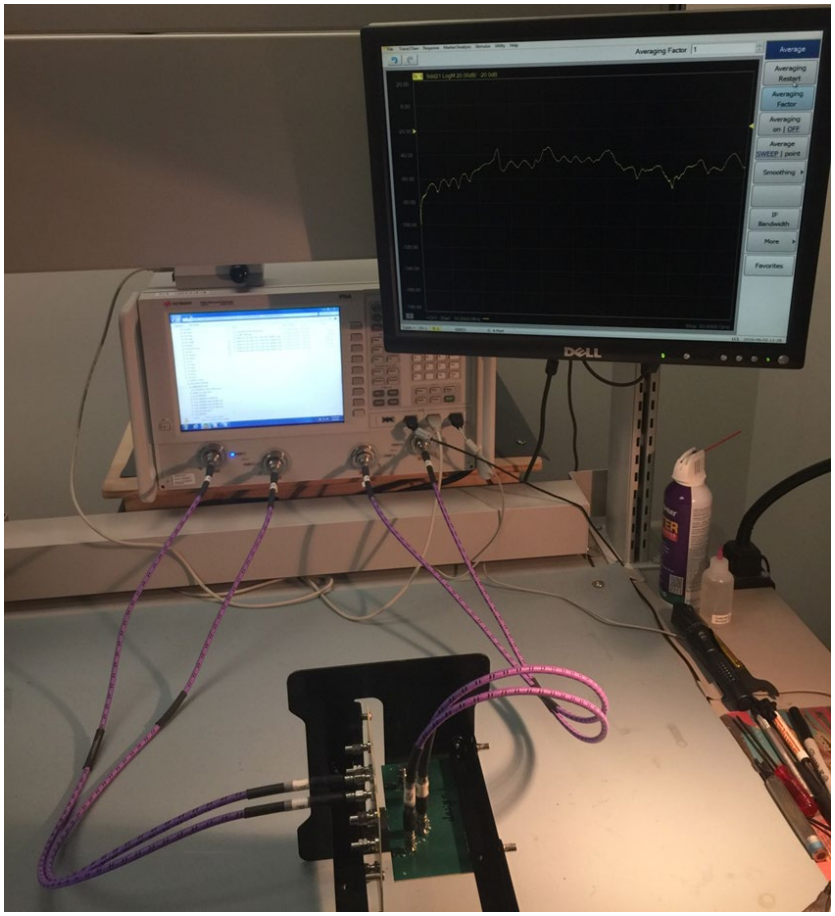
Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

Appendix D – Test and Measurement Setup

The test instrument is the Keysight N5225B PNA network analyzer with Keysight U3044A M16 Multiport Test set and Keysight U3044A M12 Multiport Test set. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Keysight ADS. The network analyzer is configured as follows:

Start Frequency – 10 MHz
Stop Frequency – 40 GHz
Step – 10 MHz
IFBW – 1 KHz

N5225B Measurement Setup



Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

Test Instruments

QTY	Description
1	Keysight N5225B PNA Network Analyzer (10 MHz to 50 GHz)
1	Keysight N4433A U3044A M16 Multiport Test Set (10 MHz to 40 GHz)
1	Keysight N4433A U3044A M12 Multiport Test Set (10 MHz to 40 GHz)
1	Keysight N4694-60003 E-Cal Module (10 MHz to 67 GHz)

Test Cables & Adapters

QTY	Description
4	Junkosha 2.92mm Cables (DC to 40 GHz)

Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the LRM calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the LRM calibration standards. A coaxial SOLT calibration is performed using an N4694 ecal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the reflect and 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid.

From the LRM calibration standard measurements, a user defined calibration kit is developed and stored in the network analyzer. Calibration is then performed on all 4 ports following the calibration wizard within the Keysight N5225B. This calibration is saved and can be recalled at any time. Calibration takes roughly 30 minutes to perform.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2017. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)
A step pulse is applied to the touchstone model of the connector and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Series: HTEC8
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Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Series: HTEC8
Description: 0.80 mm Rugged High-Speed Edge Card Connector

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
Z – Impedance (expressed in ohms)