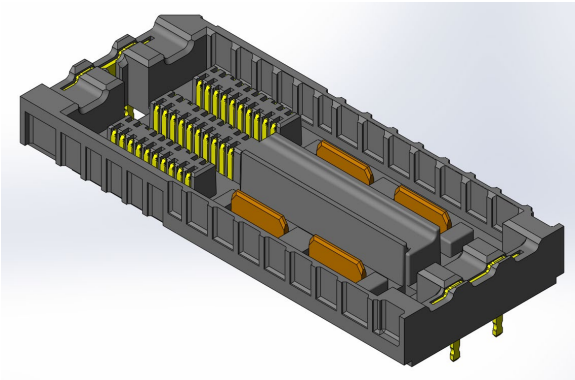
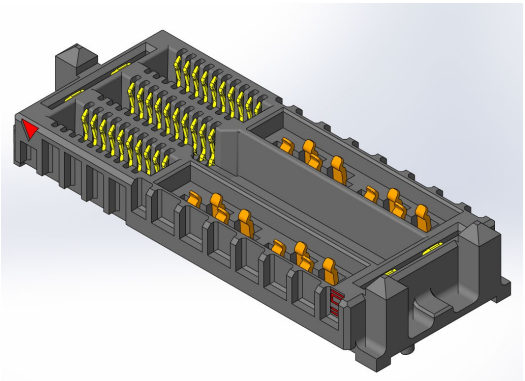
High Speed Characterization Report

UDM6-10-2-01.5-L-A-TH-TR



UDF6-10-2-03.5-L-A-TH-TR



Description:

0.635 mm Pitch AcceleRate® mP
High-Density, High-Speed Power/Signal Interconnect,
5mm Stack Height

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Connector Overview

The UDM6/UDF6 series is a 0.635 mm pitch interconnect that is part of the AcceleRate® mP High-Density, High-Speed Power/Signal interconnect family. The UDM6/UDF6 series is currently available with 2 or 4 power blades and 60 or 240 signal pins (6 rows with either 10 or 40 signal positions per row).

UDx6 supports 64 Gbps PAM4 (32 Gbps NRZ) applications and is PCIe® 6.0/CXL® 3.1 Capable. The data in the report is only for the 5mm mated stack height.

Frequency Domain Data Summary

Bandwidth Chart – Differential Insertion Loss

UDx6 Connector Series

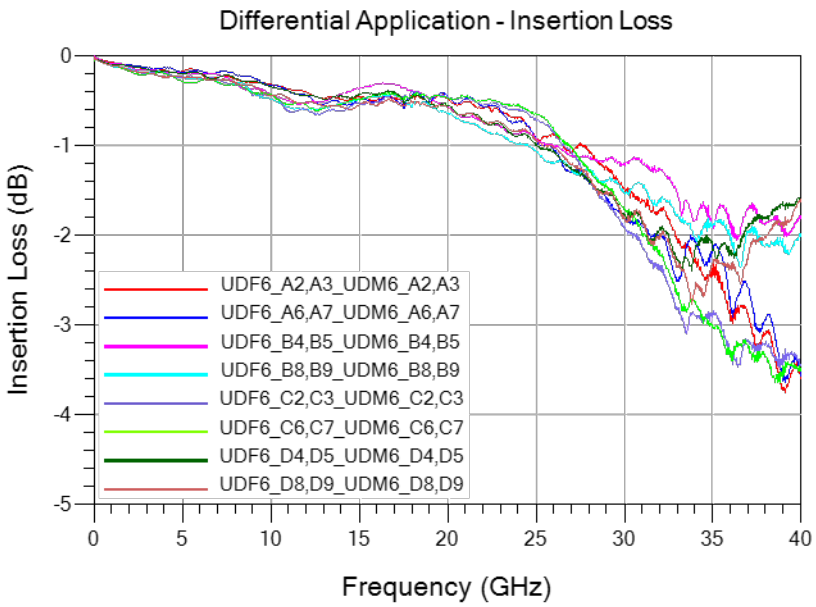

Figure 1

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Time Domain Data Summary

Table 1 - Differential Impedance (Ω)				
Driver	**Signal Rise-time**	**30ps**	**50ps**	**100ps**
UDM6_A2,A3	Maximum Impedance	106.8	106.1	104.9
	Minimum Impedance	89.8	90.0	90.8
UDM6_A6,A7	Maximum Impedance	105.4	105.1	105.0
	Minimum Impedance	90.1	90.3	90.6
UDM6_B4,B5	Maximum Impedance	105.2	105.1	104.5
	Minimum Impedance	89.8	90.3	90.6
UDM6_B8,B9	Maximum Impedance	105.2	104.9	104.3
	Minimum Impedance	90.3	90.4	90.9
UDM6_C2,C3	Maximum Impedance	105.6	105.1	104.4
	Minimum Impedance	90.8	91.1	91.4
UDM6_C6,C7	Maximum Impedance	105.5	105.1	105.0
	Minimum Impedance	89.9	90.4	91.1
UDM6_D4,D5	Maximum Impedance	105.7	105.6	105.6
	Minimum Impedance	91.7	91.8	92.1
UDM6_D8,D9	Maximum Impedance	105.3	105.3	105.3
	Minimum Impedance	91.8	92.1	92.5

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Table 2 - Differential Crosstalk (%)					
Input(tr)	**Driver**	**Receiver**	**30ps**	**50ps**	**100ps**
NEXT	UDF6_B8,B9	UDF6_C2,C3	<0.1	<0.1	<0.1
	UDF6_B8,B9	UDF6_C6,C7	0.13	<0.1	<0.1
	UDF6_B8,B9	UDF6_D4,D5	<0.1	<0.1	<0.1
	UDF6_B8,B9	UDF6_D8,D9	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDF6_A2,A3	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDF6_A6,A7	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDF6_B4,B5	0.16	0.11	<0.1
	UDF6_C6,C7	UDF6_B8,B9	0.13	<0.1	<0.1
FEXT	UDF6_B8,B9	UDM6_A2,A3	<0.1	<0.1	<0.1
	UDF6_B8,B9	UDM6_A6,A7	<0.1	<0.1	<0.1
	UDF6_B8,B9	UDM6_B4,B5	0.12	<0.1	<0.1
	UDF6_B8,B9	UDM6_C2,C3	<0.1	<0.1	<0.1
	UDF6_B8,B9	UDM6_C6,C7	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDM6_B4,B5	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDM6_B8,B9	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDM6_C2,C3	0.12	<0.1	<0.1
	UDF6_C6,C7	UDM6_D4,D5	<0.1	<0.1	<0.1
	UDF6_C6,C7	UDM6_D8,D9	<0.1	<0.1	<0.1

Table 3 - Propagation Delay (Mated Connector)	
UDF6_A2,A3_ UDM6_A2,A3	55 ps
UDF6_A6,A7_ UDM6_A6,A7	55 ps
UDF6_B4,B5_ UDM6_B4,B5	59 ps
UDF6_B8,B9_ UDM6_A2,A3	59 ps
UDF6_C2,C3_ UDM6_C2,C3	59 ps
UDF6_C6,C7_ UDM6_C6,C7	59 ps
UDF6_D4,D5_ UDM6_D4,D5	56 ps
UDF6_D8,D9_ UDM6_D8,D9	55 ps

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended driven scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high-speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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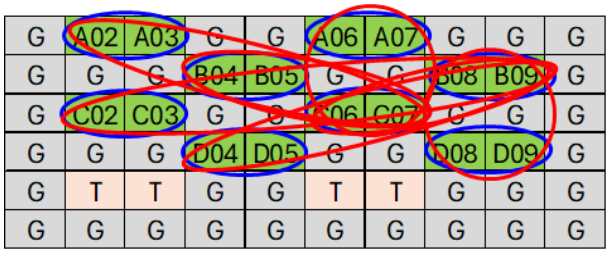
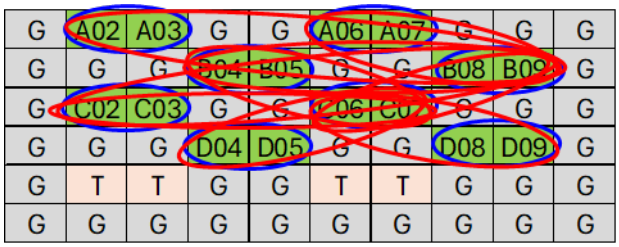
For this connector, the following configurations were evaluated:



NEXT



FEXT

Differential Impedance (denoted by blue circles)**:**

- GSSG (Ground-positive Signal-negative Signal-Ground)

Differential Crosstalk (denoted by red circles)**:**

- In row: from the terminals to the other terminals on the same row.
- Across row: from one row of terminals to the other row of terminals.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance. In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 100 ps.

For this report, measured rise times were at 20%-80% signal levels.

Frequency Domain Data
Frequency Domain parameters are helpful in evaluating the connector system’s signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or

Series: UDM6 / UDF6
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S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data
Time Domain parameters indicate Impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Keysight Advanced Design System to obtain the time domain response. Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 1.5 mm of PCB trace on both the UDM6 and UDF6 each. Delay is measured at 100 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Appendix A – Frequency Domain Responses

Differential Application – Insertion Loss

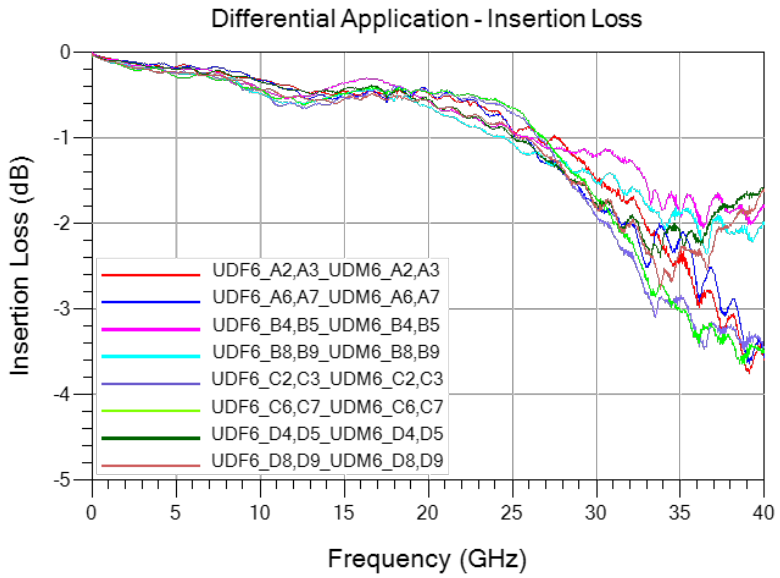


Figure 2

Differential Application – Return Loss

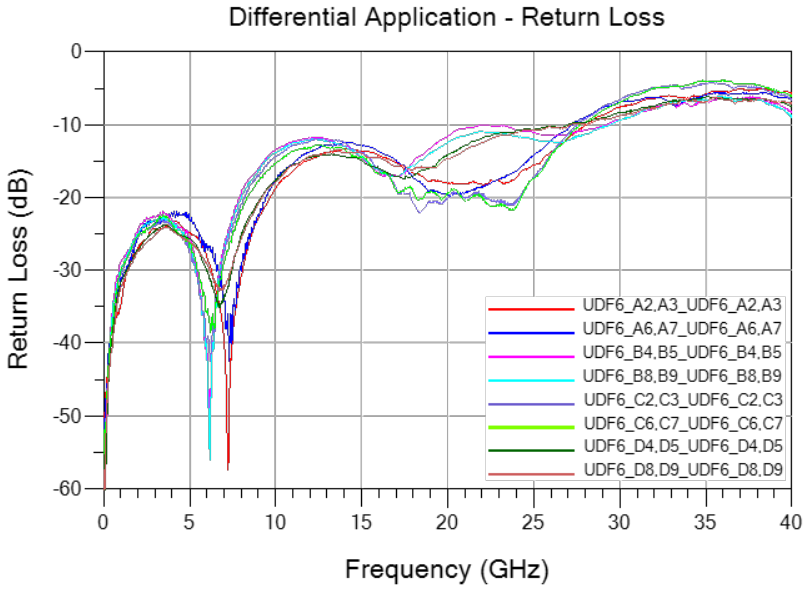


Figure 3

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Differential Application – NEXT Configurations

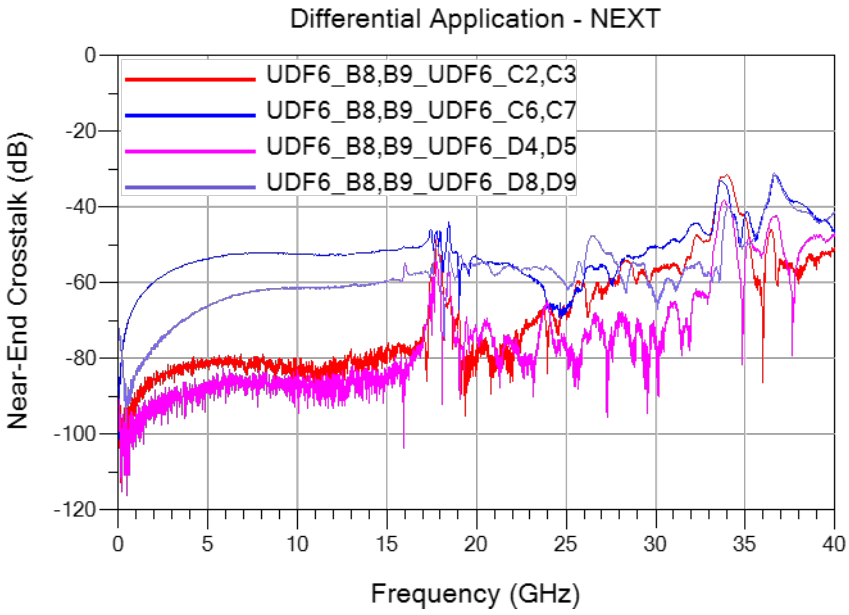


Figure 4

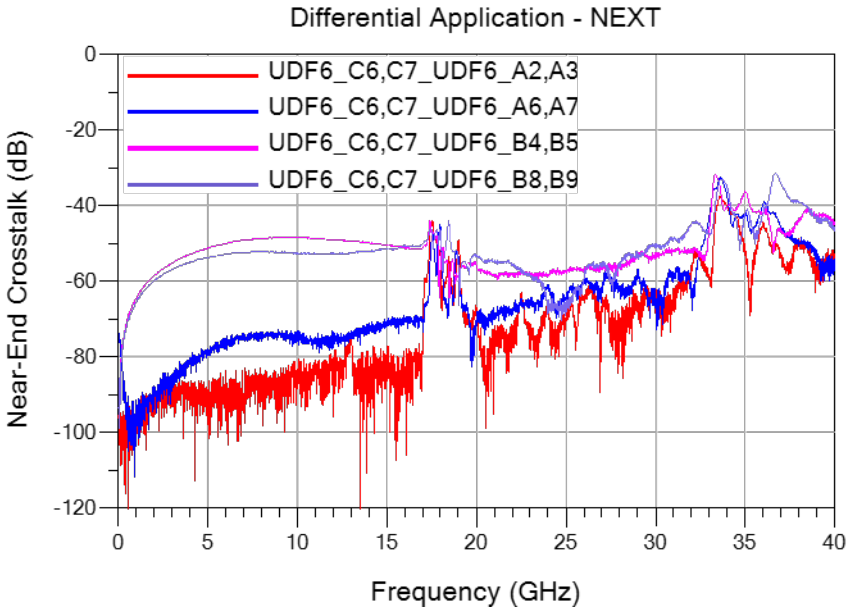


Figure 5

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Differential Application – FEXT Configurations

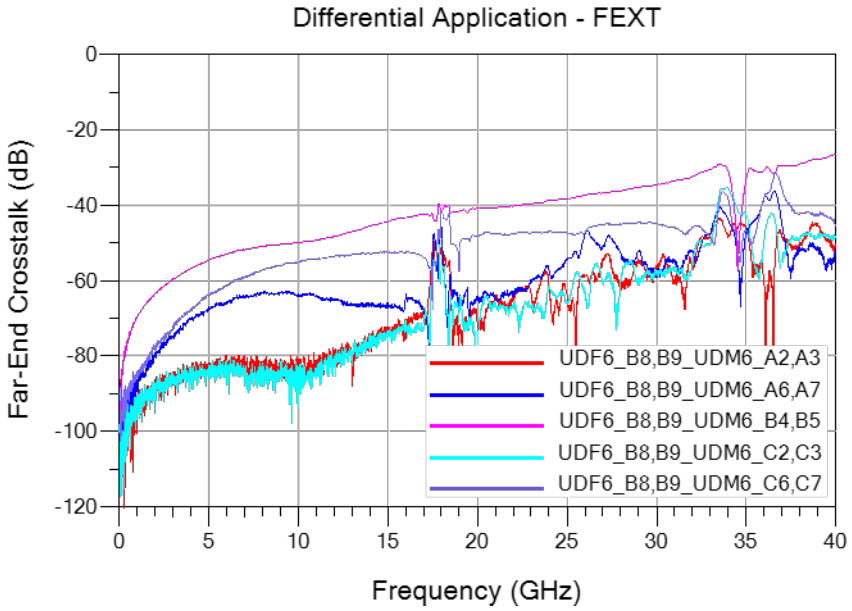


Figure 6

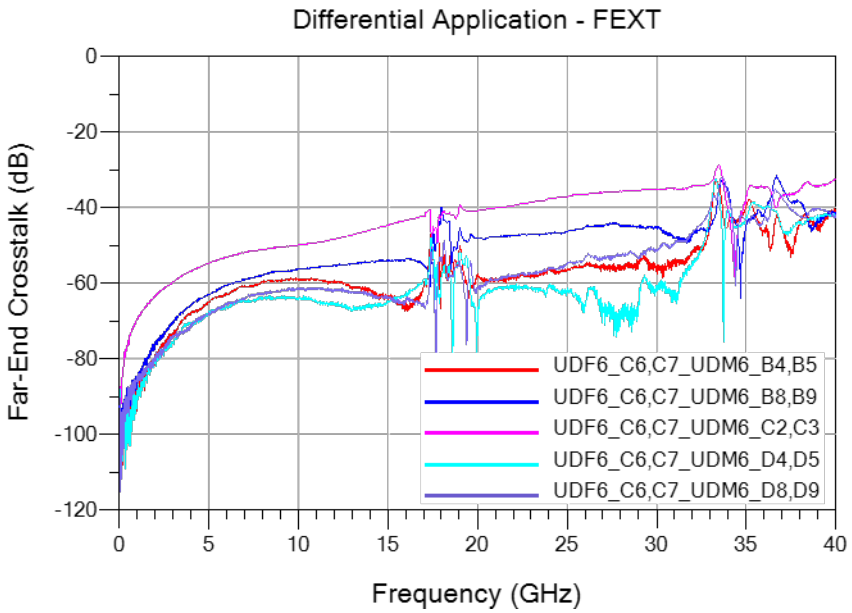
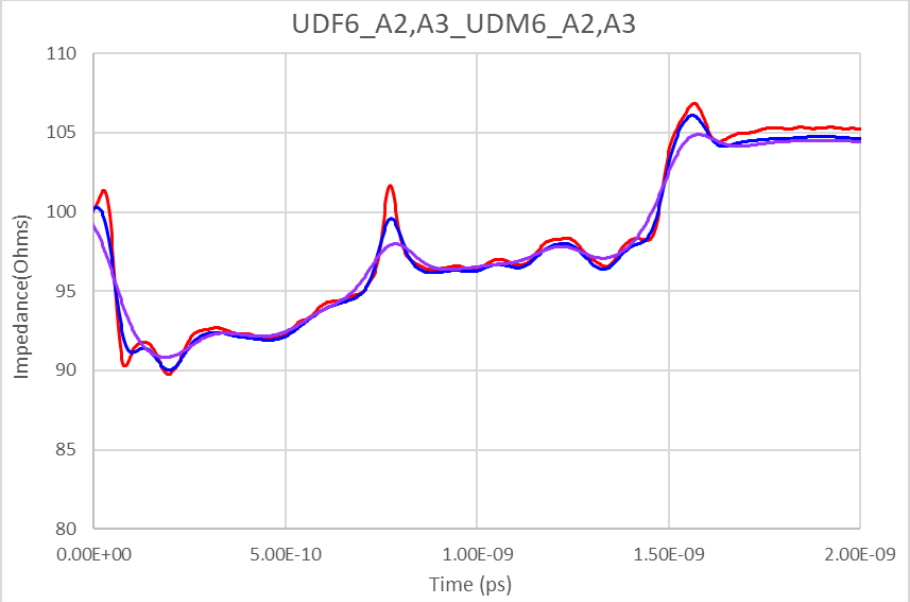


Figure 7

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Appendix B – Time Domain Responses

Differential Application – Impedance



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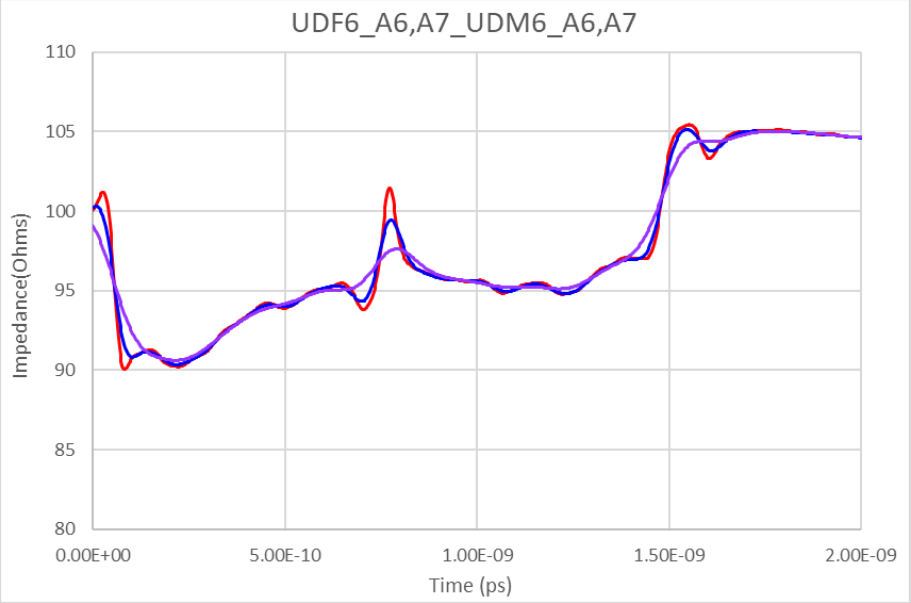

Figure 9

Series: UDM6 / UDF6
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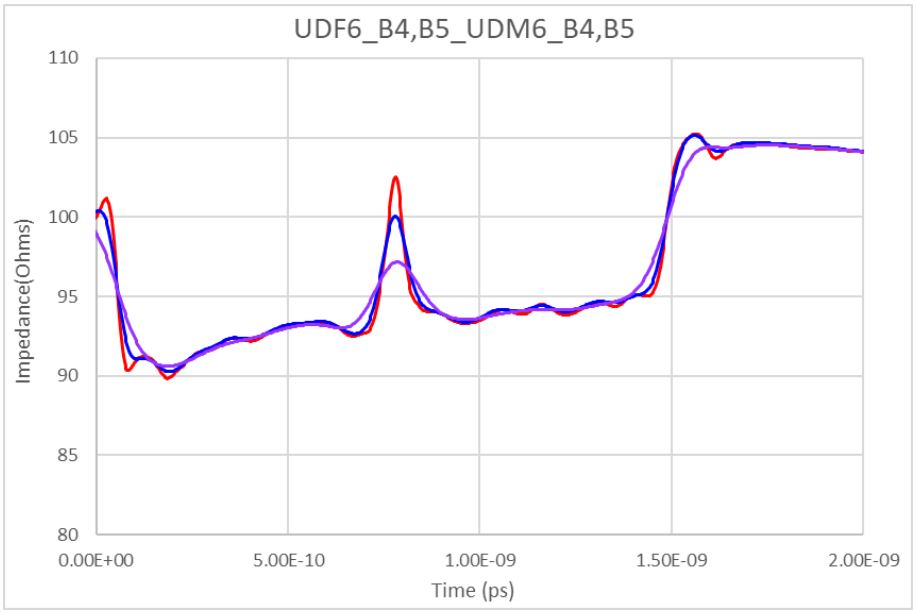

Figure 10

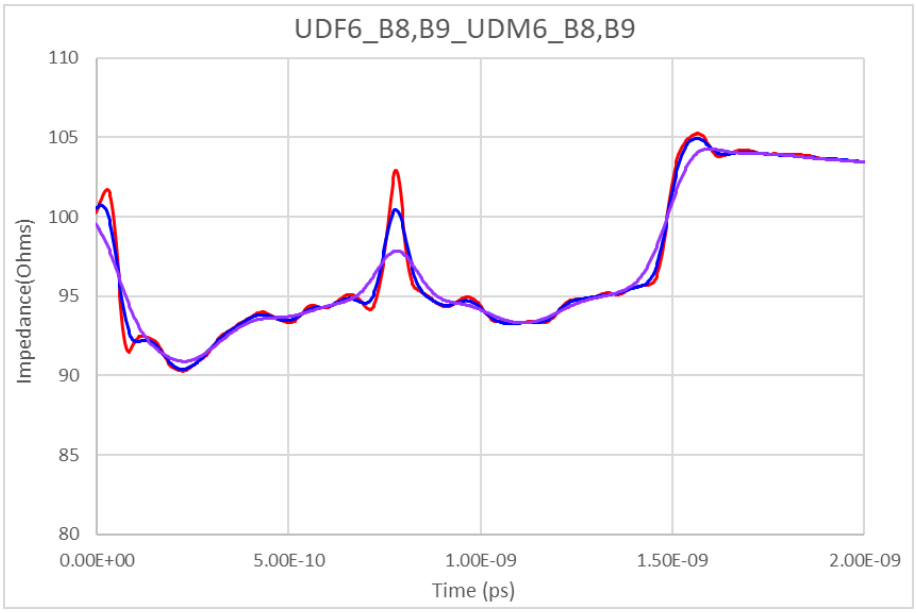

Figure 11

Series: UDM6 / UDF6
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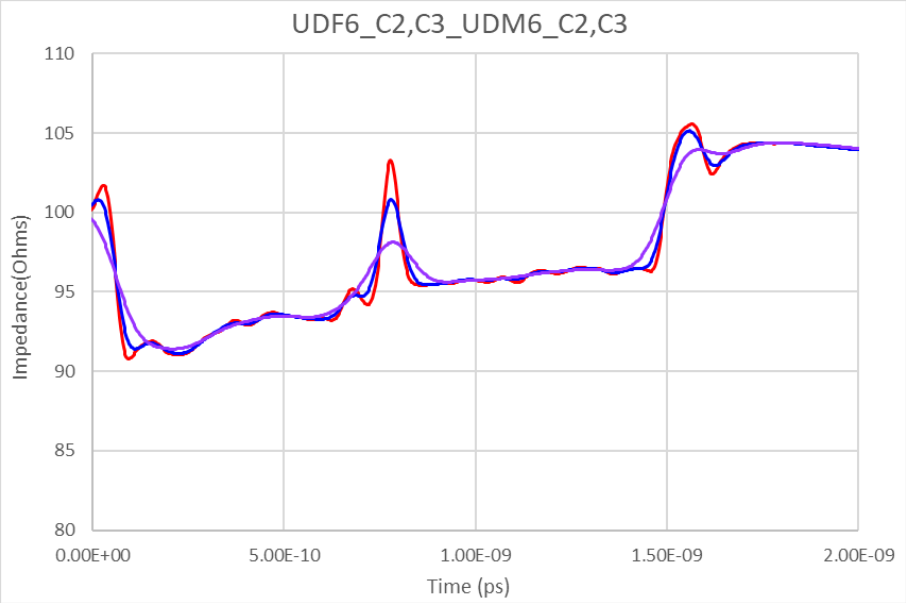

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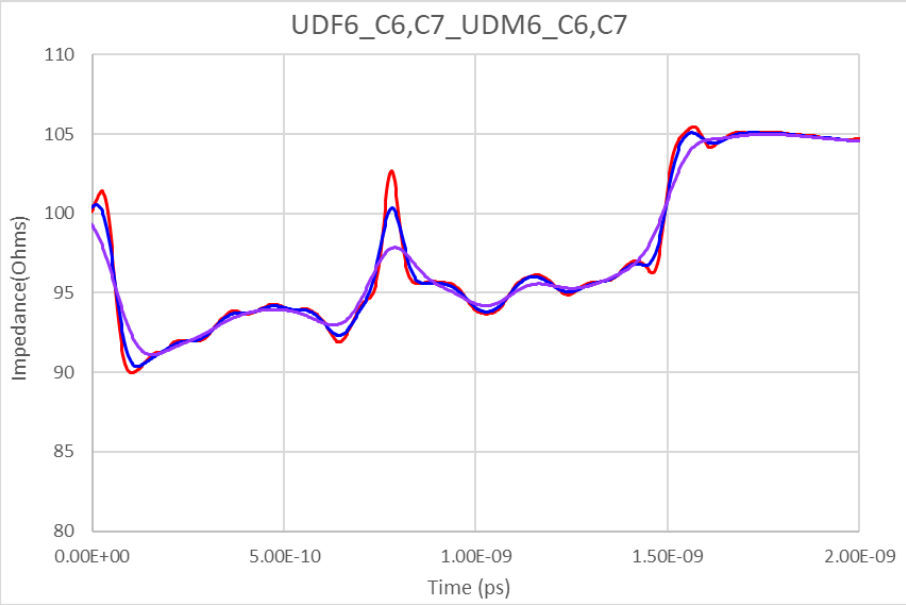
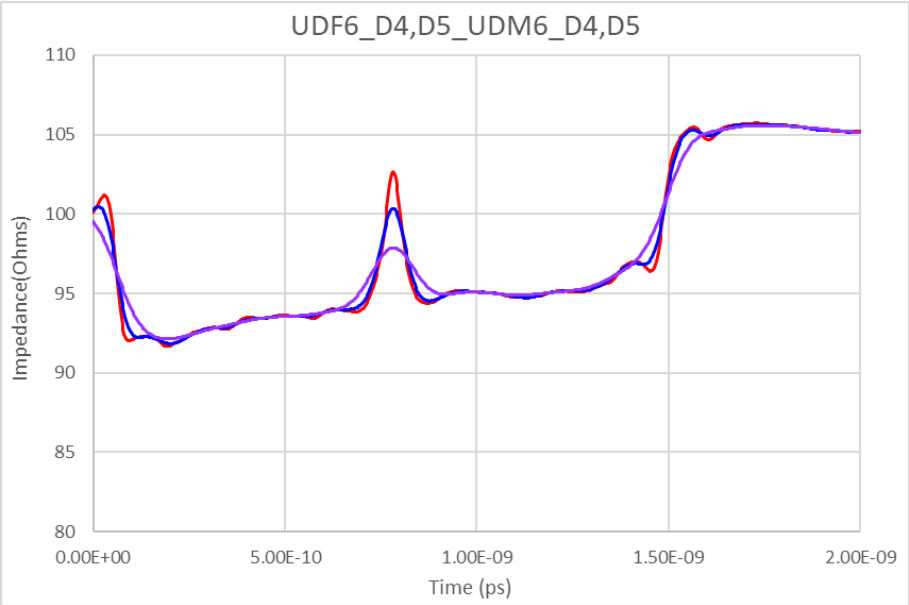


Figure 13

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height



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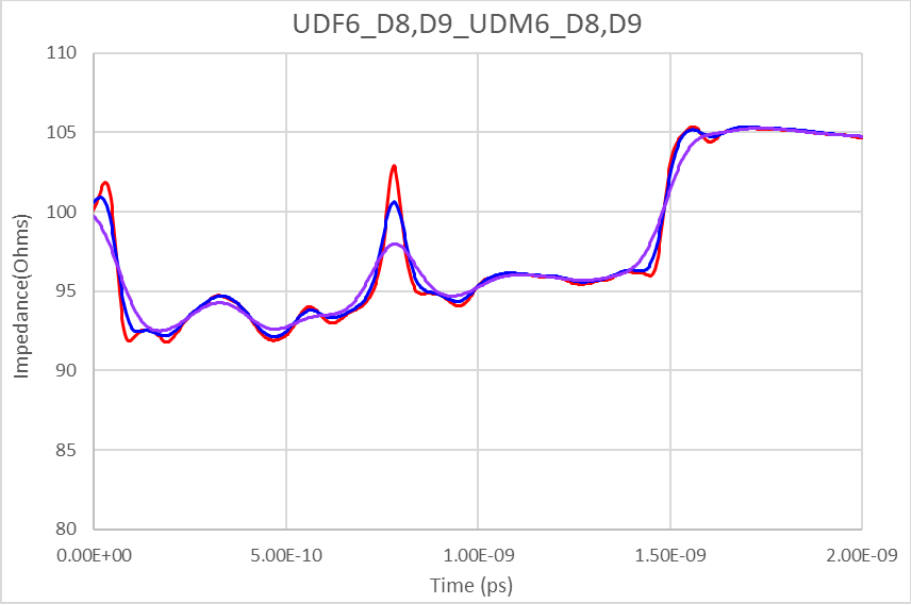

Figure 15

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Differential Application – Propagation Delay

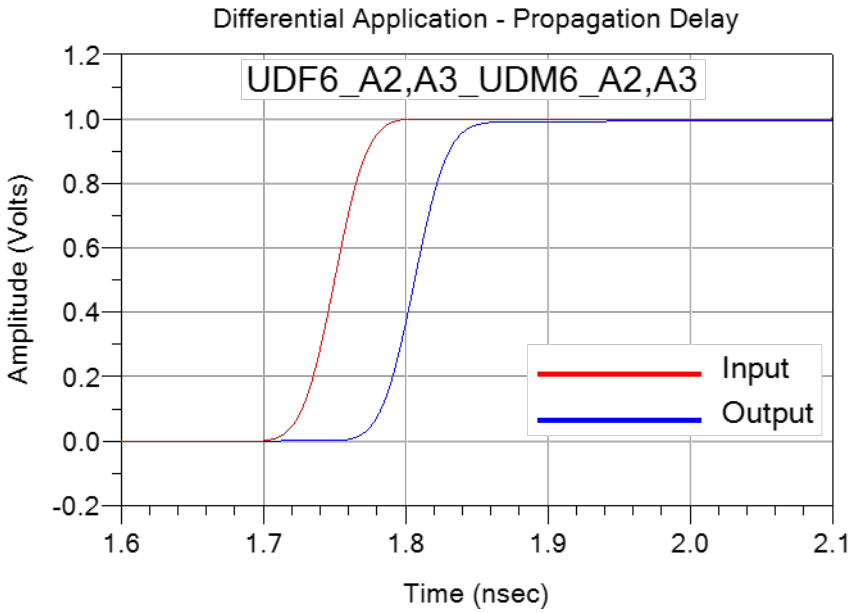

Figure 16

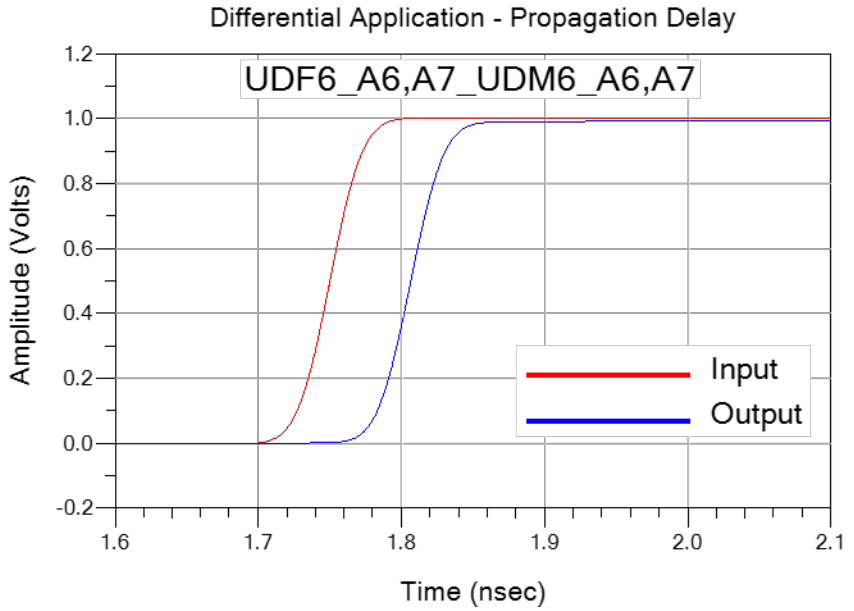

Figure 17

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

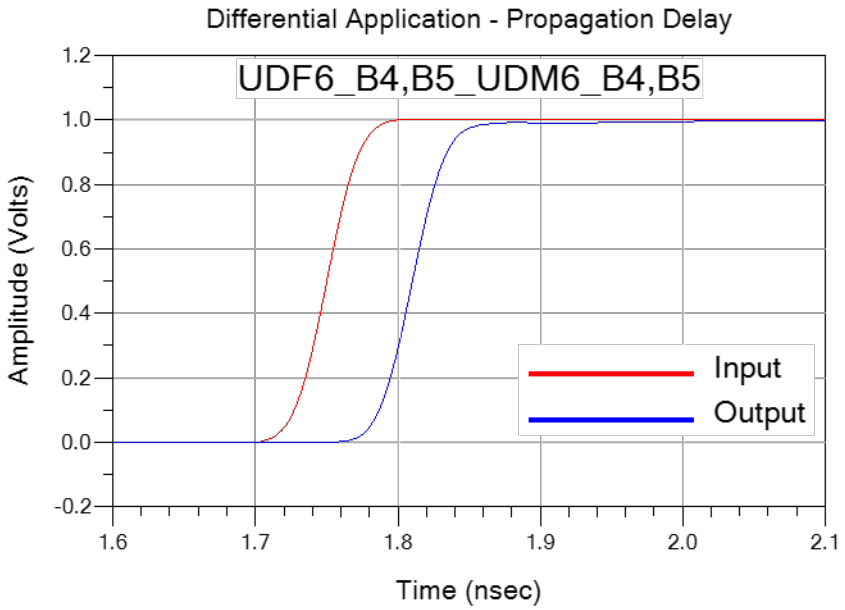

Figure 18

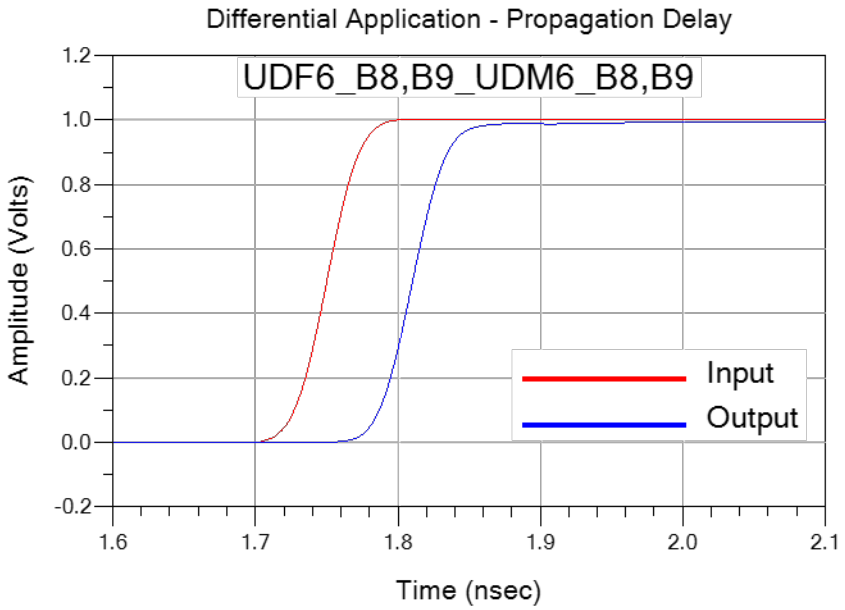

Figure 19

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

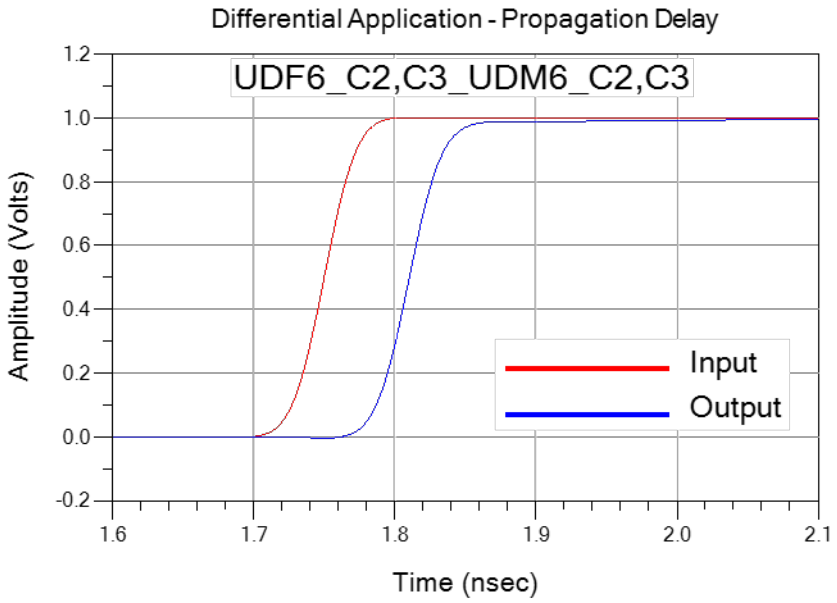

Figure 20

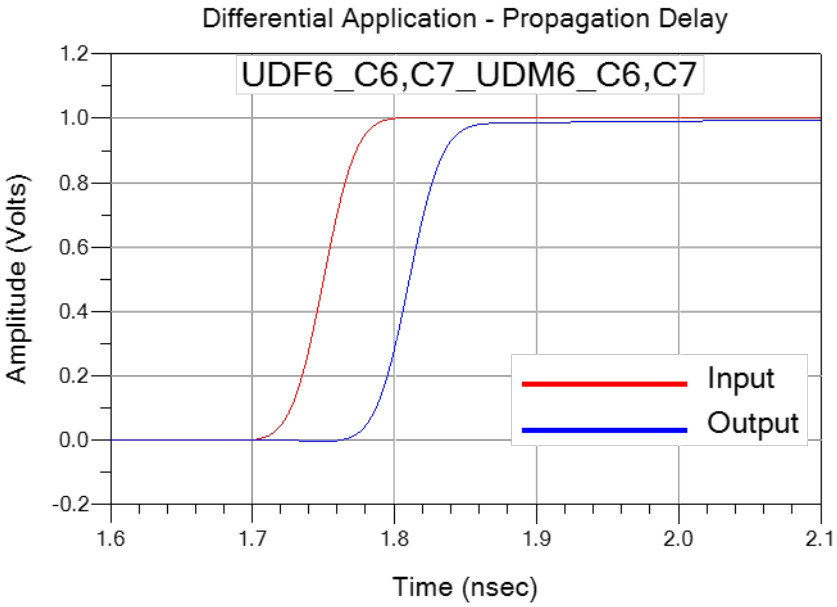

Figure 21

Series: UDM6 / UDF6
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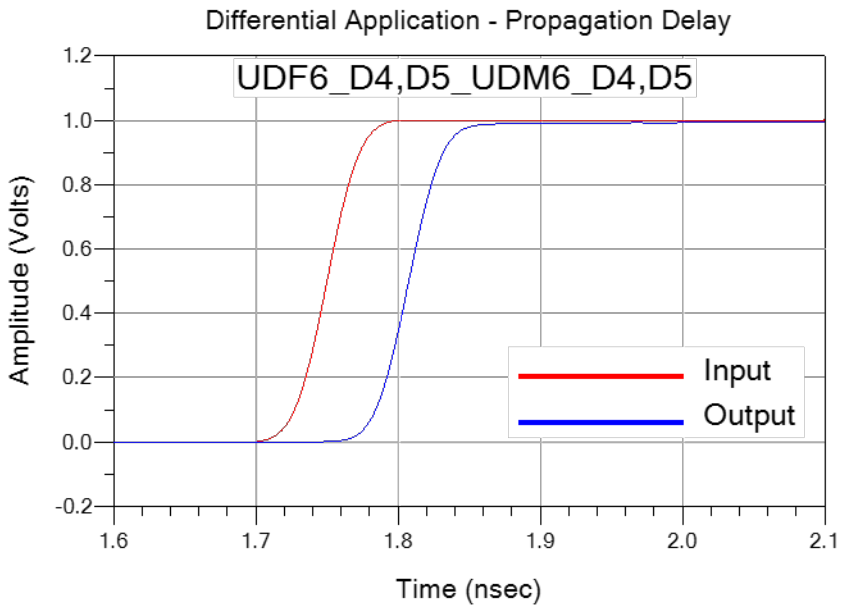

Figure 22

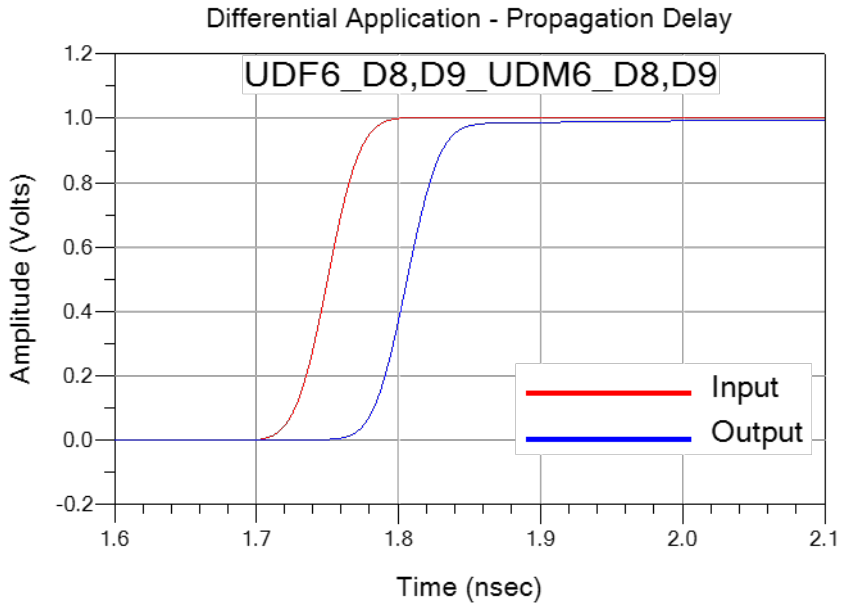

Figure 23

Series: UDM6 / UDF6
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Appendix C – Product and Test System Descriptions

Product Description

Product test samples are High-Density UDx6 Series connectors. The part number is UDM6-10-2-01.5-L-A-TH-TR and UDF6-10-2-03.5-L-A-TH-TR. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of fourteen-layer Tachyon 100G material with 46.25Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount 2.4mm connector is used to interface the PNA test cables to the test fixtures. Optimization of the 2.4mm launch was performed using full wave simulation tools to minimize reflections. The test fixtures and calibration kit are specific to the UDx6 series connector set and identified by part number PCB-UDx6-112776-SIG-0.

PCB-UDx6-112776-SIG-0 Test Fixtures

Shown below is a photograph of test board set.

Figure 24

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PCB Fixtures

The test fixtures used are as follows:

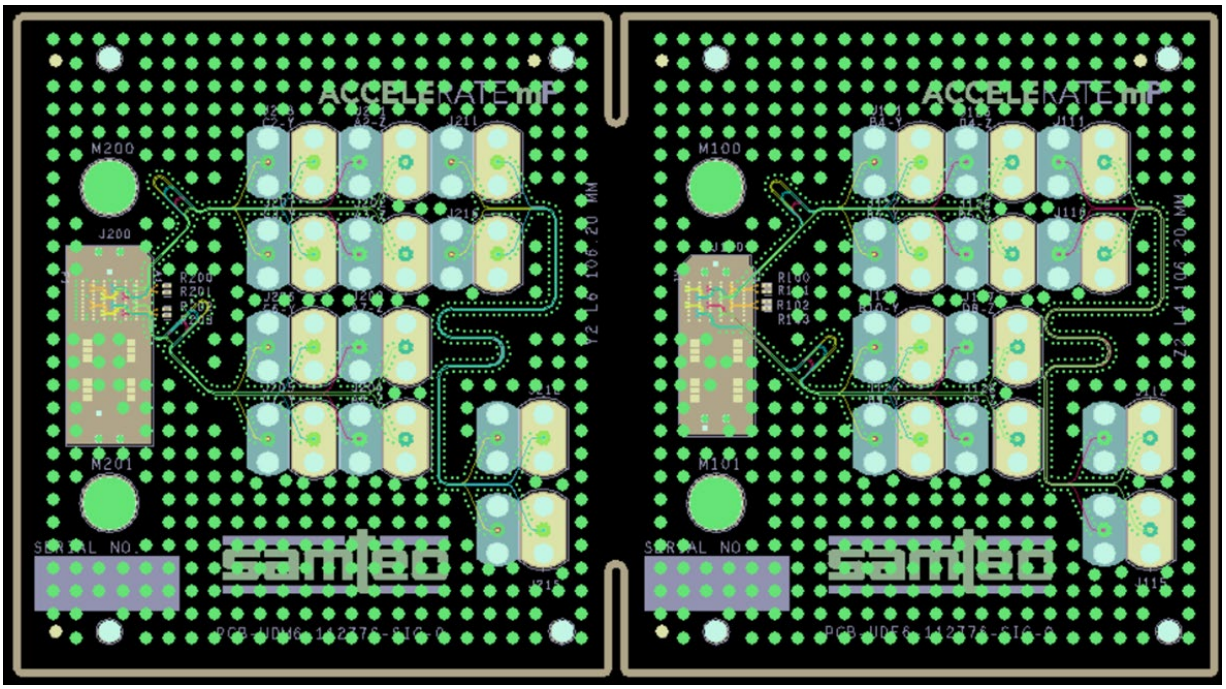

Figure 25

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

All traces on the test boards are length matched to 54.87 mm measured from the center of the pad to the 2.4mm connector. The AFR calibration effectively removes 53.37 mm of test board trace effects. This means that 1.5 mm of test board trace length effects are included in both sides of test boards in the measurement. The S-Parameter measurement includes:

A- The UDx6 Series connector set
B- Test board vias, pads (footprint effects) for the UDM6 connector side.
C- 1.5 mm of 0.147 mm wide stripline trace.
D- Test board vias, pads (footprint effects) for the UDF6 side.
E- 1.5 mm of 0.147 mm wide stripline trace.

The figure below shows the location of the measurement reference plane.

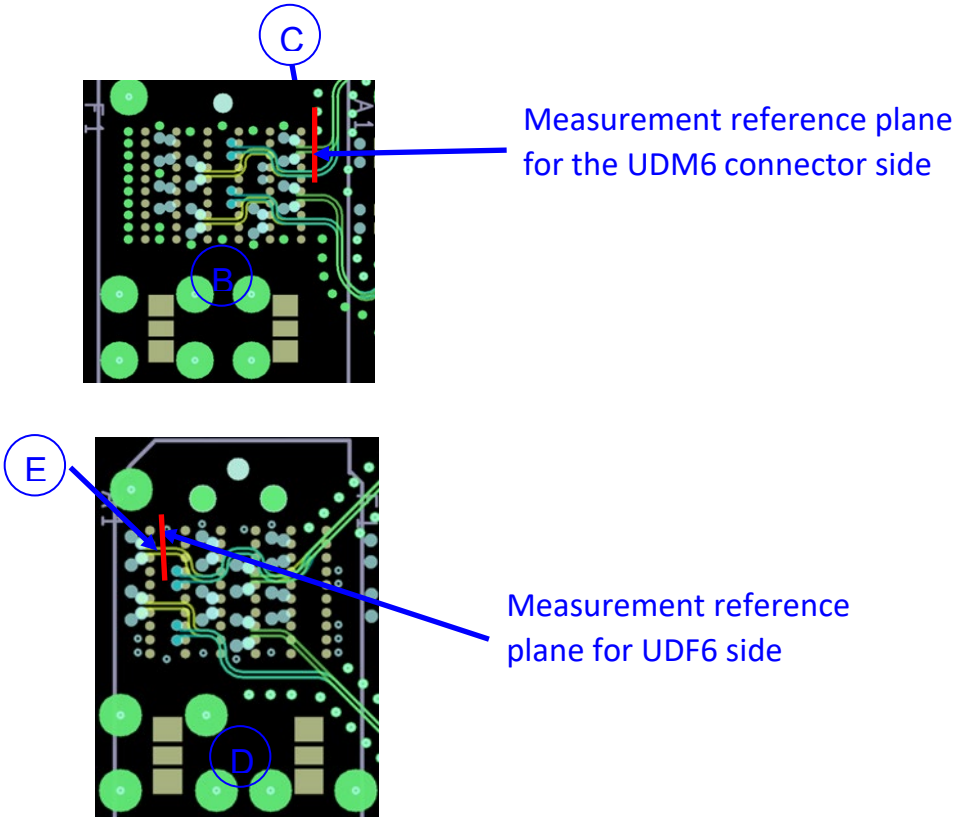

Figure 26

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Keysight N5225B PNA-L network analyzer. Frequency domain data are obtained directly from the instrument and figures are generated by Keysight ADS. The network analyzer is configured as follows:

Start Frequency – 10 MHz
Stop Frequency – 40 GHz
Number of points – 4000
IFBW – 1 KHz

N5225B Measurement Setup

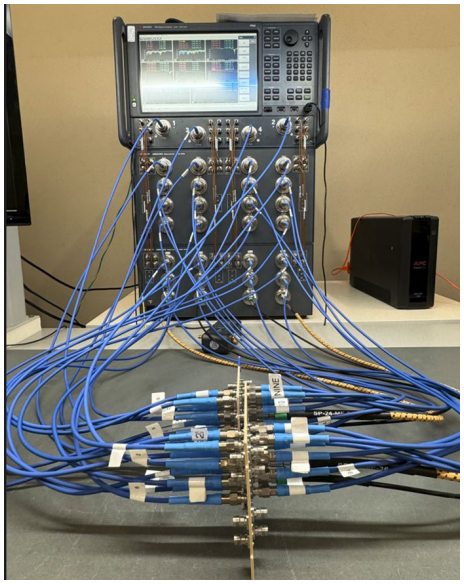

Figure 27

Test Instruments

QTY	Description
1	Keysight N5225B PNA-L Network Analyzer (10 MHz to 40 GHz)
1	Keysight N4694-60003 ECAL Module (10 MHz to 40 GHz)

Test Cables & Adapters

QTY	Description
32	Junkosha 2.4mm male to female cables

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the through calibration standards, the SI test boards, and the selection of the PCB vendor.

A coaxial SOLT calibration is performed using a N4694-60003 ECAL module. Then DUT measurements are performed under SOLT calibration. The measurements include the effect of test fixture. The measurements of the 2X THRU line standards are required to remove the test fixture effect.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with band-width-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2022. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)
A step pulse is applied to the touchstone model of the connector and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Series: UDM6 / UDF6
Description: 0.635 mm Pitch AcceleRate® mP High-Density, High-Speed Power/Signal Interconnect, 5mm Stack Height

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
Z – Impedance (expressed in ohms)