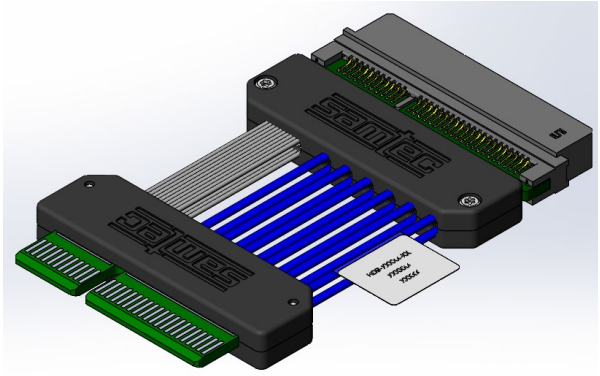
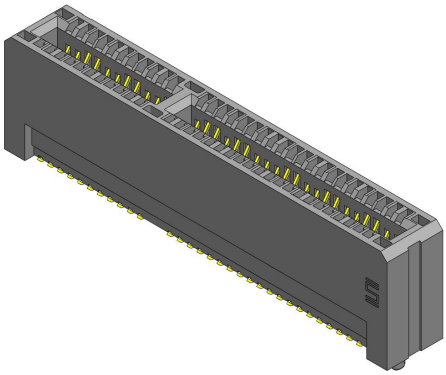
High Speed Characterization Report

PCIEC-G5-XXX-XXXX-M1-85



Mated with:

PCIE-G5-04-01-X-DP-A-XX



Description:

PCI Express® 5.0 Cable Assembly,
Eye Speed® 34 AWG 85-ohm Twinax Cable,
End 2: PCIe Edge Mount Socket

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Cable Assembly Overview

The PCIEC-G5 Cable Assembly is constructed using Samtec 34 AWG, Twinax Cable. The cable is terminated at the first end with an edge card and terminated at the second end with an edge card or an edge mount connector on a printed circuit board. The cable assembly is wired to facilitate Pin 1 to Pin 1 mapping between the cable terminations. The PCIEC-G5 series cable assemblies are available in 36, 64, 98 and 164 positions. The data in this report is only applicable to 250 mm, 500mm and 1000 mm length cable assembly with edge card terminated at first end and edge mount socket terminated at second end.

Each PCIEC-G5 cable assembly was tested by mating it to a PCIE-G5 Socket at first end and Edge Card at second end. One sample of each assembly was tested. The actual part numbers that were tested are shown in Table 1, which also identifies End 1 and End 2 of each assembly. A relative sample picture is shown in Figure 1, and a diagram is shown in Figure 2.

Length	Part Number	End 1	End 2
250 mm	PCIEC-G5-064-0250-M1-85	Edge-Card	Edge-Mount
500 mm	PCIEC-G5-064-0500-M1-85	Edge-Card	Edge-Mount
1000 mm	PCIEC-G5-064-1000-M1-85	Edge-Card	Edge-Mount

Table 1: Sample Description

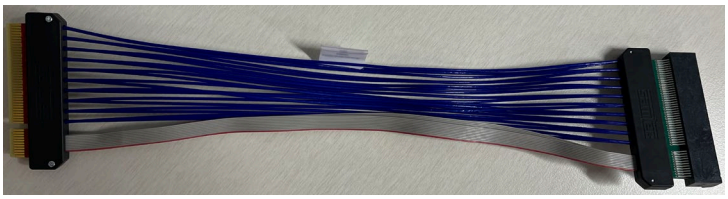

Figure 1: Test Sample

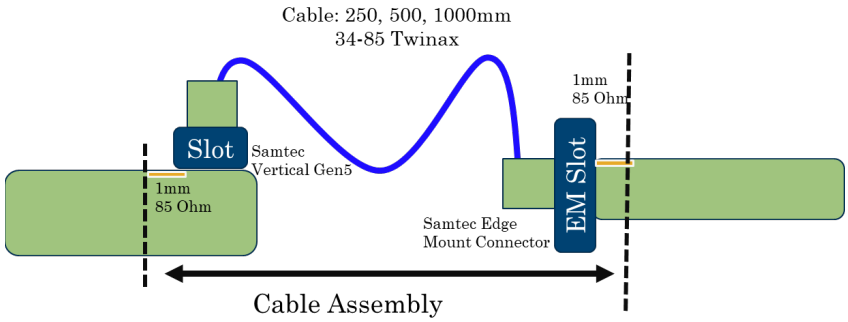

Figure 2: Diagram of the DUT

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Frequency Domain Data Summary

Bandwidth Figures – Differential Insertion Loss

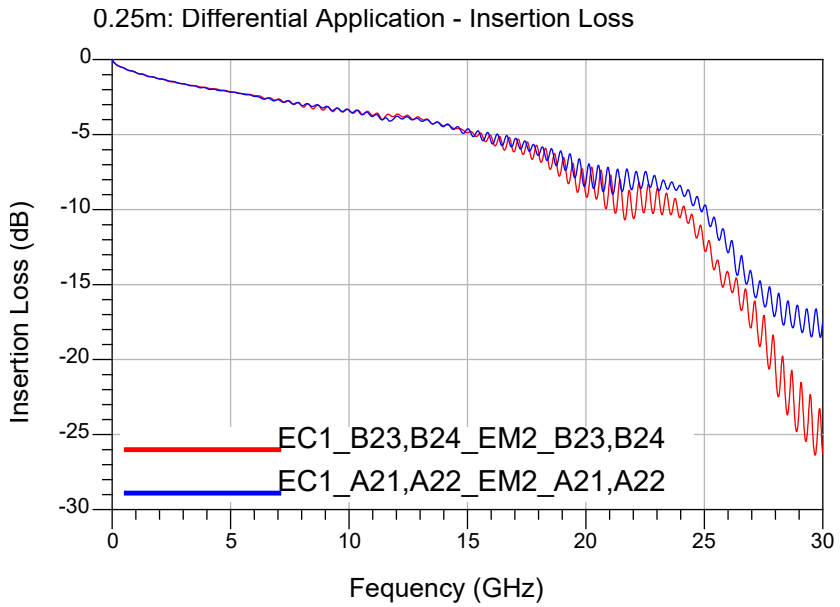

Figure 3

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable,
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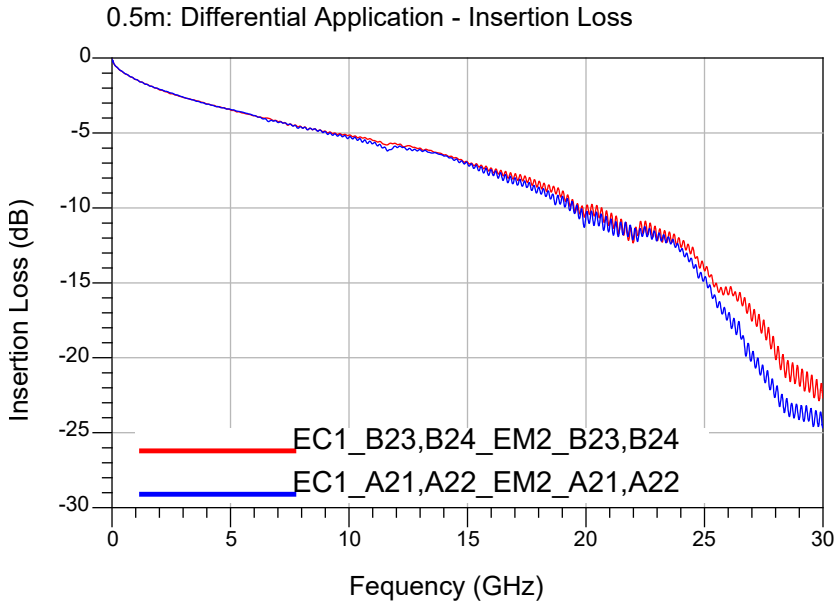

Figure 4

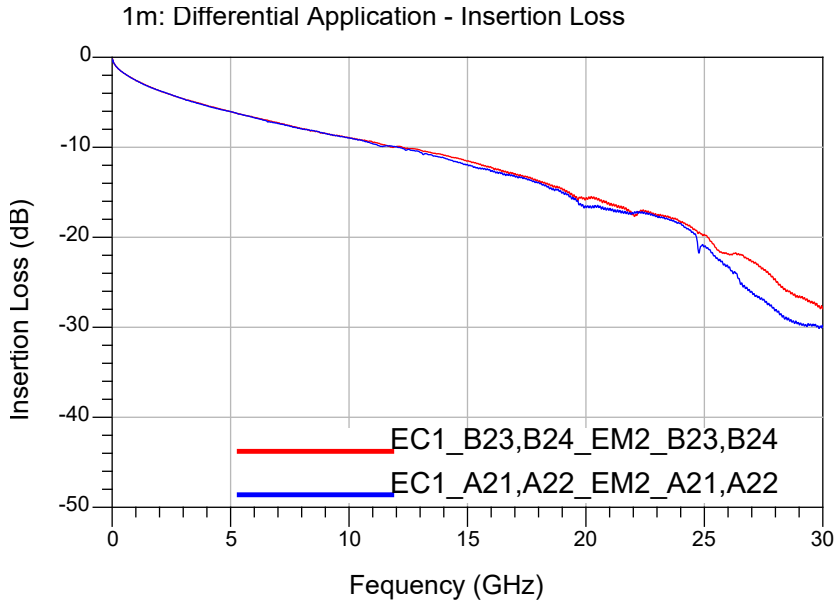

Figure5

Series: PCIEC-G5
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Time Domain Data Summary

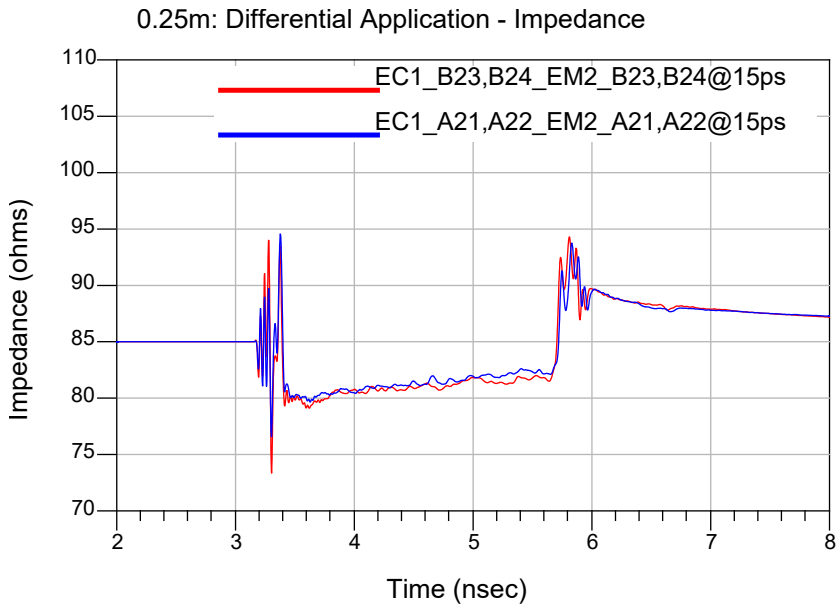

Figure 6

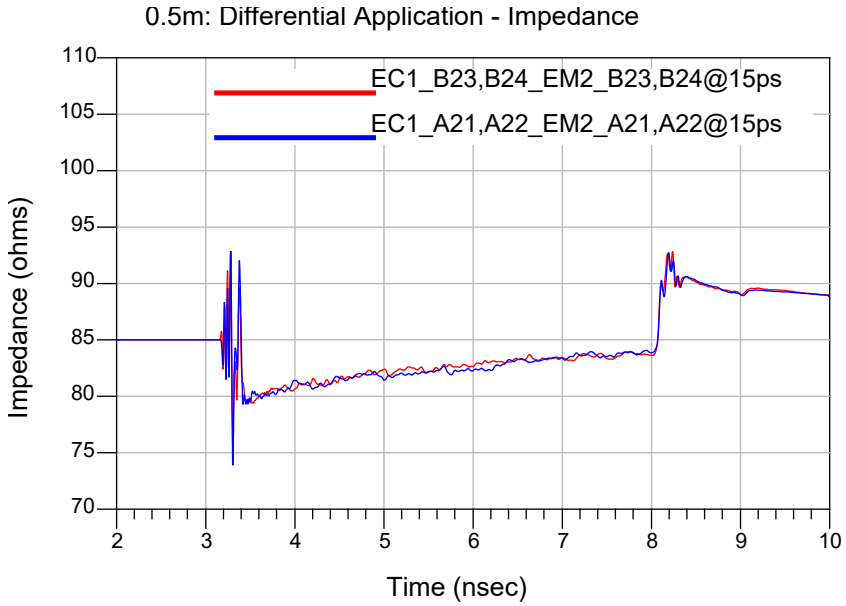

Figure 7

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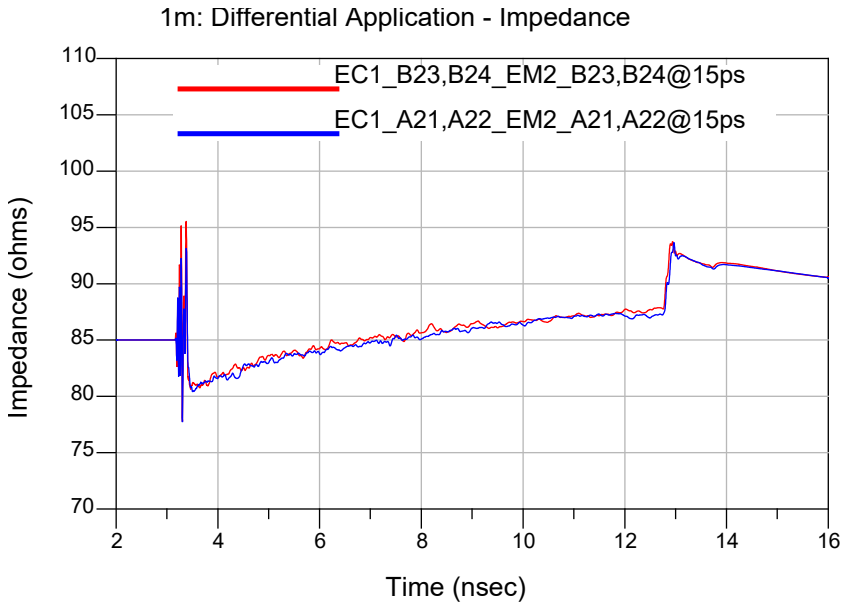

Figure 8

Table 2 - Propagation Delay (Cable Assembly)				
Driver	**Receiver**	**0.25 m**	**0.5 m**	**1 m**
EC1_B23,B24	EM2_B23,B24	1.395 ns	2.587 ns	4.957 ns
EC1_A21,A22	EM2_A21,A22	1.405 ns	2.591 ns	4.968 ns

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Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board-related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GGSSGG" differential drive configuration only.

Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high-speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.
In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals might be encountered as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary

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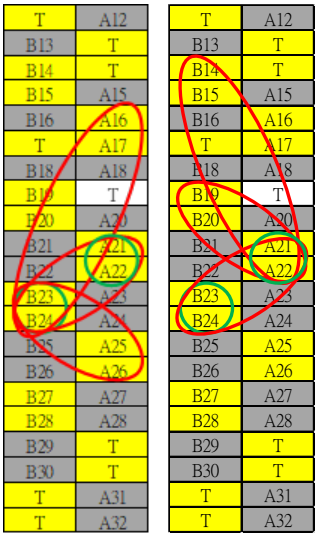
slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

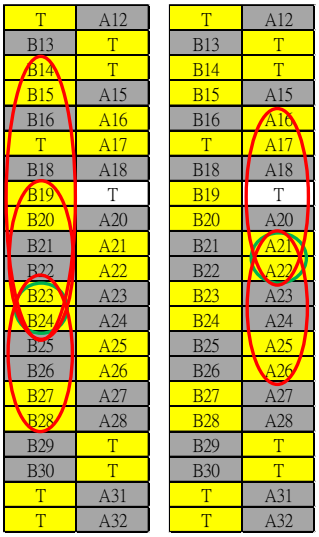
Cable Assembly Pin Map

The PCIEC-G5 cable assembly is pre-defined and following standard PCIe GEN5.0 pinout. For this report, the following configurations are evaluated.

For NEXT



For FEXT



T: Terminators

Differential Impedance (denoted by green circles)

- GGSSGG (Ground-ground-positive signal-negative signal-ground-Ground)

Differential Crosstalk (denoted by red circles)

- In Row: from the terminals to the other terminal on the same row
- Across Row: from one row of terminals to the other row of terminals

See Appendix C – Product and Test System Descriptions for details.

Signal Edge Speed (Rise Time)

In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or the rise time of the exciting signal. For this report, the fastest rise time used was 15 ps. Generally, this should demonstrate the worst-case performance.

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In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between15ps and 50ps.

For this report, measured rise times were at 20%-80% signal levels.

Frequency Domain Data
Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from network analyzer measurements.

Time Domain Data
Time Domain parameters indicate Impedance mismatch versus length, and signal propagation time in a pulsed signal environment.

The measured S-Parameters from the network analyzer are post-processed using Agilent ADS to obtain the time domain response. Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 1 mm of PCB trace on each connector side. Delay is measured at 50 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Additional information concerning test conditions and procedures is in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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Appendix A – Frequency Domain Responses

Differential Application – Insertion Loss

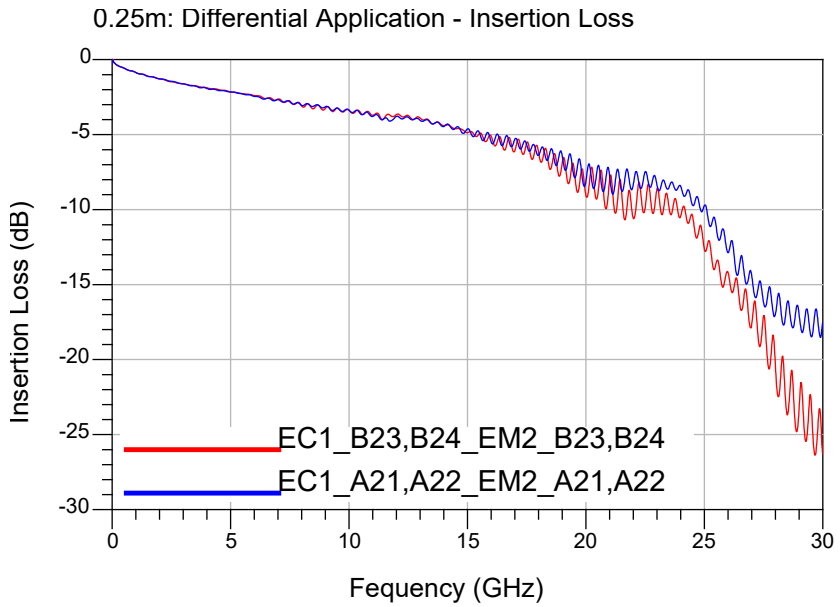

Figure 9

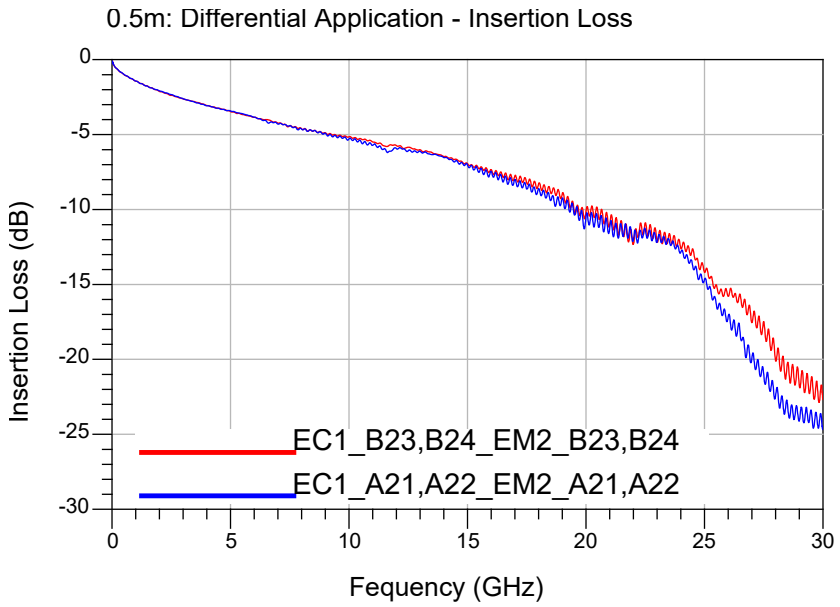

Figure 10

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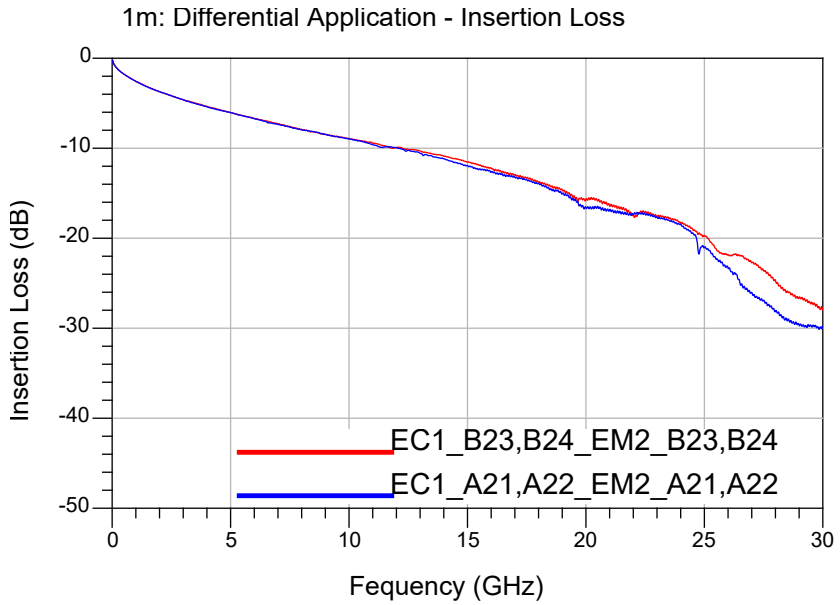

Figure 11

Differential Application – Return Loss

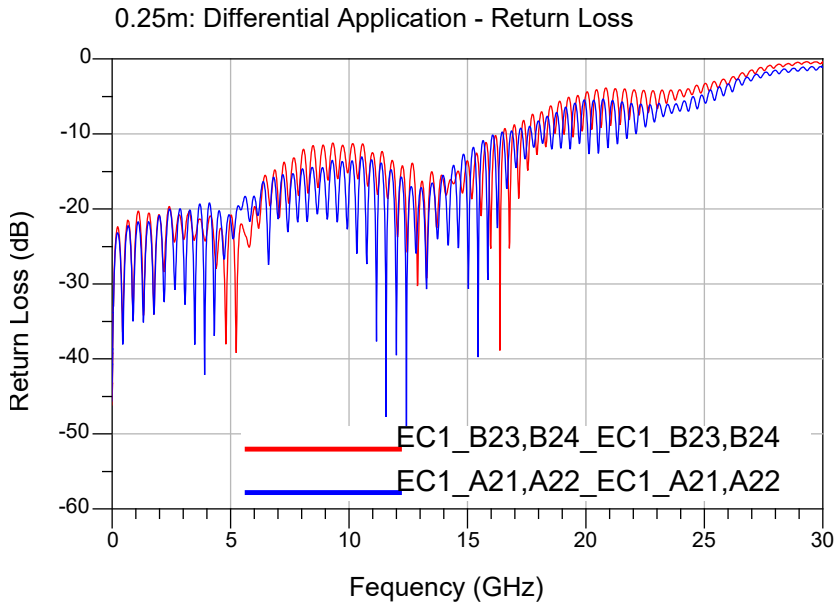

Figure 12

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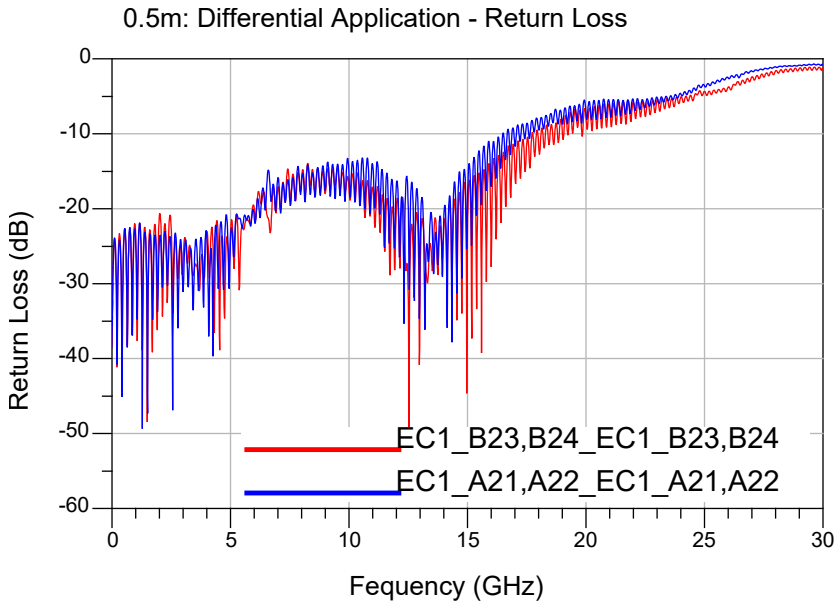

Figure 13

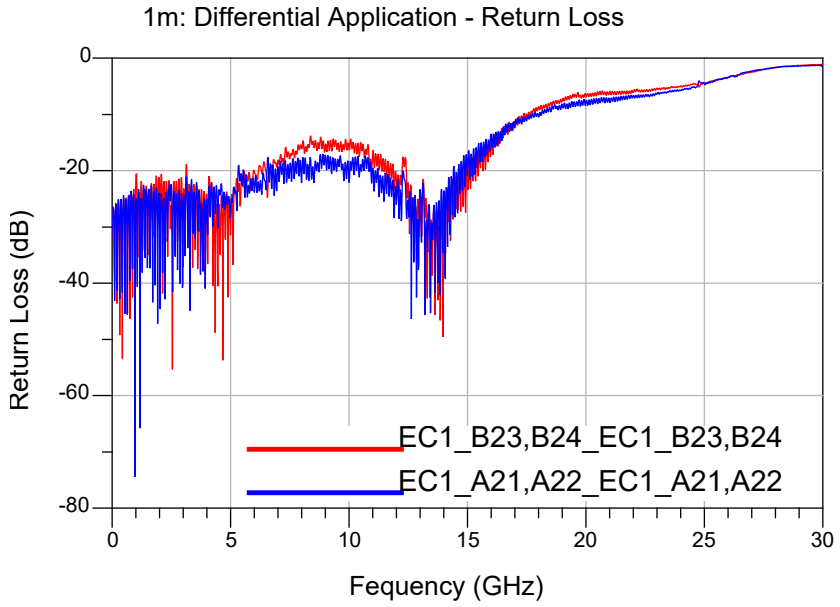

Figure 14

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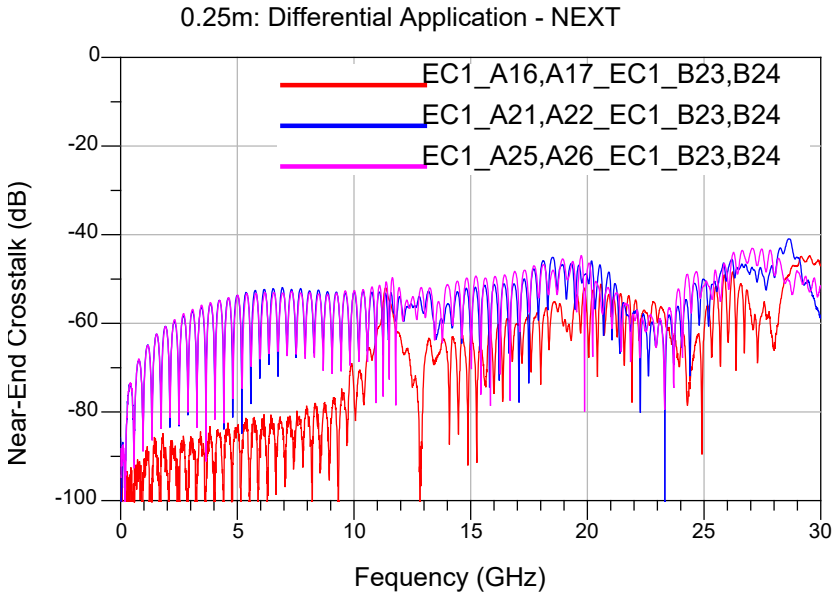
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Differential Application – NEXT Configurations



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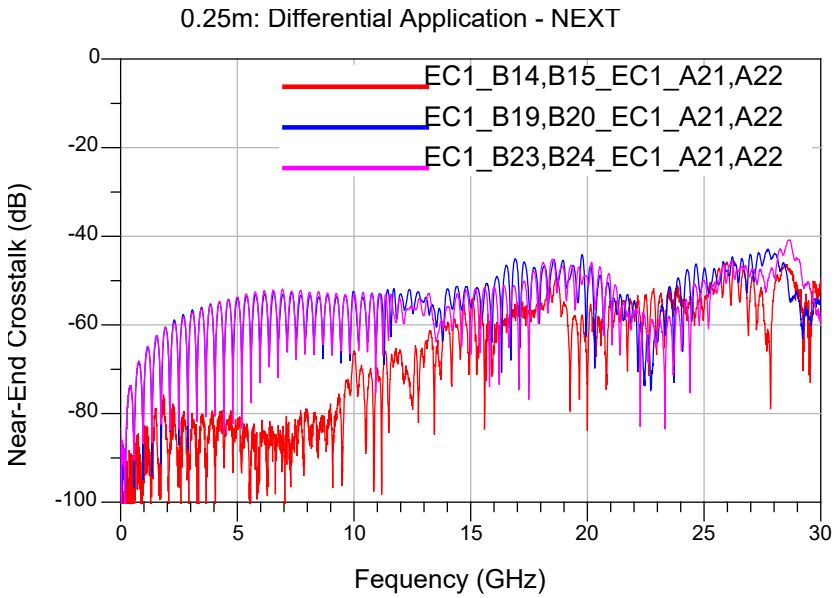


Figure 16

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

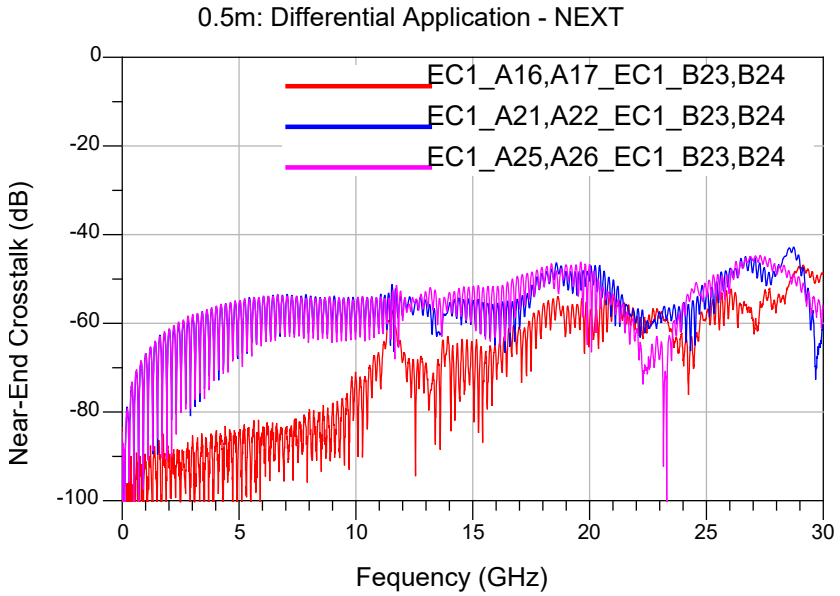


Figure 17

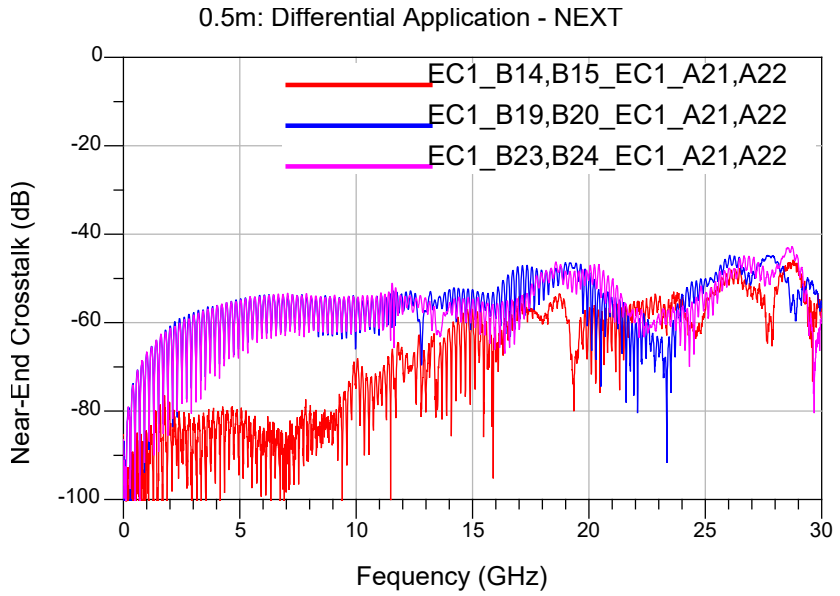
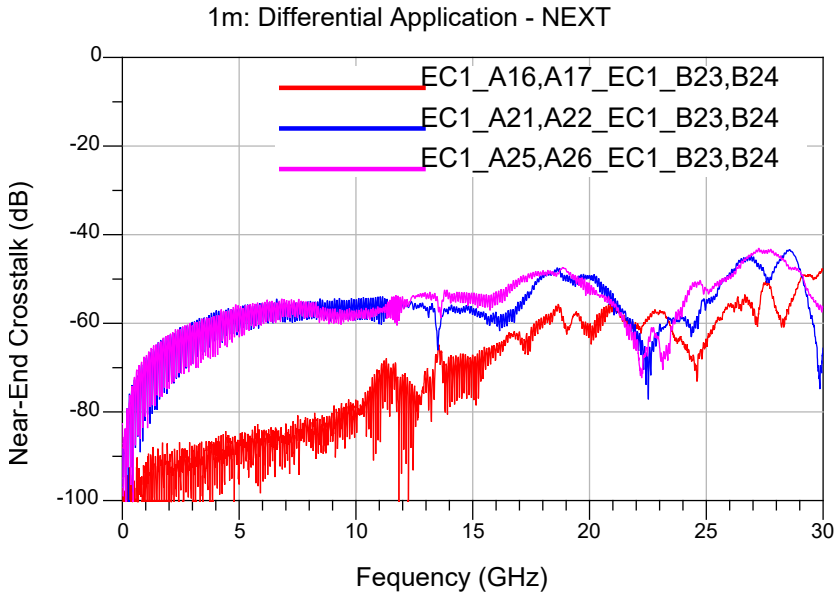


Figure 18

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket



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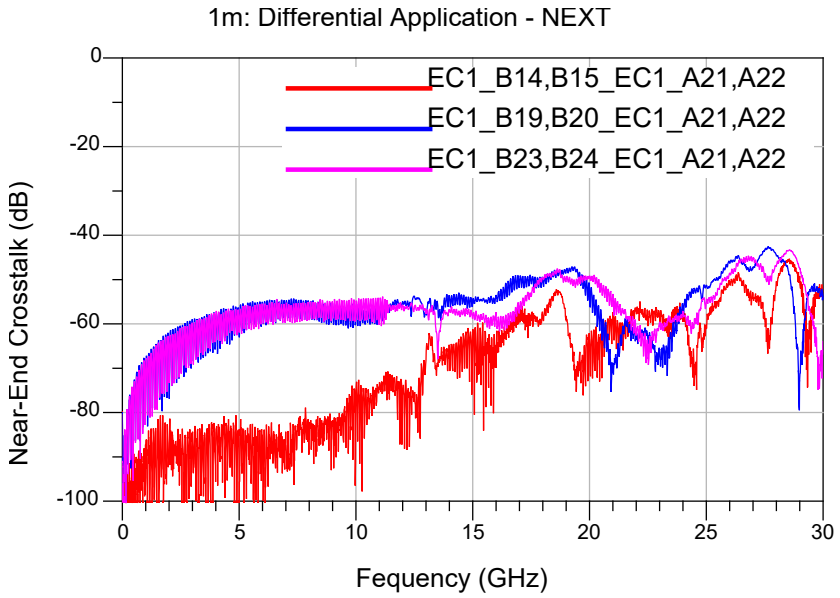
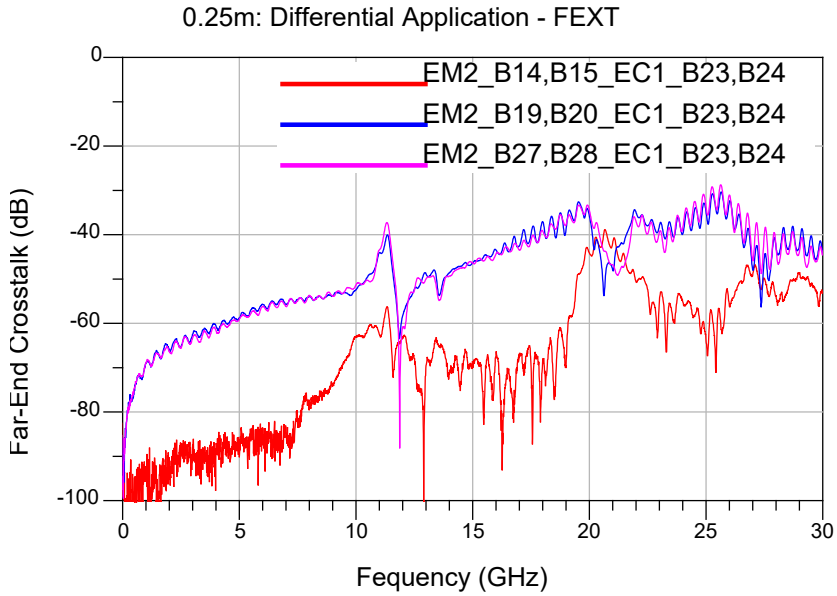


Figure 20

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Differential Application – FEXT Configurations



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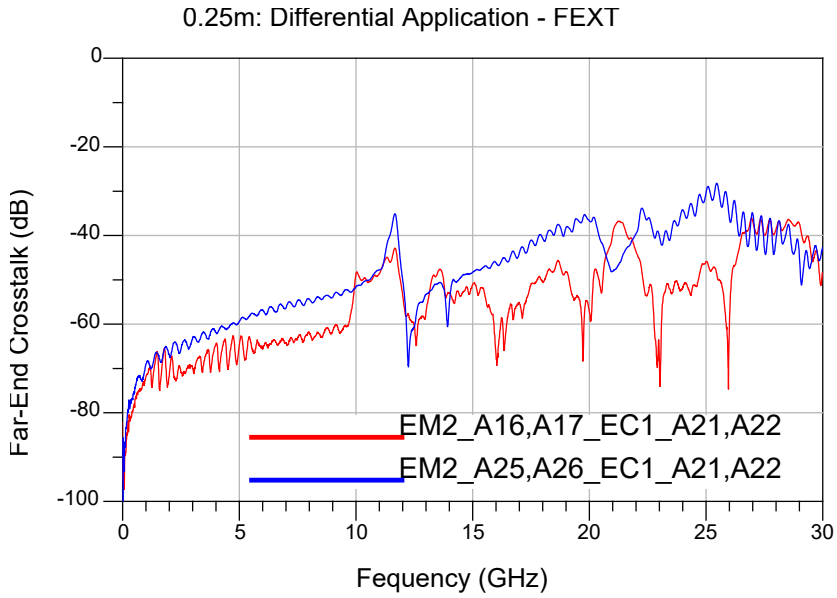
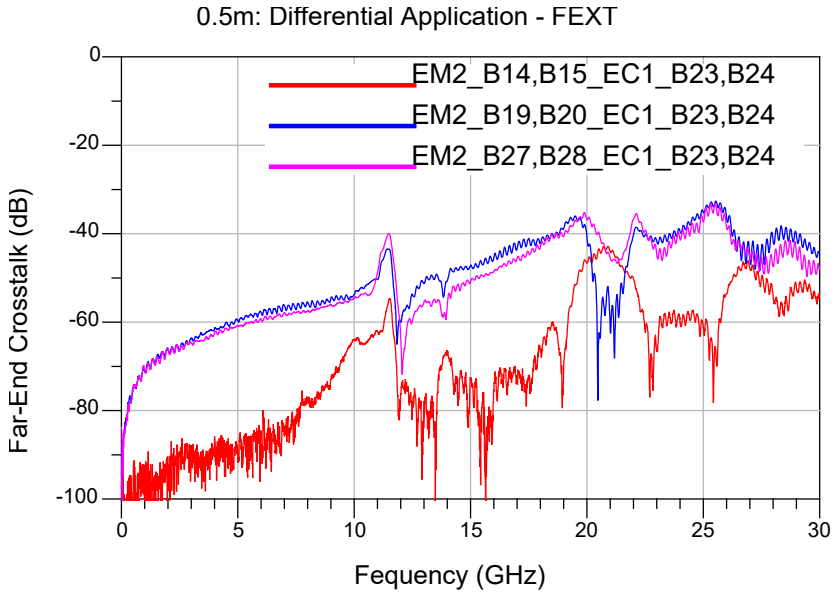


Figure 22

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket



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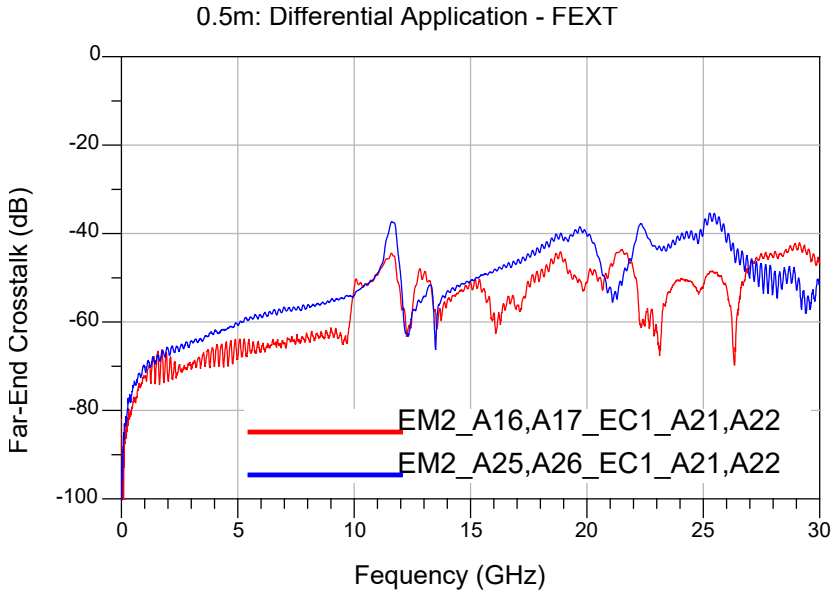

Figure 24

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Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

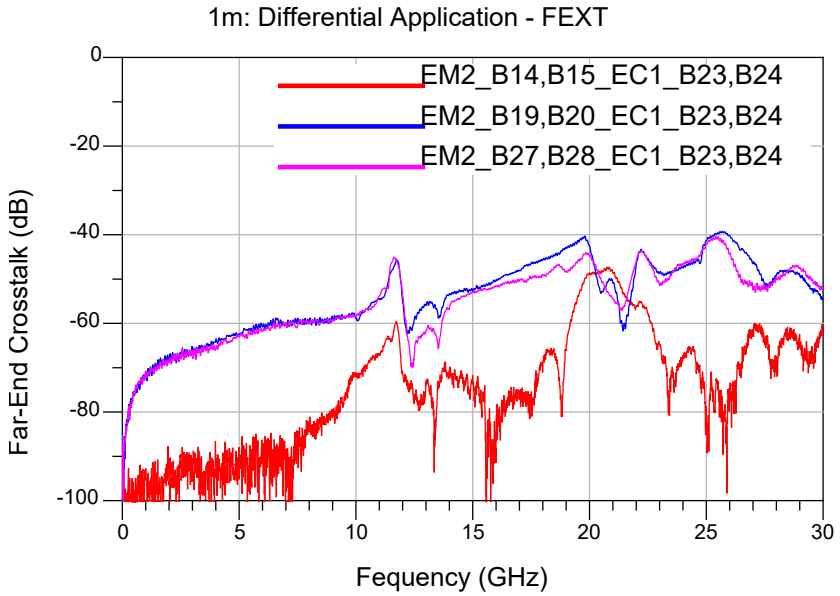

Figure 25

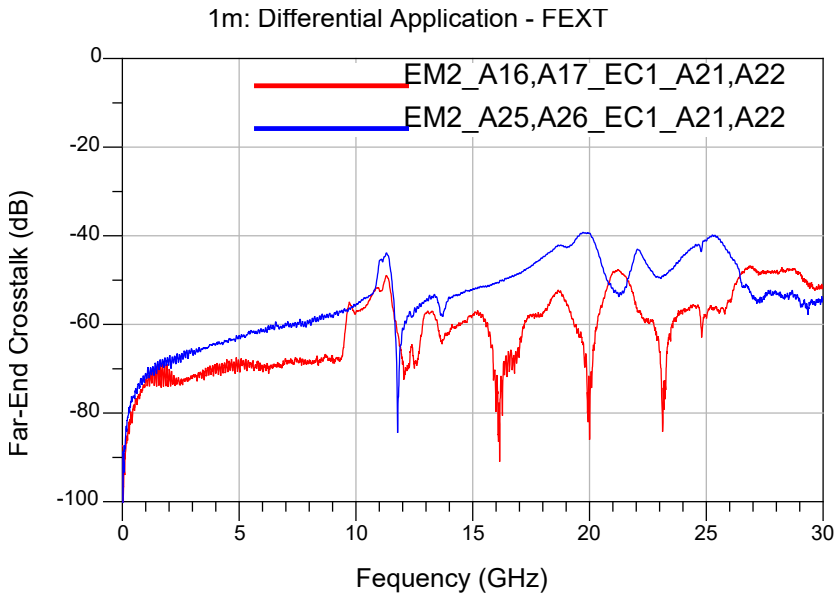

Figure 26

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Differential Application – Differential to Common Mode Conversion

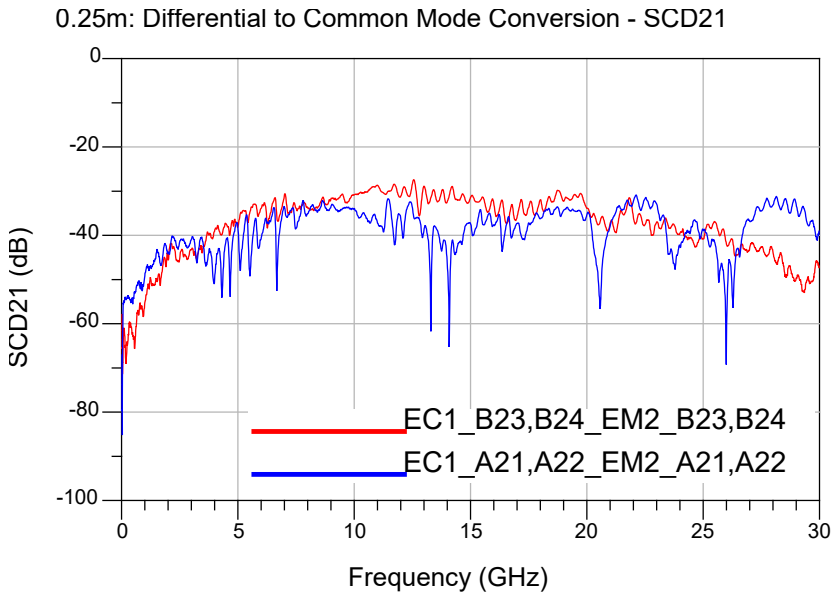

Figure 27

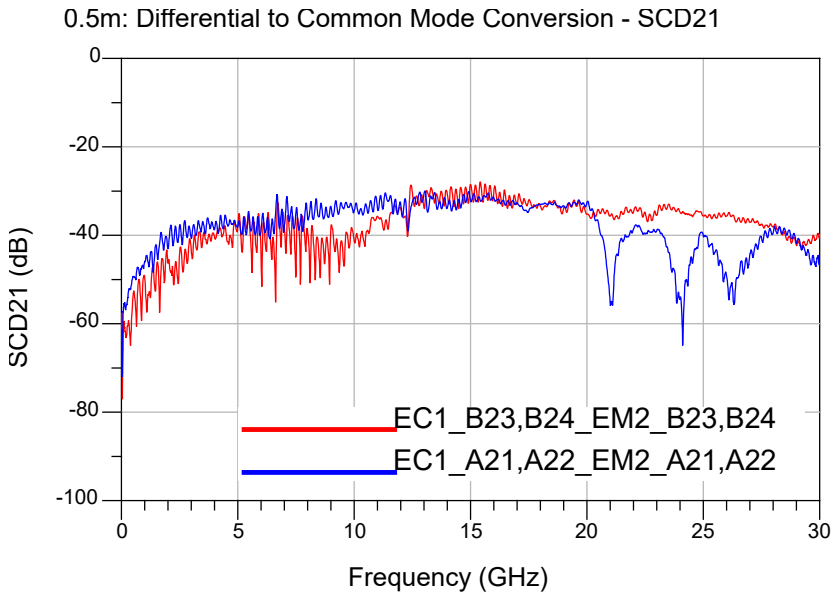

Figure 28

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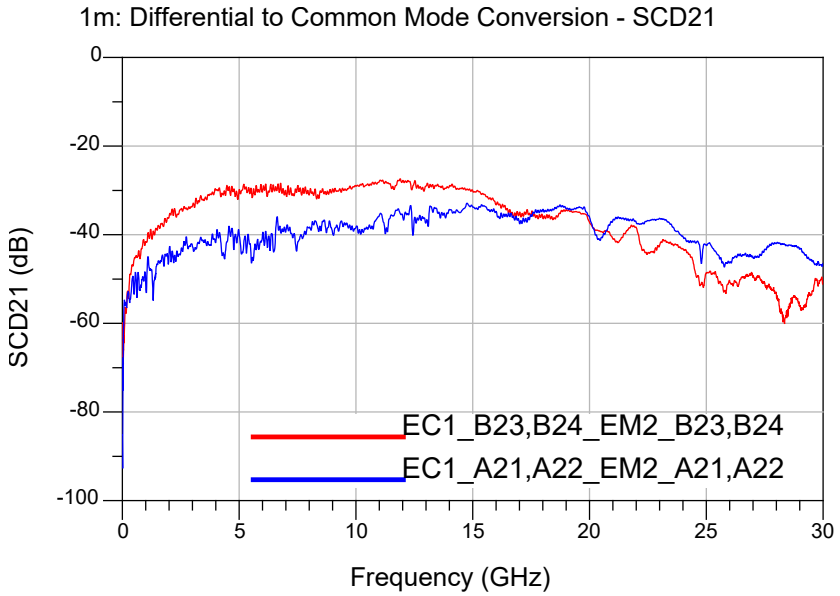

Figure 29

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Appendix B – Time Domain Responses

Differential Application – Input Pulse

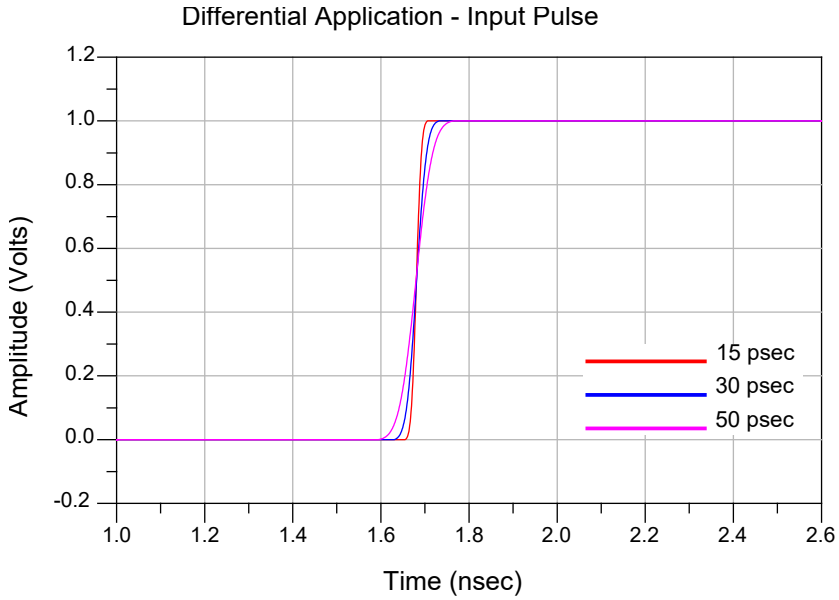

Figure 30

Differential Application – Cable assembly Impedance

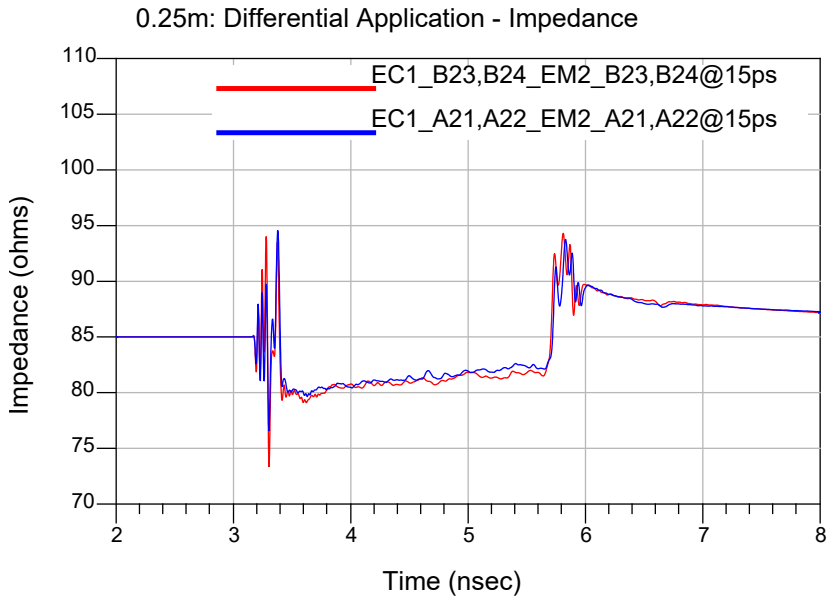

Figure 31

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

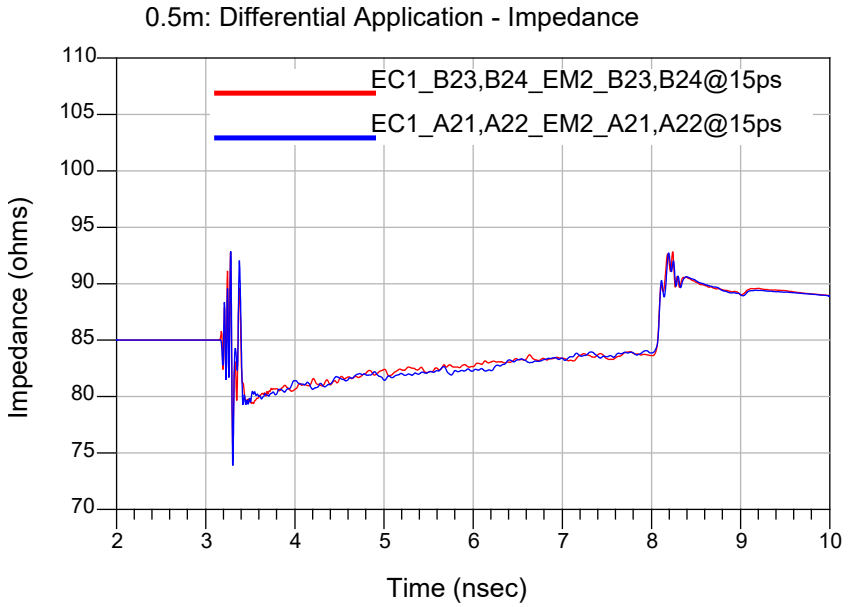

Figure 32

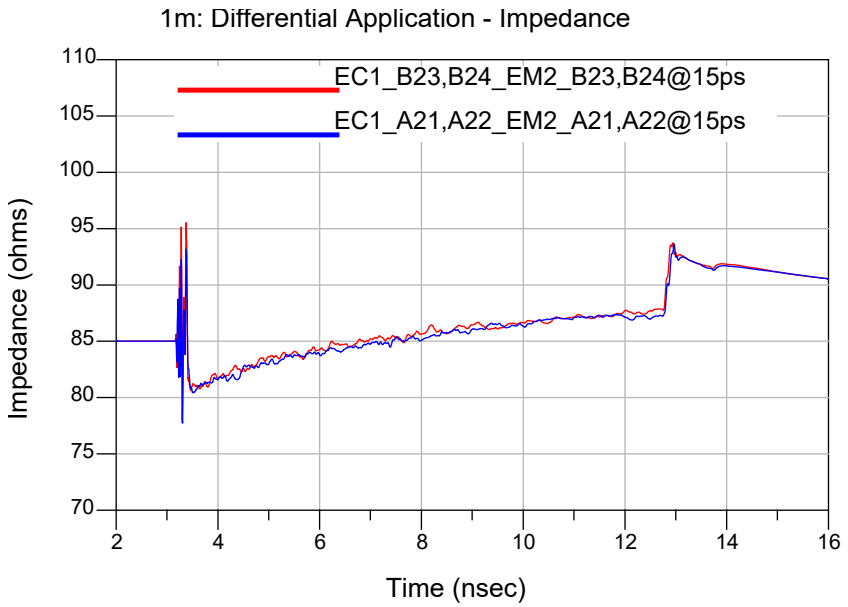

Figure 33

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Differential Application – Cable assembly Impedance

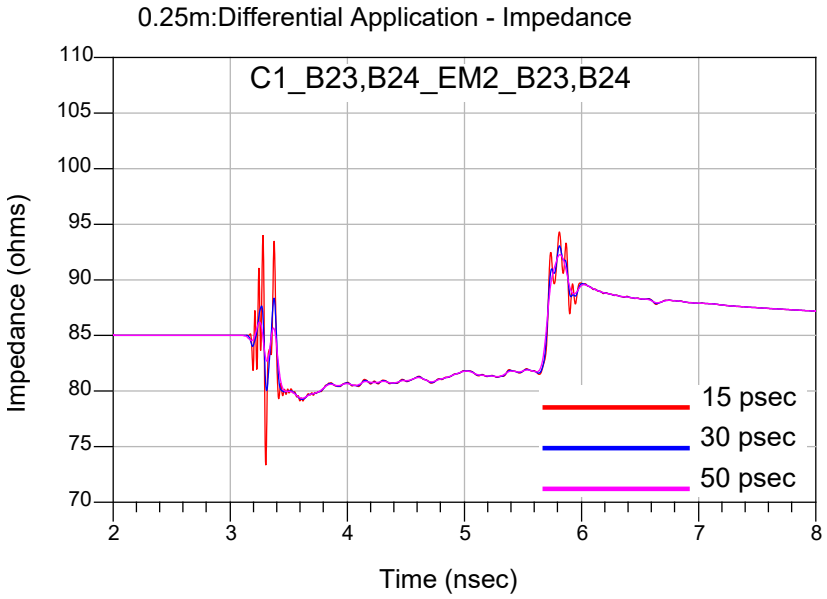

Figure 34

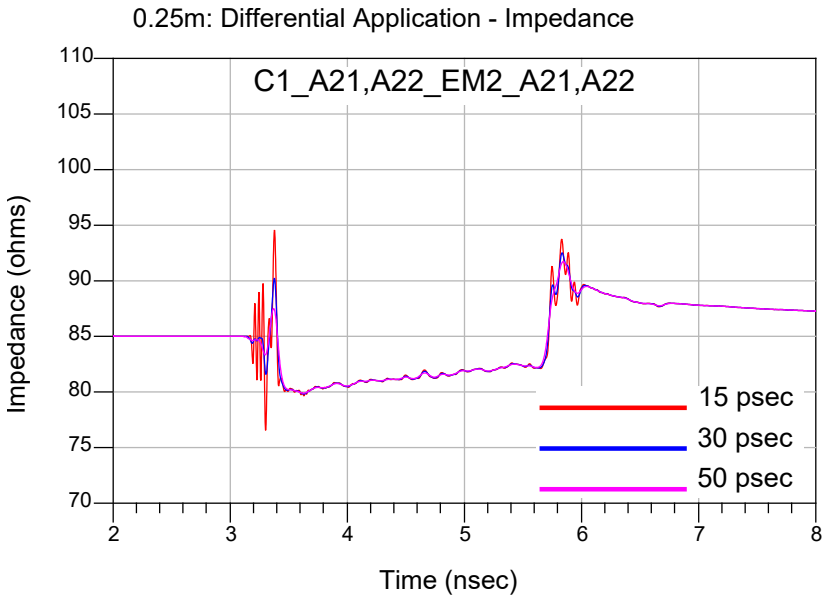

Figure 35

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

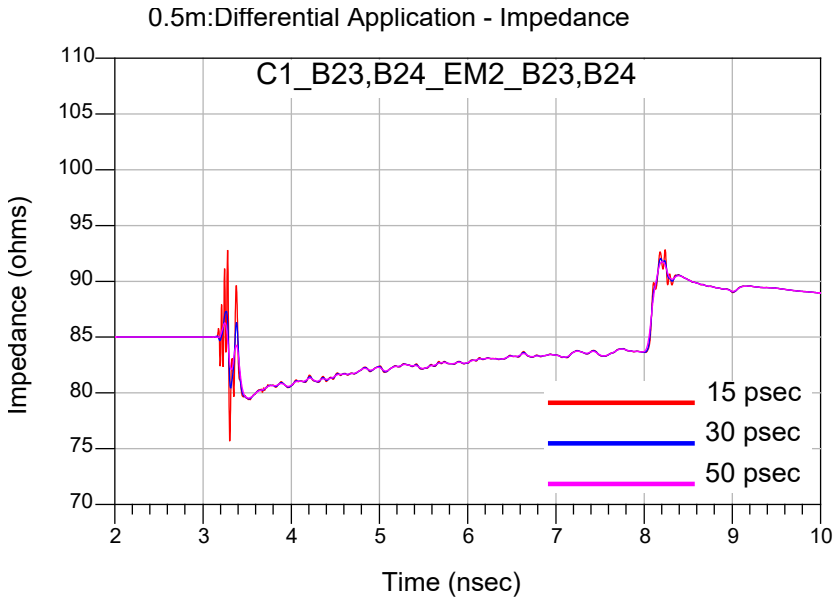

Figure 36

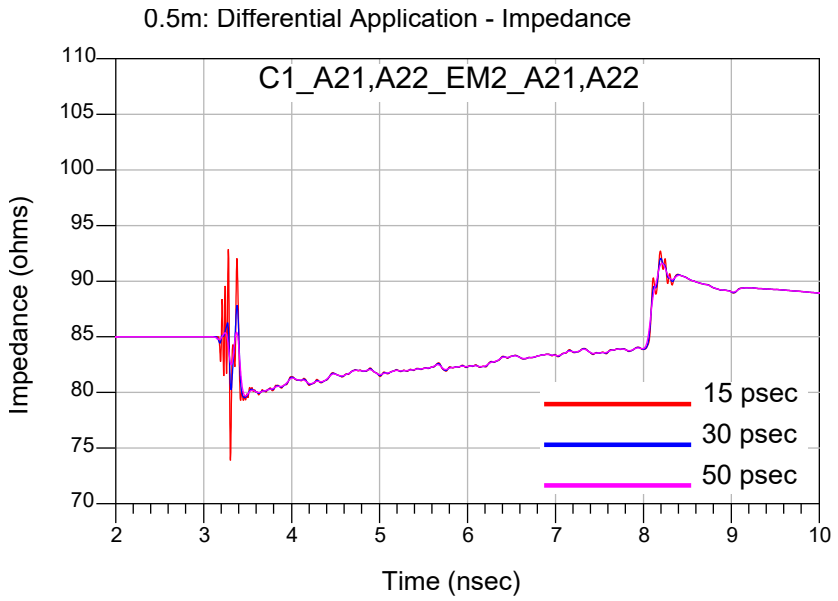

Figure 37

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

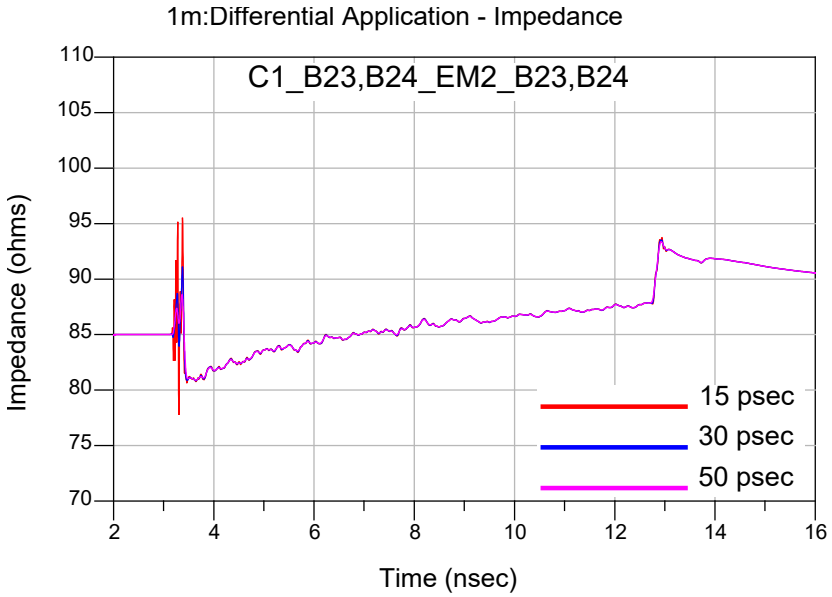

Figure 38

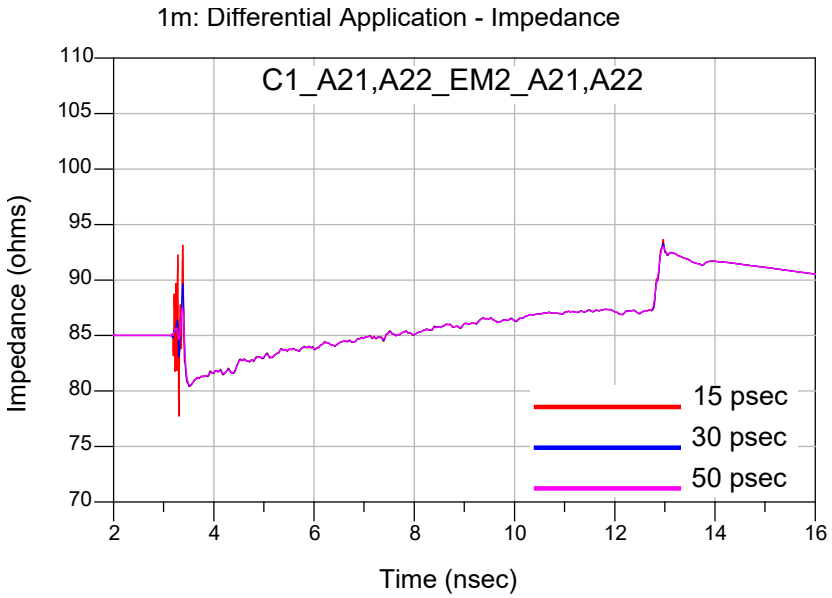

Figure 39

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Differential Application – Propagation Delay

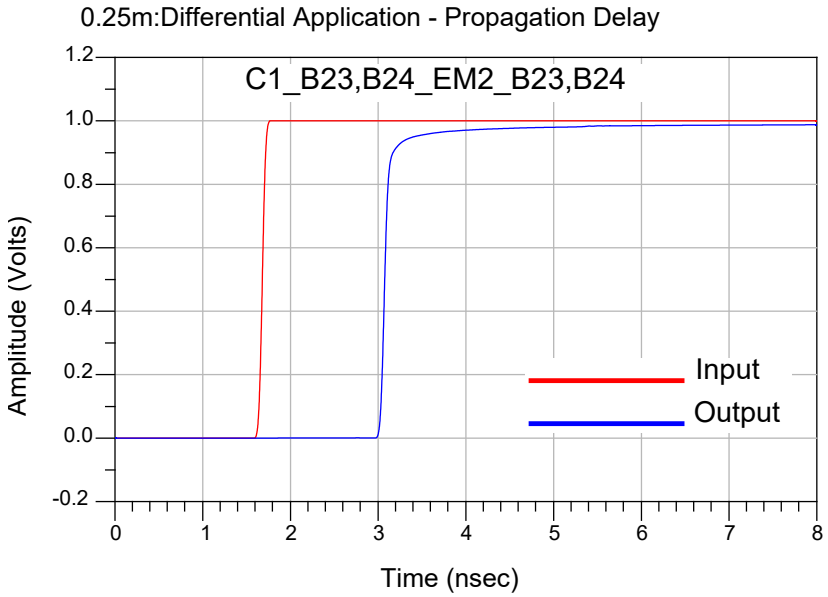

Figure 40

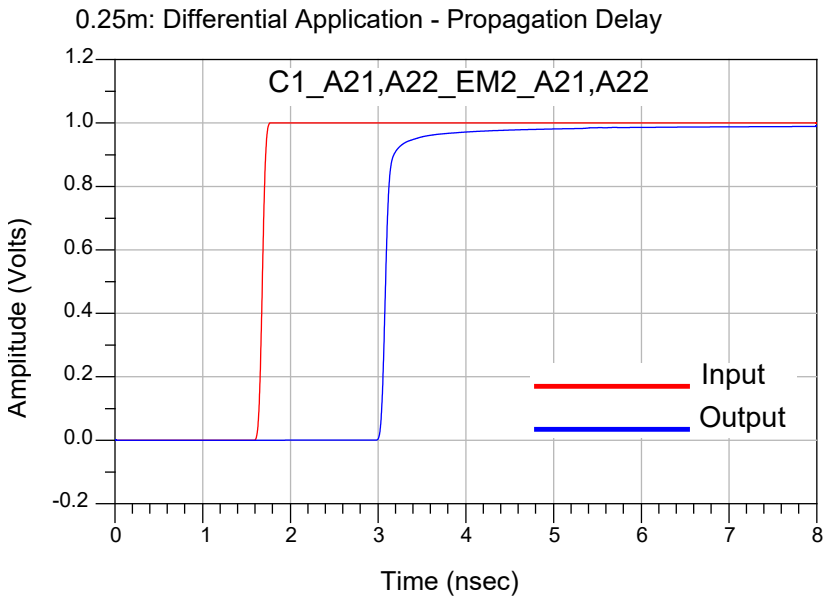

Figure 41

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

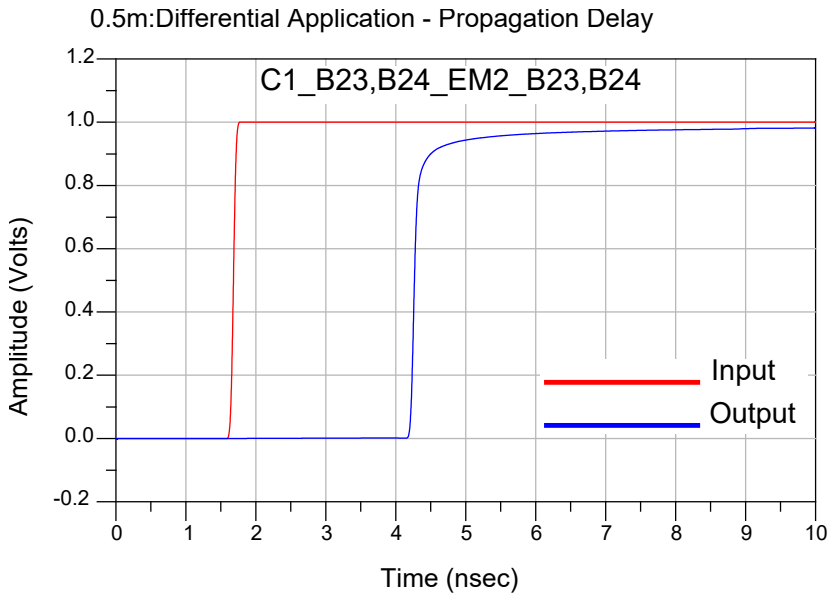

Figure 42

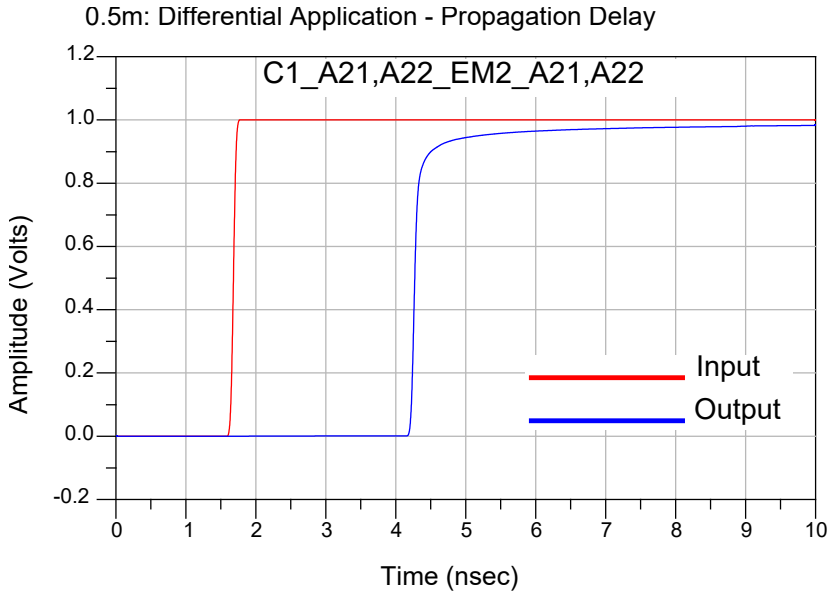

Figure 43

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

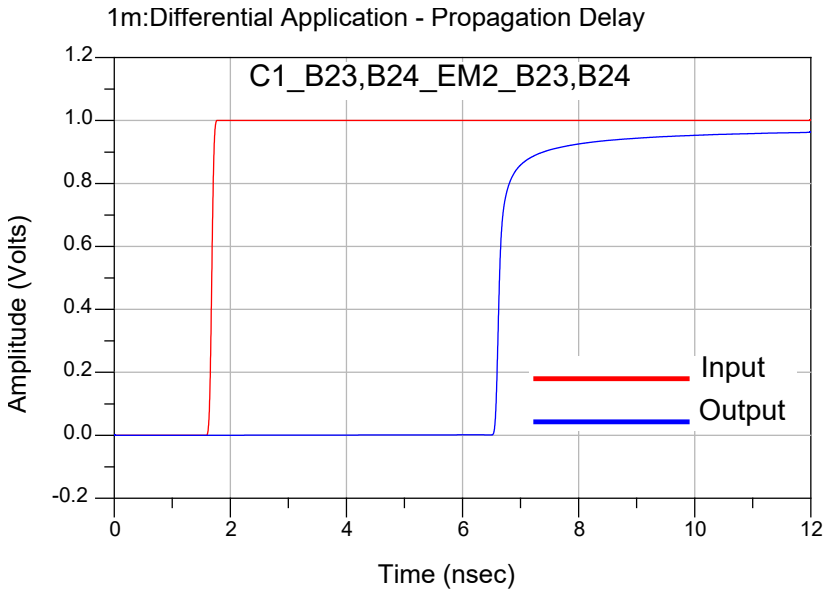

Figure 44

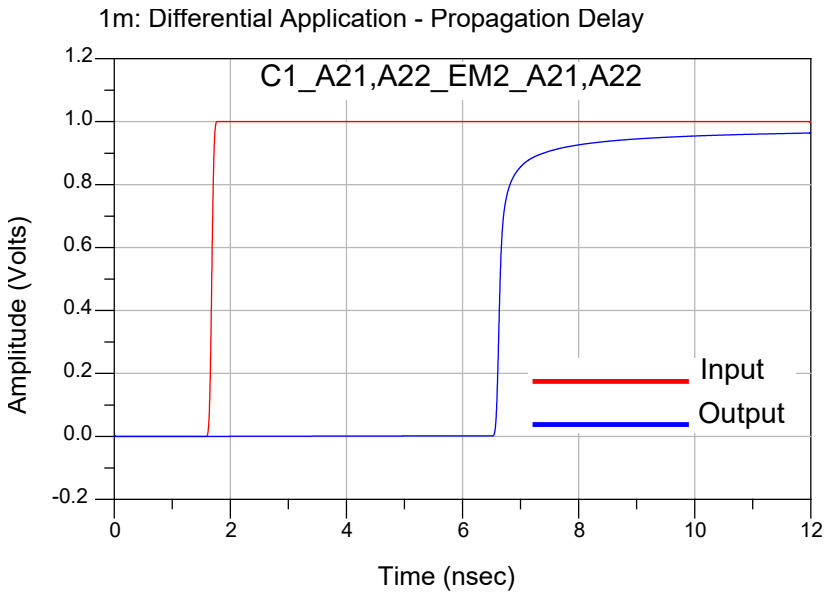

Figure 45

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Appendix C – Product and Test System Descriptions

Product Description

Product test samples are PCI Express® 5.0 Cable Assemblies. The part numbers are PCIEC-G5-064-0250-M1-85, PCIEC-G5-064-0500-M1-85 and PCIEC-G5-064-1000-M1-85. They mate with PCIE-G5-04-01-X-DP-A-XX and Edge Card. A photo of the mated test article mounted to SI test boards is shown below.

The cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in Table 3. There is a total of 32 positions per row, but all are not shown. Positions 1 – 11 terminate to the PVC power cable. All Side B pairs are Transmitter pairs. All Side A pairs are Receiver pairs except for pair A13-A14, which is the Reference Clock Pair.

Side A	G	13	14	G	16	17	G	19	G	21	22	G	G	25	26	G	G	**29**	**30**	G	32
Side B	12	G	14	15	G	17	G	19	20	G	G	**23**	**24**	G	G	27	28	G	30	31	G

Table 3: Signal line numbers

Test System Description

The test fixtures are composed of six-layer MEGTRON6 material with 42.5Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount 2.4mm connector is used to interface the PNA test cables to the test fixtures. Optimization of the 2.4mm launch was performed using full wave simulation tools to minimize reflections. The test fixtures and calibration kit are specific to the PCIE-G5 series connector set and the edge card, identified by part number PCB-PCIG5F-112180-SIG-0 and PCB-PCIG5M-112180-SIG-0.

PCB-PCIG5F-112180-SIG-0 and PCB-PCIG5M-112180-SIG-0 Test Fixtures

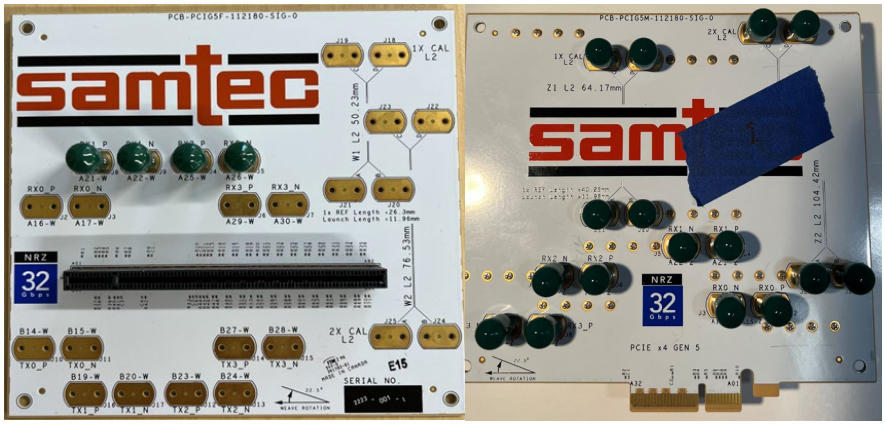

Figure 46

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Artwork of the PCB design is shown below.

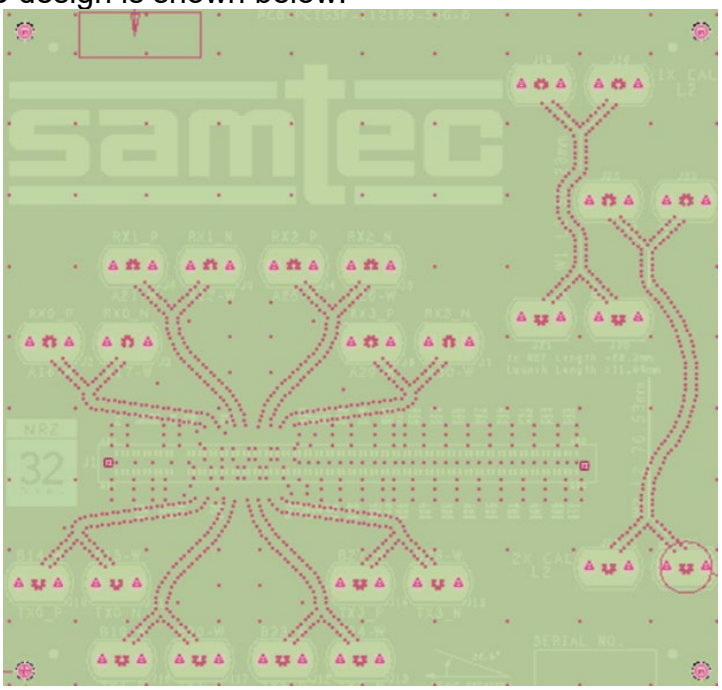

Figure 47

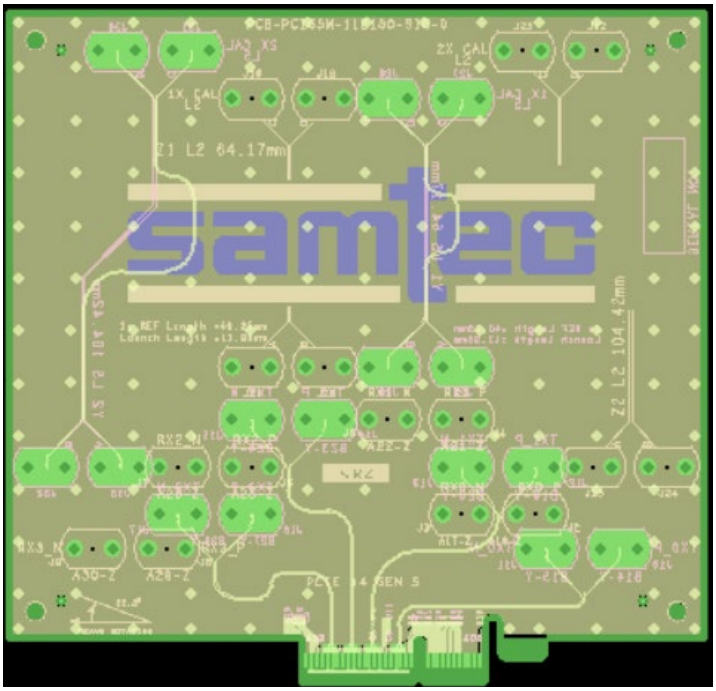

Figure 48

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is Keysight N5225B PNA-L network analyzer. Frequency domain data and figures are extracted from the instrument by AFR application. Post-processed time domain data and figures are generated using convolution algorithms within Keysight ADS. The network analyzer is configured as follows:

Start Frequency – 10 MHz
Stop Frequency – 40 GHz
IFBW – 1 KHz

N5225B Measurement Setup

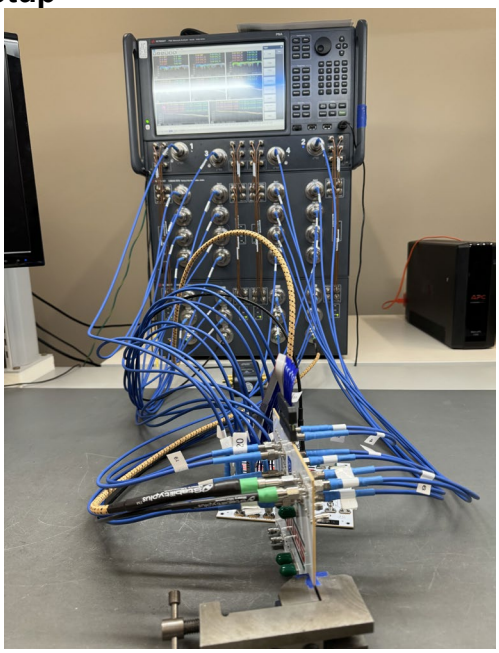

Figure 49

Test Instruments

QTY	Description
1	Keysight N5225B PNA-L Network Analyzer (10 MHz to 67 GHz)
1	Keysight N4694-60003 ECAL Module (10 MHz to 67 GHz)

Test Cables & Adapters

QTY	Description
28	1m Junkosha 2.4mm male to female cables

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards and the selection of the PCB vendor.

A coaxial SOLT calibration is performed using a N4694-60003 ECAL module. Then DUT measurements are performed under SOLT calibration. The measurements include the effect of test fixture. The measurements of the 2X THRU line standards are required to remove the test fixture effect.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2022. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly, and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same figure. The difference in time, measured at the 50% point of the step voltage, is the propagation delay.

Series: PCIEC-G5
Description: PCI Express® 5.0 Cable Assembly, Eye Speed® 34AWG 85-ohm Twinax Cable, End 2: PCIe Edge Mount Socket

Impedance (TDR)

Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g., 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform are limited.

Appendix F – Glossary of Terms

ADS – Keysight Advanced Design System
AFR – Automatic Fixture Removal
PCB – Printed Circuit Board
SUT – System Under Test
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission