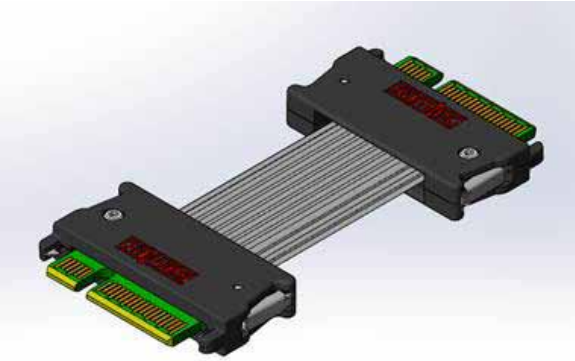
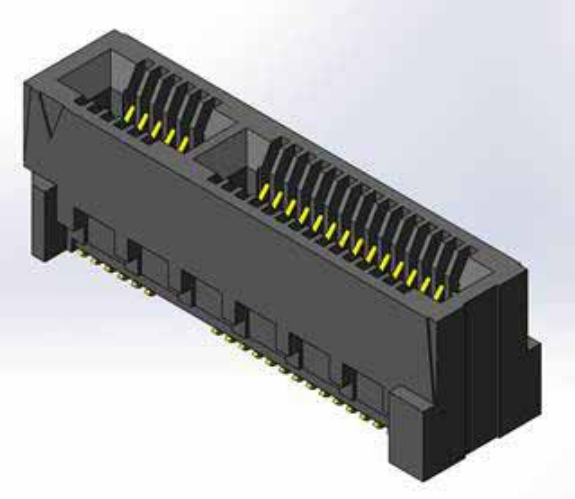
High Speed Characterization Report

ECDP-16-XX-L1-L2-2-1



Mated with:
HSEC8-125-XX-XX-DV-X-XX



Description:

High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly, 30 AWG ACCELERATE™ Twinax Cable

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 2/28/2014

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

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Cable Assembly Overview

The 0.80 mm (.0315") ECDP Cable Assembly is constructed using Samtec 30 AWG, 100 Ω, AcceleRate™ twinax cable. The cable is terminated at each end with a 4 layer double vertical PCB edge card connector. Each edge card are double row structures with up to 16 signal pairs. The ECDP-16-XX-L1-L2-2-1 assembly is wired to facilitate a Pin 1 to Pin 2 mapping between the cable ends. The data in this report is applicable to 9.80 and 39.37 inch cable assemblies.

Each ECDP assembly was tested by mating it to a HSEC8-125-01-L-DV-L1 2 Row 0.8mm High Speed Edge Card Assembly at each end. One sample of each assembly was tested. The actual part numbers that were tested are shown in Table 1, which also identifies End 1 and End 2 of each assembly. A relative sample picture is shown in Figure1. Two differential pairs, a Long Path and a Short Path, of each assembly type were tested. Both End 1 and End 2 of ECDP-16-XX-L1-L2-2-1 have a green transition PCB.

Length	Part Number	End 1	End 2
9.80 inches	ECDP-16-09.80-L1-L2-2-1	HSEC8	HSEC8
39.37 inches	ECDP-16-39.37-L1-L2-2-1	HSEC8	HSEC8

Table 1: Sample Description

Figure 1: Test Sample

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Cable Assembly Speed Rating

The cable assembly Speed Rating is based on the –7 dB insertion loss point of the mated cable assembly. The –7 dB point can be used to estimate usable system bandwidth in a typical two-level signaling environment.

To calculate the Speed Rating, the measured –7 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for any loss from the test board traces. The resulting loss value is then doubled to determine the approximate maximum data rate in

Gigabits per second (Gbps). The following table summarizes the Cable Assembly Speed Ratings for the ECDP cable assemblies tested.

Assembly		-7 dB Frequency	Speed Rating
ECDP-16-09.80-L1-L2-2-1	Long Row	8.5 GHz	17 Gbps
	Short Row	10.0 GHz	20 Gbps
ECDP-16-39.37-L1-L2-2-1	Long Row	8.0 GHz	16 Gbps
	Short Row	9.0 GHz	18 Gbps

Table 2: Cable Assembly Speed Rating

The Samtec Speed Rating is best considered a figure of merit for comparing relative performance between cable assemblies. The Speed Rating becomes less meaningful in systems using multi-level signaling or where crosstalk or impedance mismatch are more critical parameters. Modern high-speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The –7 dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

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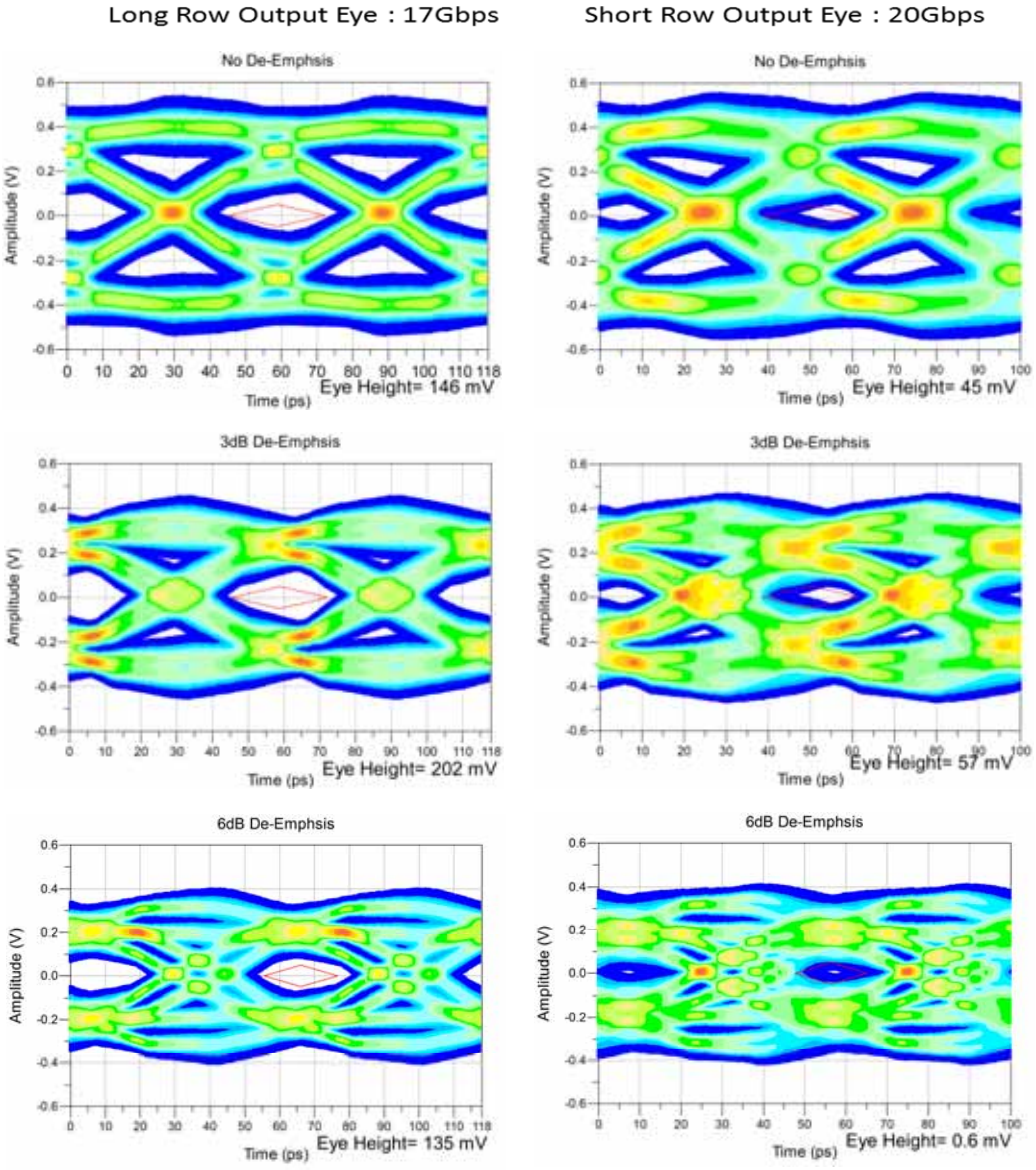
Eye Pattern Summary

ECDP-16-09.80-L1-L2-2-1



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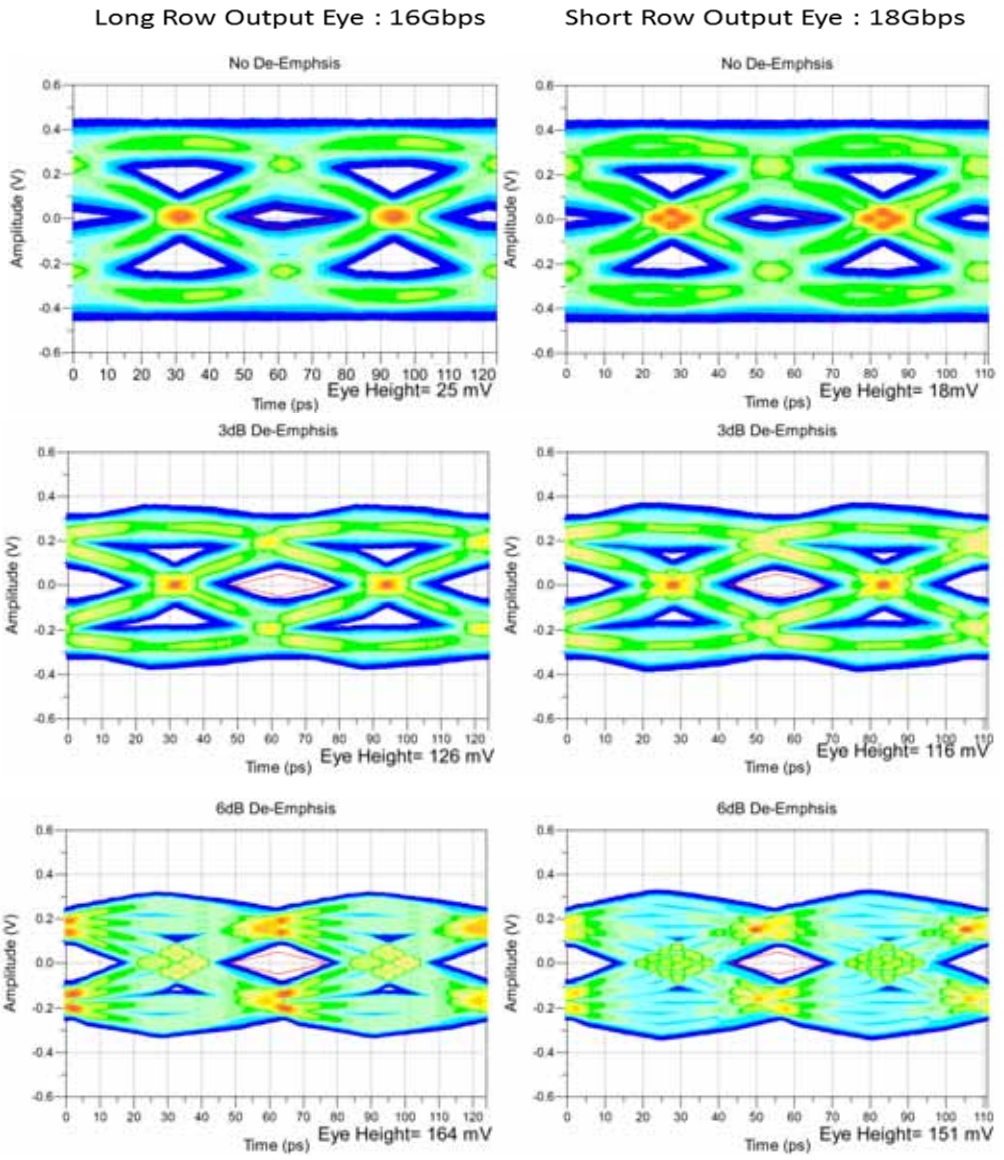
ECDP-16-39.37-L1-L2-2-1



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Frequency Domain Data Summary

Table 3 - Single-Ended Connector System Performance

Test Parameter	Configuration	Driver	Receiver	0.25m	1m
Insertion Loss	Long Row	L1_HSEC8_3,5	L2_HSEC8_4,6	7dB@ 8.4 GHz	7dB@ 7.8 GHz
	Short Row	L1_HSEC8_22,24	L2_HSEC8_21,23	7dB@ 9.6GHz	7dB@ 8.8 GHz
Return Loss	Long Row	L1_HSEC8_3,5	L1_HSEC8_3,5	>10dB to 0.7 GHz	>10dB to 0.9 GHz
	Short Row	L1_HSEC8_22,24	L1_HSEC8_22,24	>10dB to 0.7 GHz	>10dB to 0.8 GHz
Near-End Crosstalk	Cross Row	L1_HSEC8_3,5	L1_HSEC8_4,6	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Long Row	L1_HSEC8_3,5	L1_HSEC8_9,11	<-20dB to 12.2 GHz	<-20dB to 11.9GHz
	Cross Row	L1_HSEC8_22,24	L1_HSEC8_21,23	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Short Row	L1_HSEC8_22,24	L1_HSEC8_28,30	<-20dB to 12.0 GHz	<-20dB to 12 GHz
Far-End Crosstalk	Cross Row	L1_HSEC8_3,5	L2_HSEC8_3,5	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Long Row	L1_HSEC8_3,5	L2_HSEC8_10,12	<-20dB to 20 GHz	<-20dB to 20 GHz
	Cross Row	L1_HSEC8_22,24	L2_HSEC8_22,24	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Short Row	L1_HSEC8_22,24	L2_HSEC8_27,29	<-20dB to 20 GHz	<-20dB to 20 GHz

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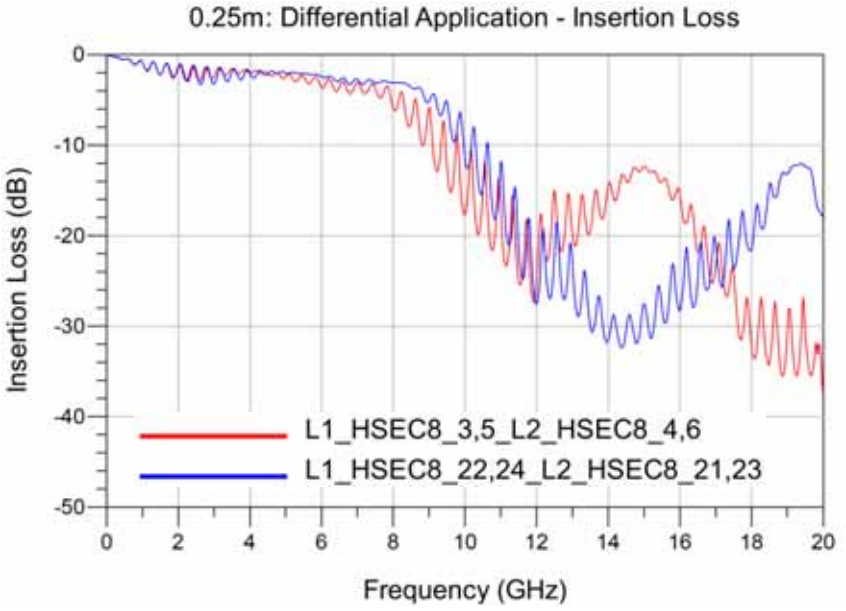
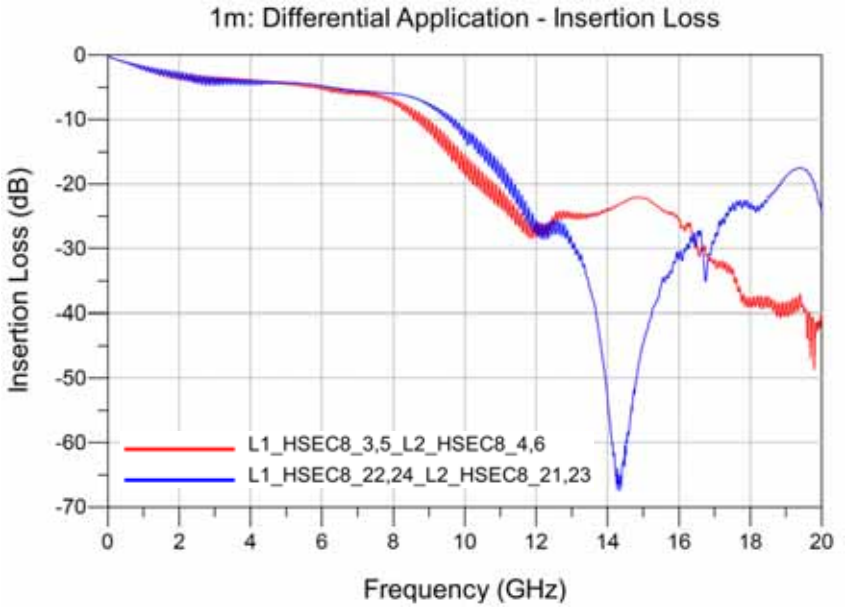
Bandwidth Chart – Differential Insertion Loss





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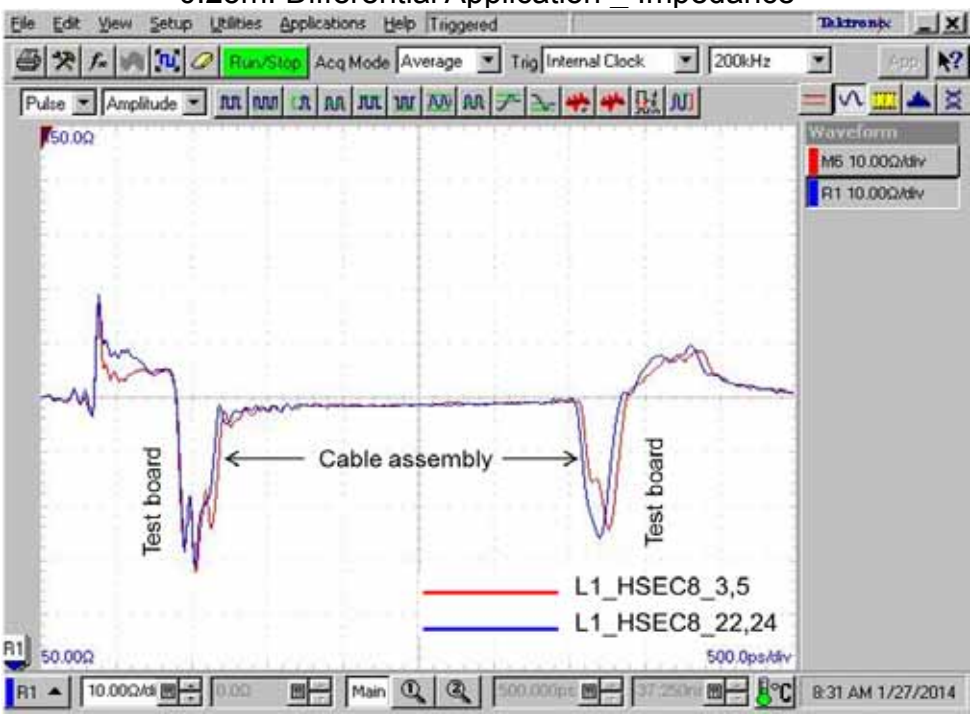
Time Domain Data Summary

0.25m: Differential Application _ Impedance



1m: Differential Application _ Impedance

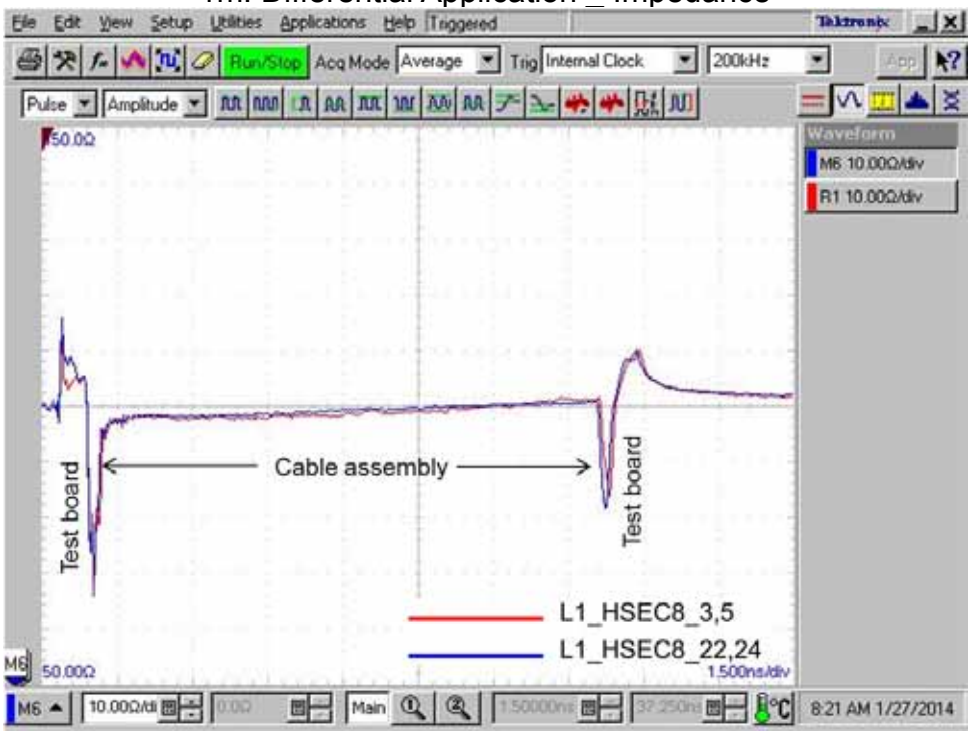


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Table 4 - Propagation Delay (Cable Assembly)		
Cable length	**Driver/ Receiver**	**Driver/ Receiver**
	L1_HSEC8_3,5/ L2_HSEC8_4,6	L1_HSEC8_22,24/ L2_HSEC8_21,23
0.25m	1.44ns	1.42ns
1m	5.23ns	5.20ns

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Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GSSG" differential drive configuration only.

Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this cable assembly, the following array configurations are evaluated:

Differential Impedance**:**

- Long Row (upper terminals, furthest from test fixture)
- Short Row (bottom terminals, closest to test fixture)

Differential Crosstalk**:**

- In Row: Long Row (adjacent terminals in the long row)
- In Row: Short Row (adjacent terminals in the short row)
- Cross Row: “Xrow”: (from one row of terminals to the other row)

See Appendix D – Product and Test System Descriptions for details

Two differential pairs were driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

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Eye Diagram Data

Eye patterns are a time domain characterization of system level performance. Eye patterns are generated by sending continuous streams of data from a transmitter to a receiver, and overlaying the received signals upon one another. Over time, the received data builds to resemble an eye. Negative SI effects in the transmission path can cause the signal to distort, which over time, will cause the eye to "close". Specifications, such as an eyemask template, can be placed on the amount of open area required in the eye to ensure a functional system.

An eyemask template is a representation of the receiver's sensitivity and is often used as a metric of performance. While there are lot-to-lot and vendor-to-vendor variations in receiver sensitivity, some general guidelines can be developed. After reviewing several major industry standards (PCIe, Gigabit Ethernet) we find similar eyemask requirements and we will use these as the basis for a generic template in this report. For this report we will assume a receiver amplitude sensitivity of 50 mVpp and a jitter margin of 0.5 UI. This results in a diamond shape eyemask template that is 50 mV high and 0.5 UI wide.

Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, and signal propagation time in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Agilent ADS to obtain the time domain response. Time Domain procedure is provided in Appendix F of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

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In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 6.5 mils of PCB trace on each connector side. Delay is measured at 30 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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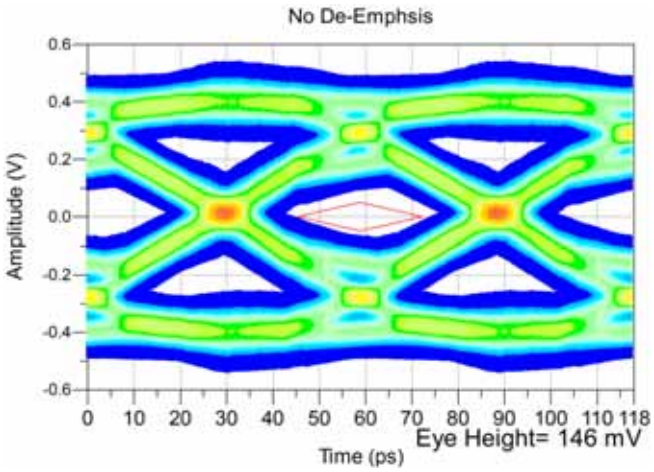
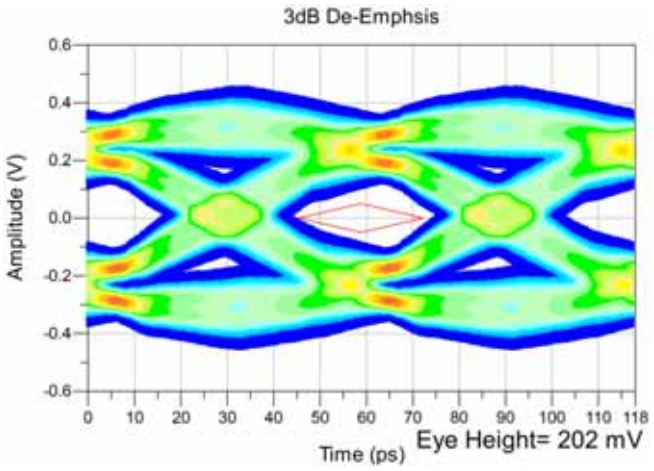
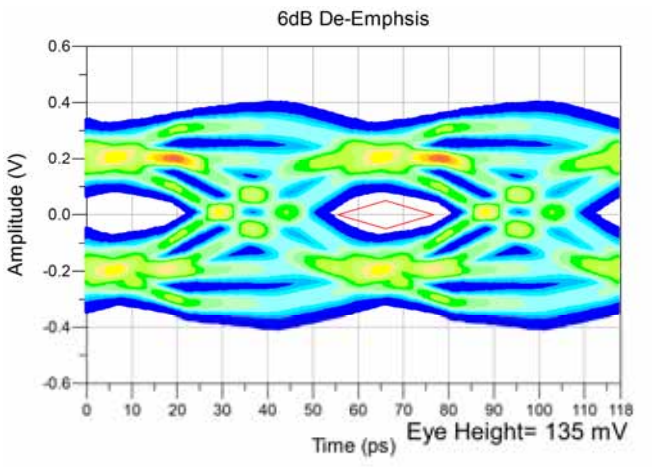
Appendix A – Eye Diagrams

ECDP-16-09.80-L1-L2-2-1

17Gbps: Long Row







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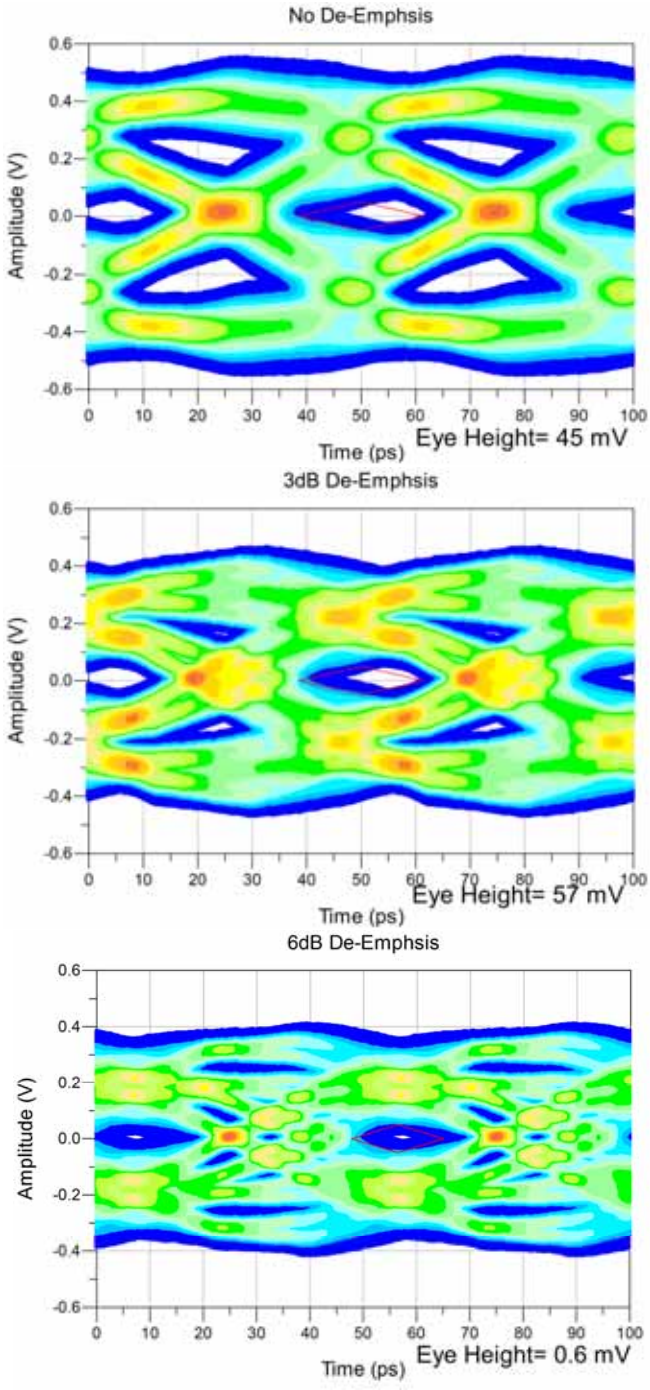
20Gbps: Short Row



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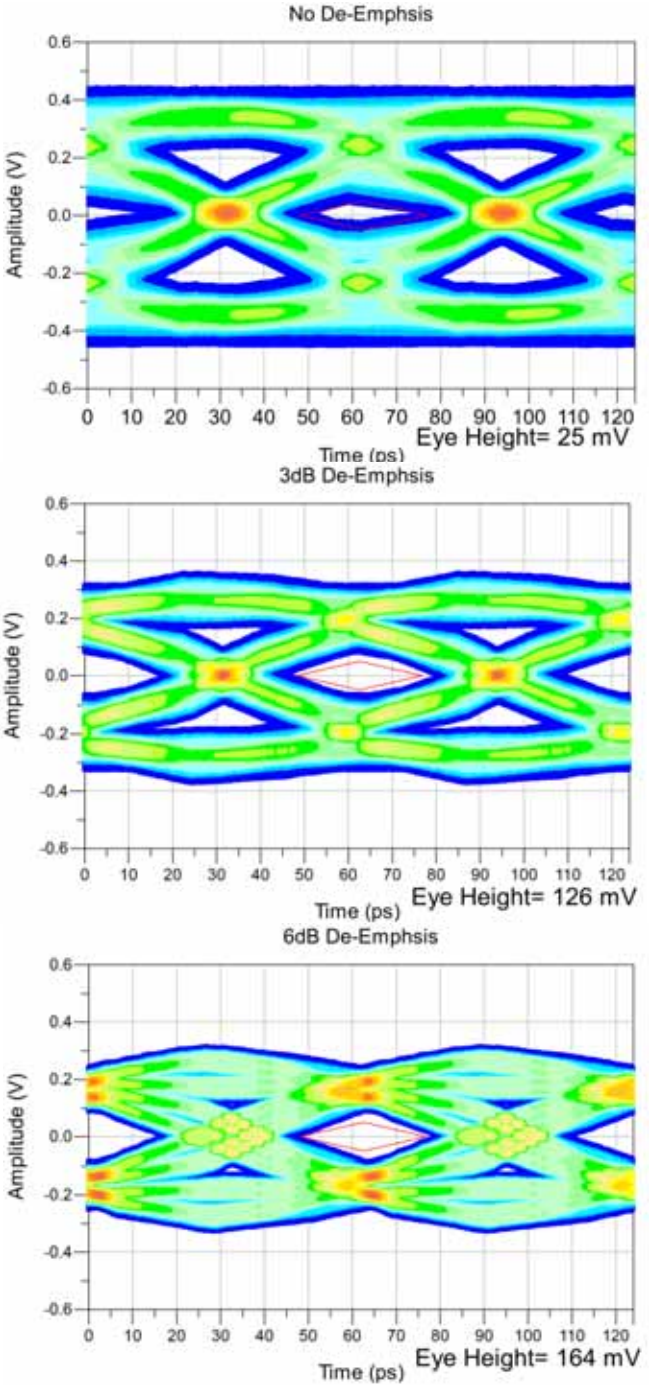
ECDP-16-39.37-L1-L2-2-1

16Gbps: Long Row



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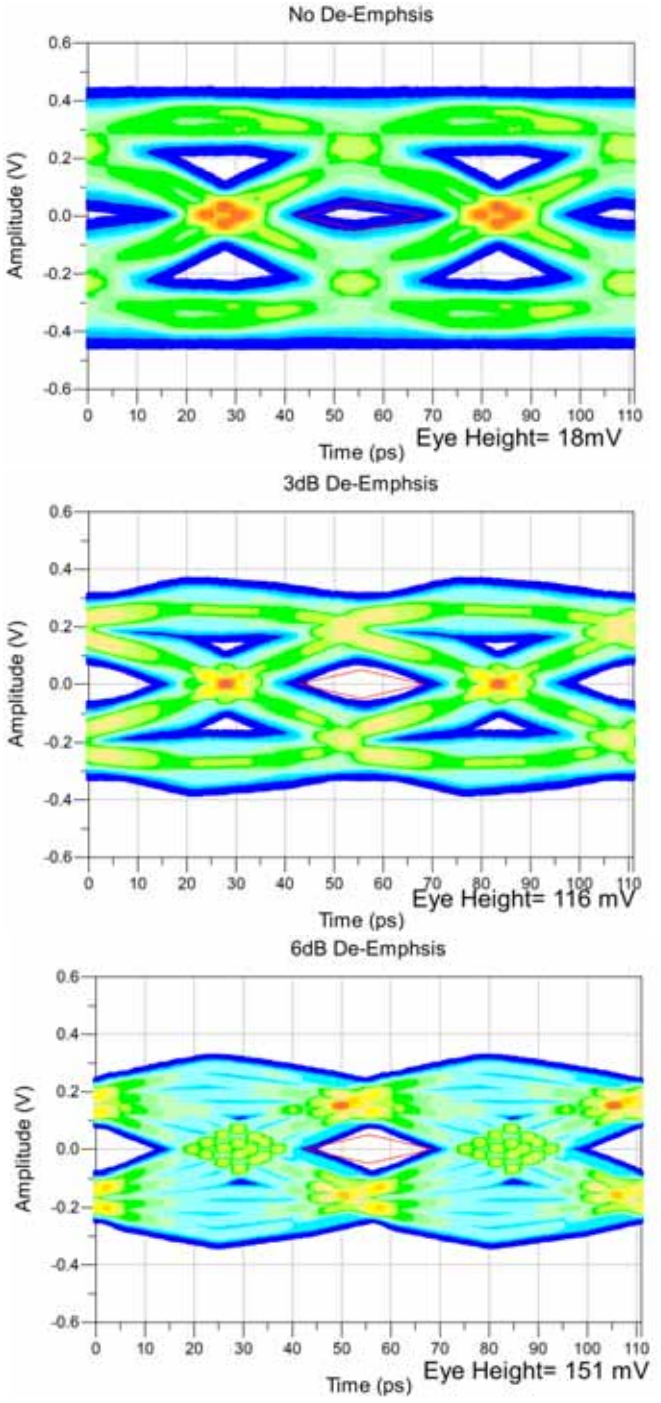
18Gbps: Short Row



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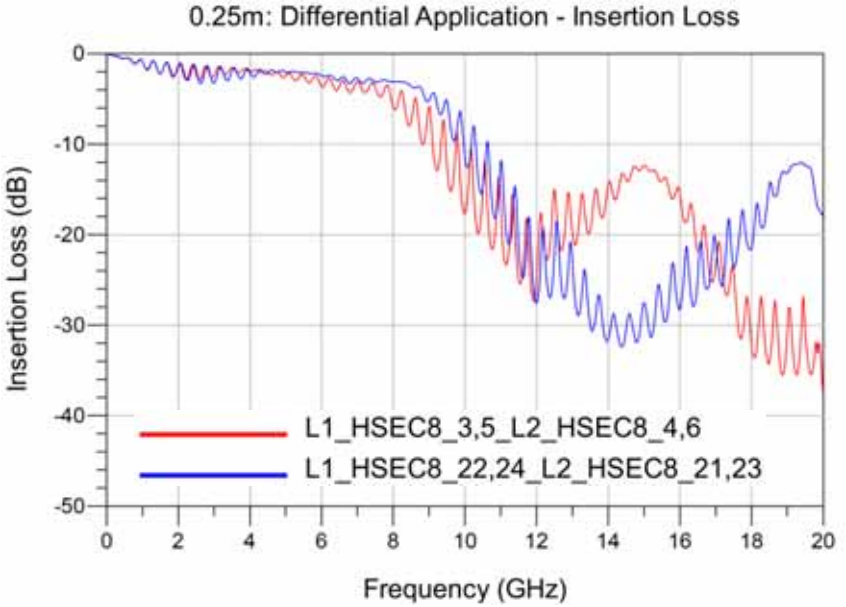
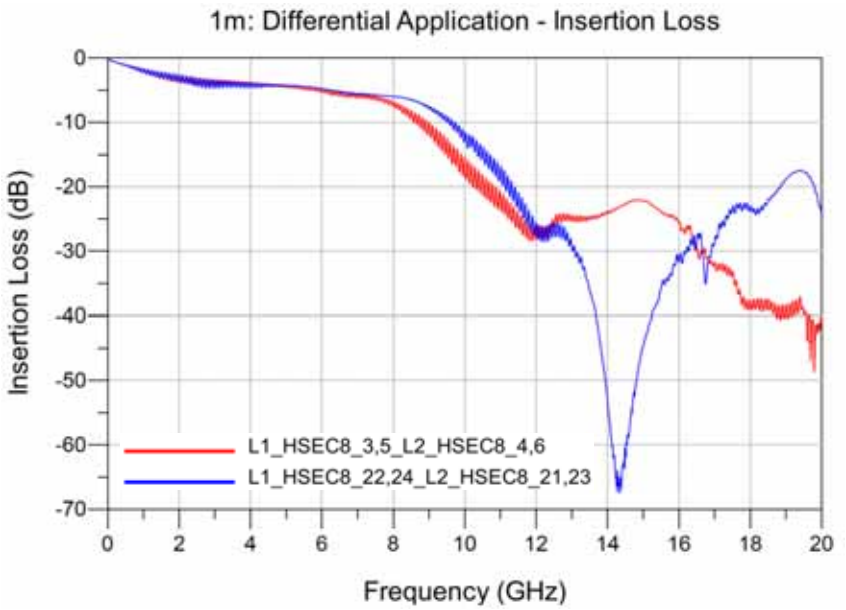
Appendix B – Frequency Domain Response Graphs

Differential Application – Insertion Loss





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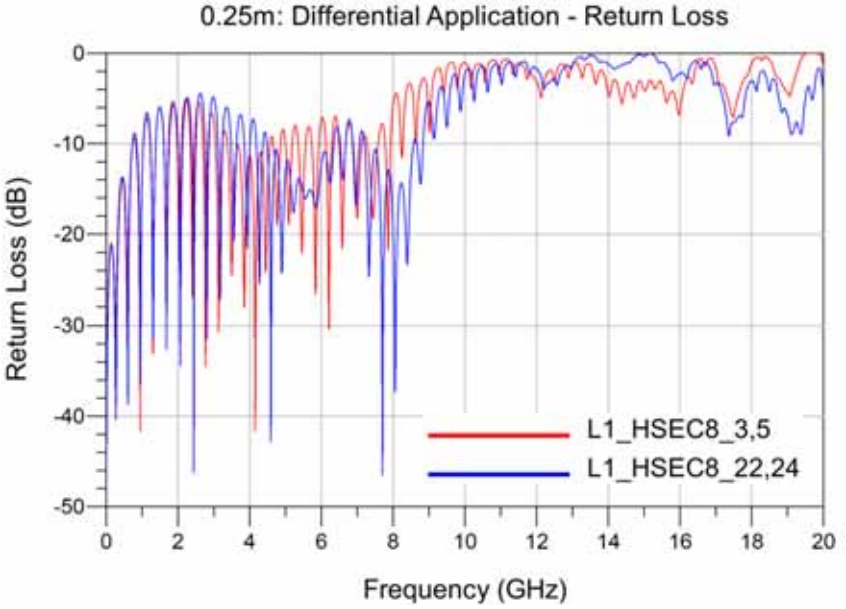
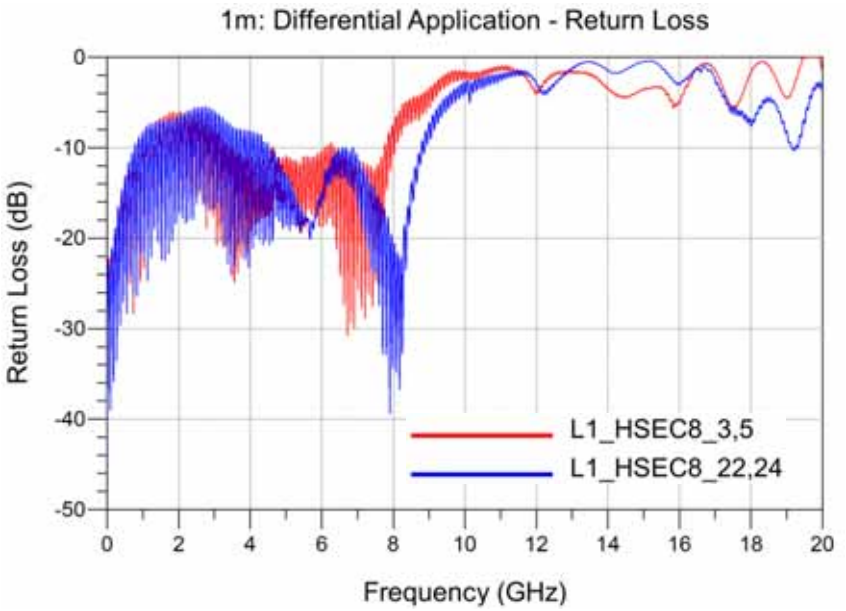
Differential Application – Return Loss





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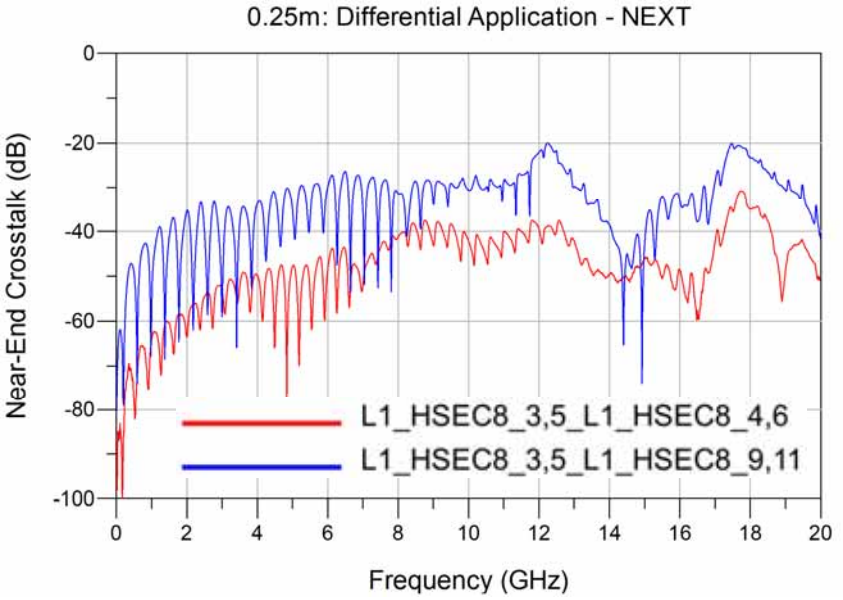
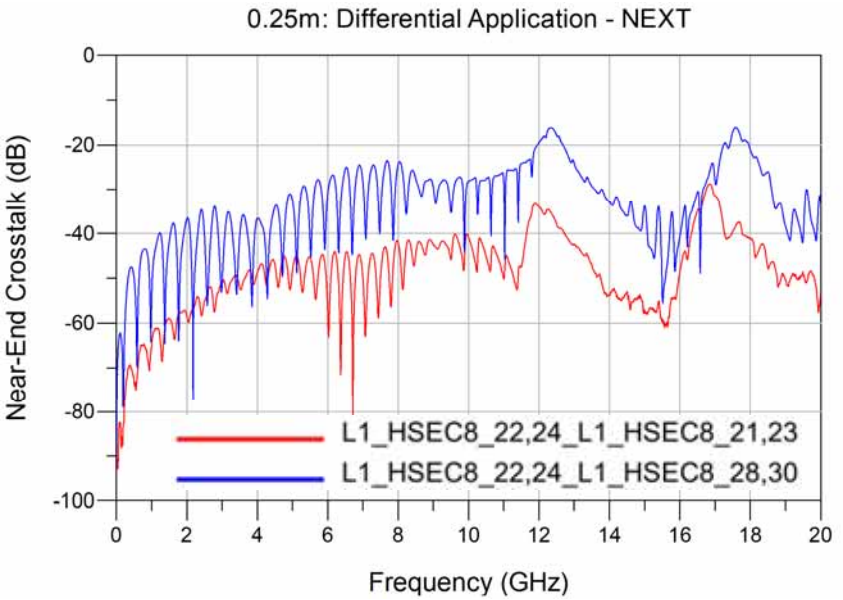
Differential Application – NEXT Configurations





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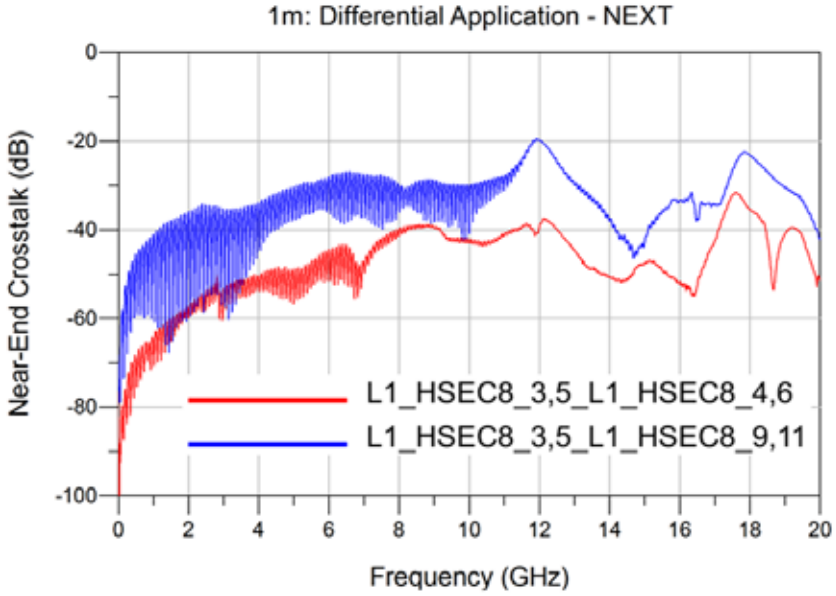

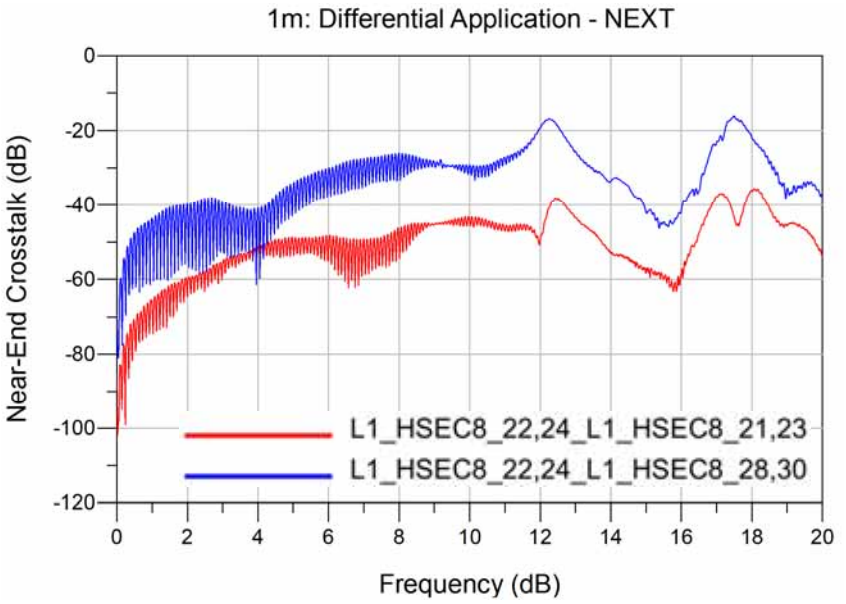

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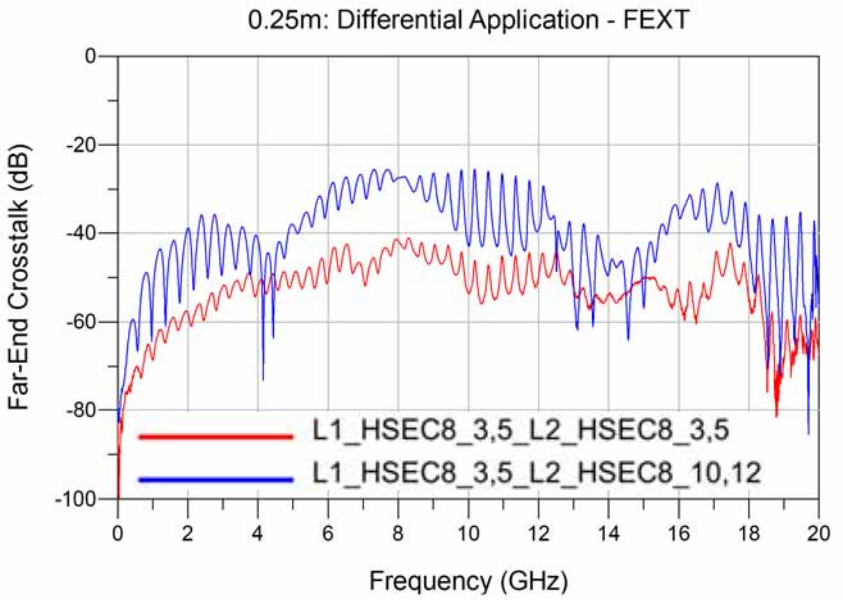
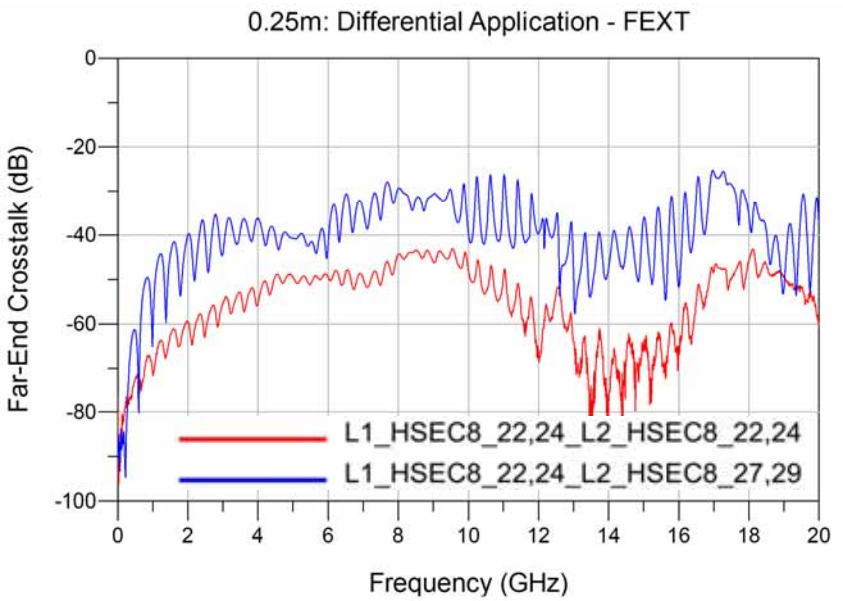
Differential Application – FEXT Configurations





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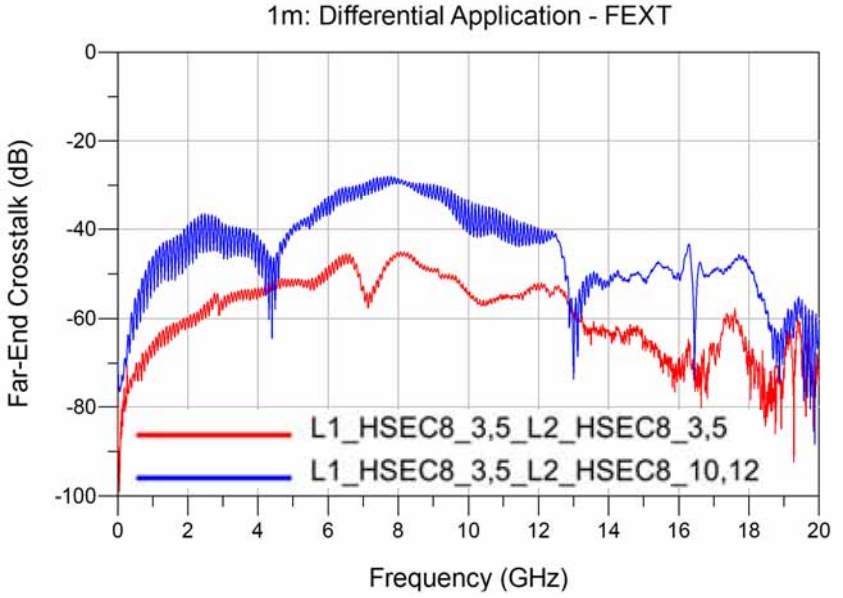

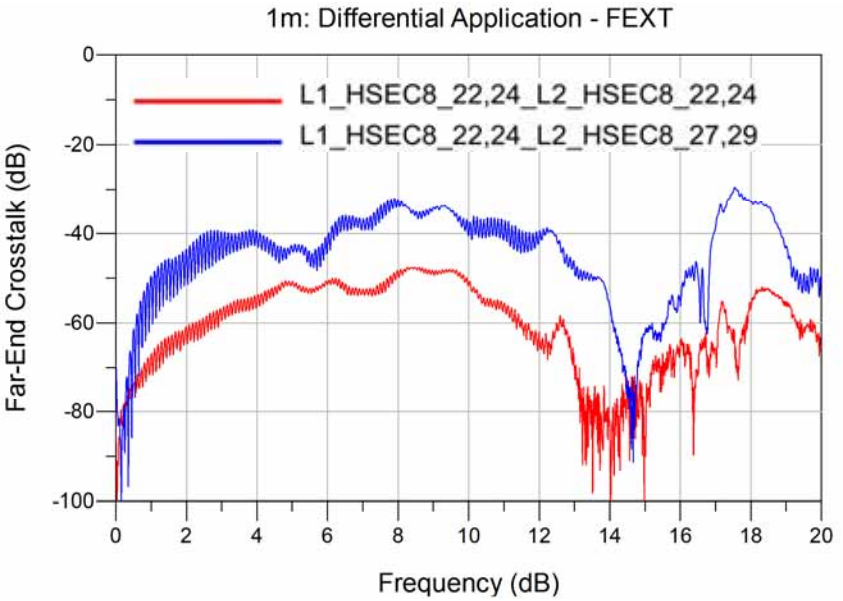

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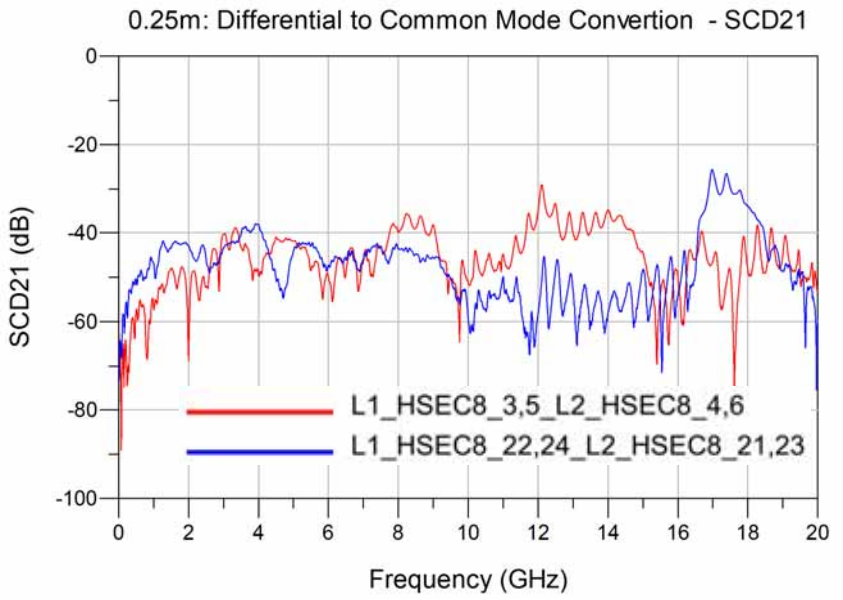
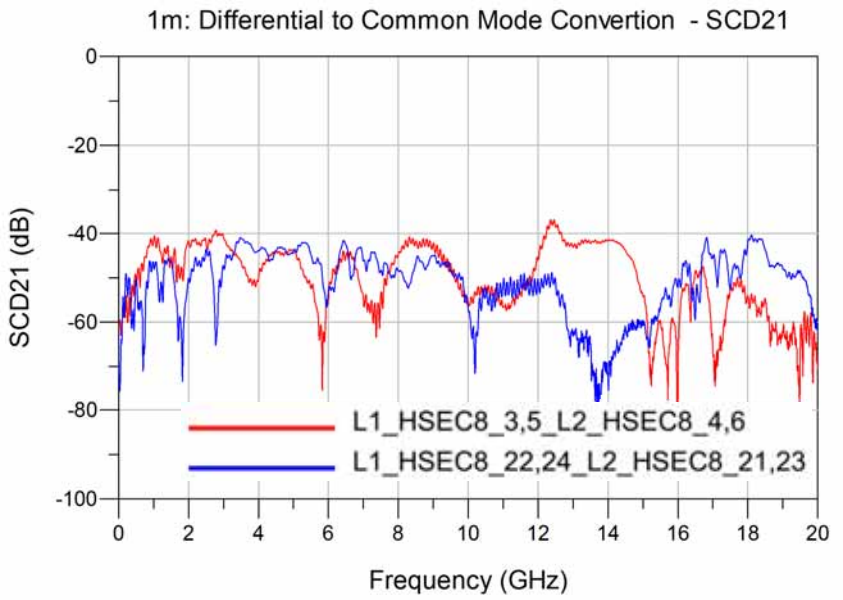
Differential Application – Differential to Common Mode Conversion





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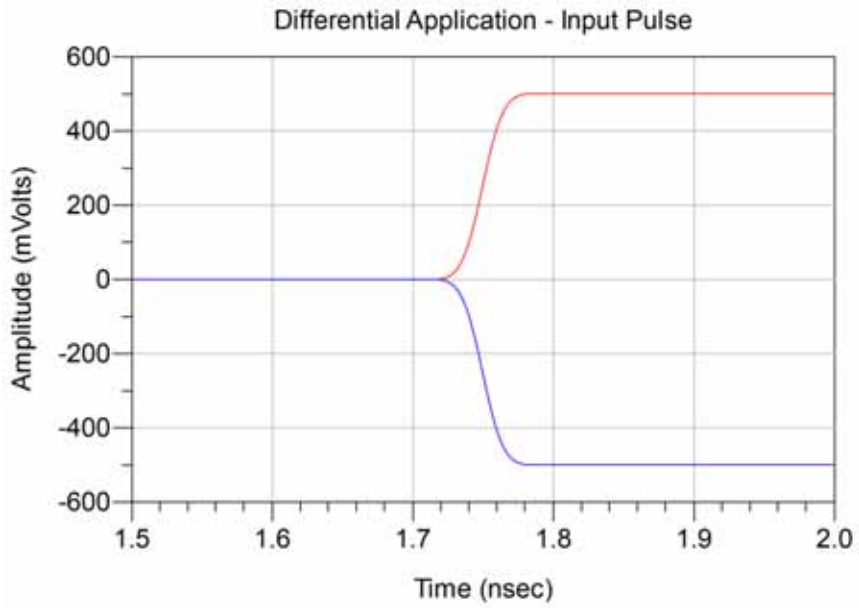
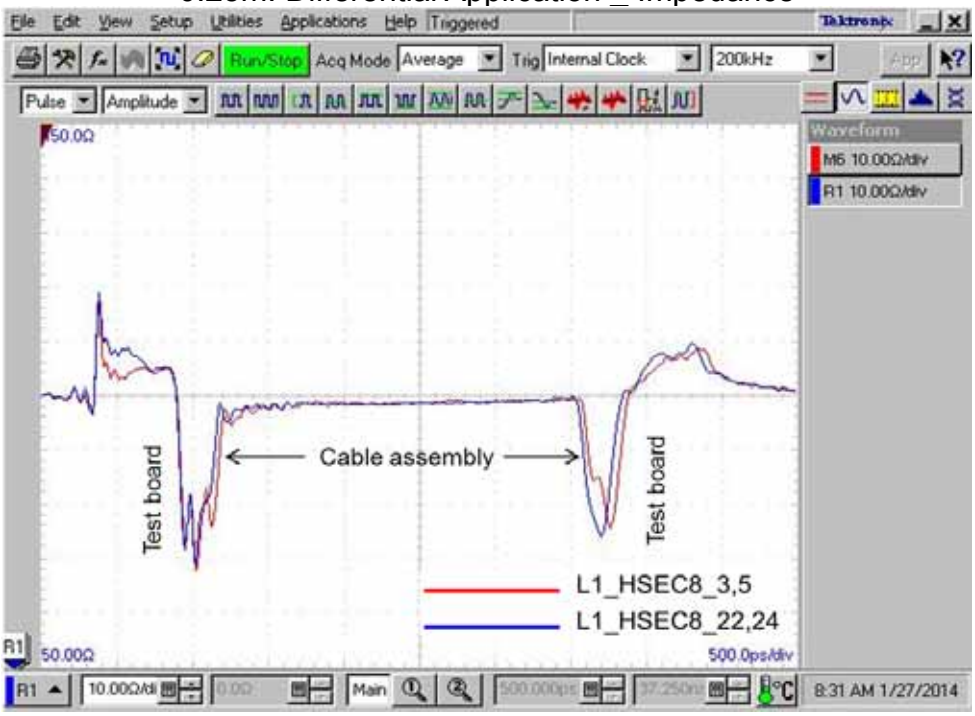
Appendix C – Time Domain Response Graphs

Differential Application – Input Pulse



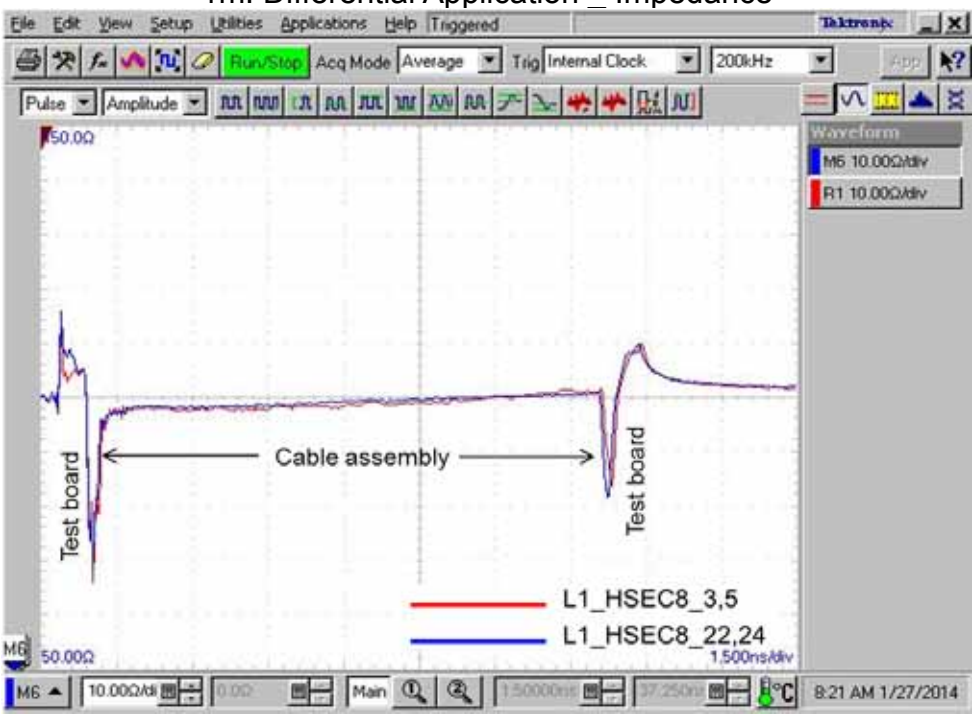
Differential Application – Cable Assembly Impedance

0.25m: Differential Application _ Impedance



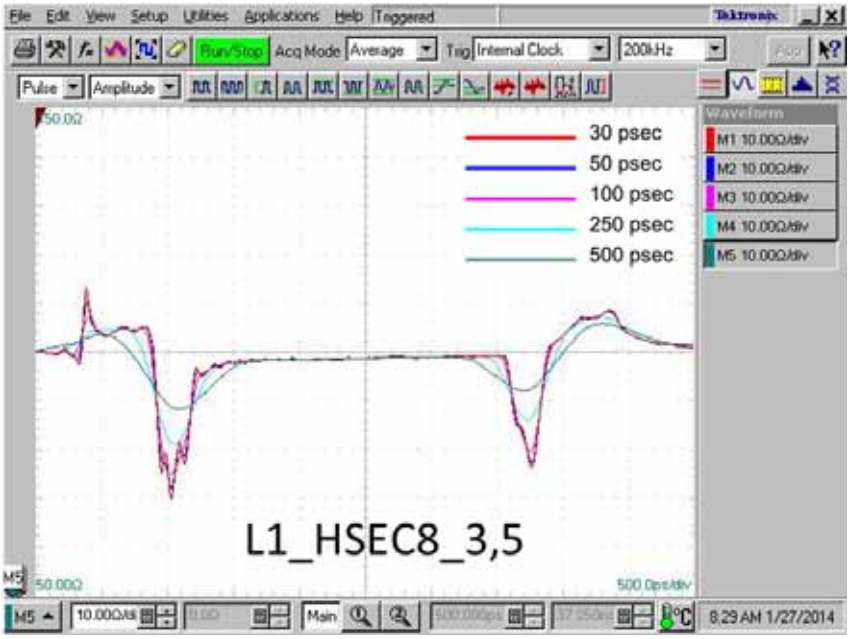
Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

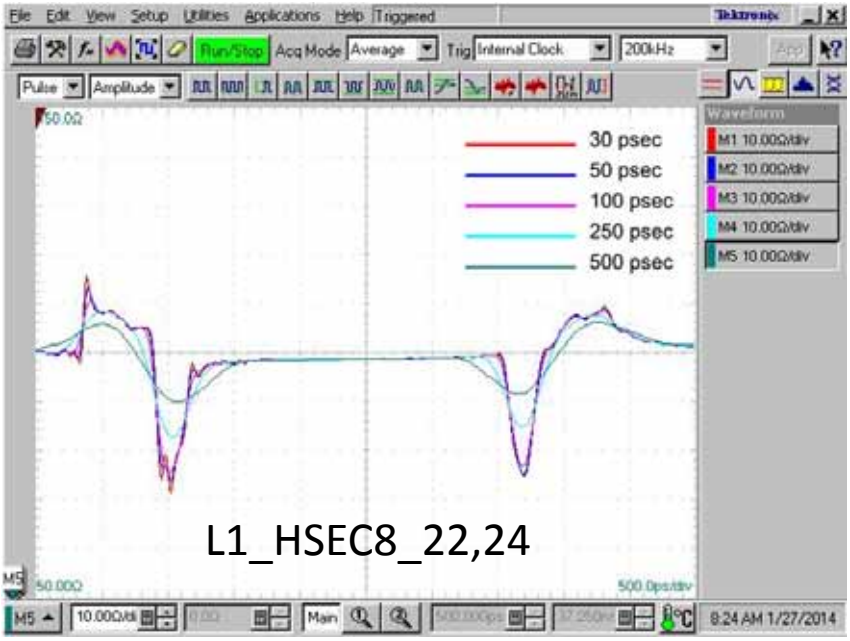
1m: Differential Application _ Impedance



Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable
Differential Application – Cable assembly Impedance

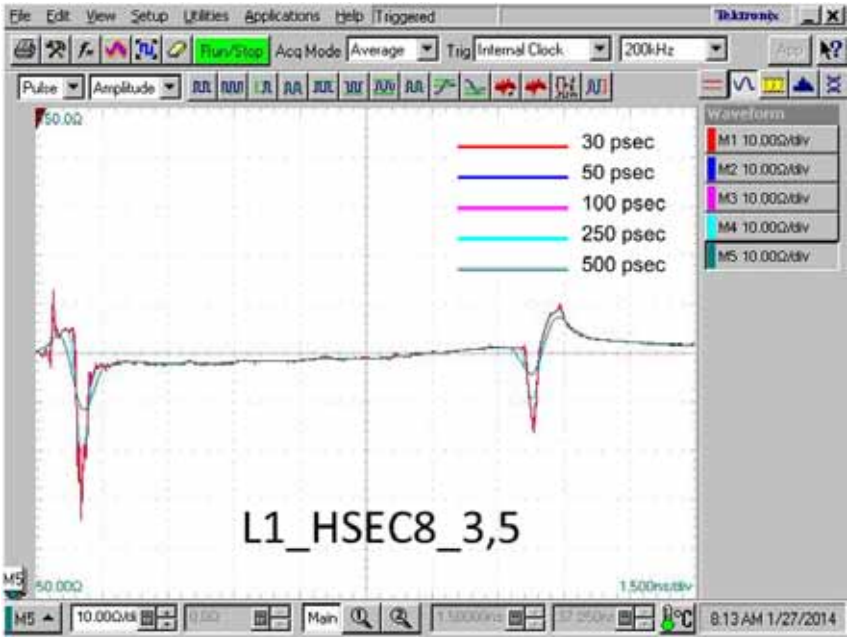
ECDP-16-09.80-L1-L2-2-1

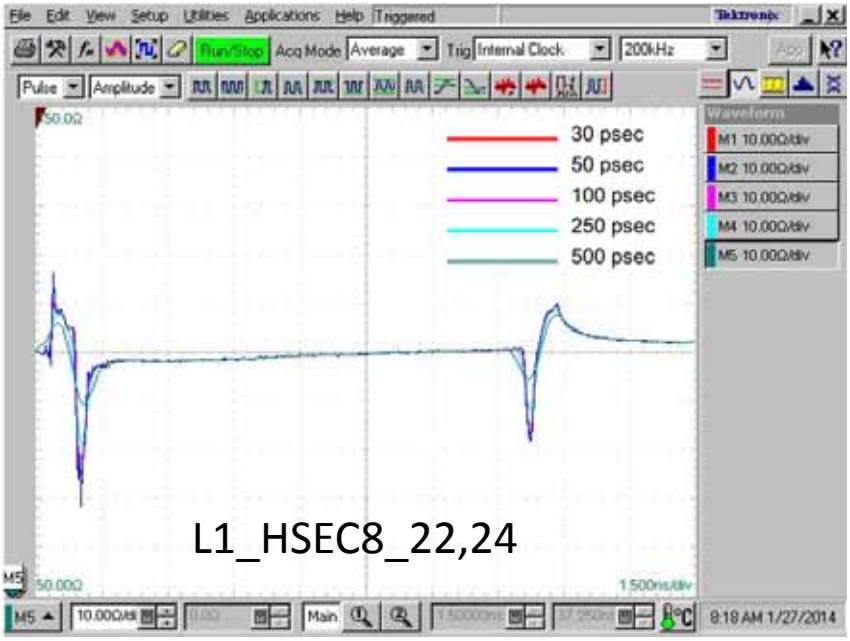




Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

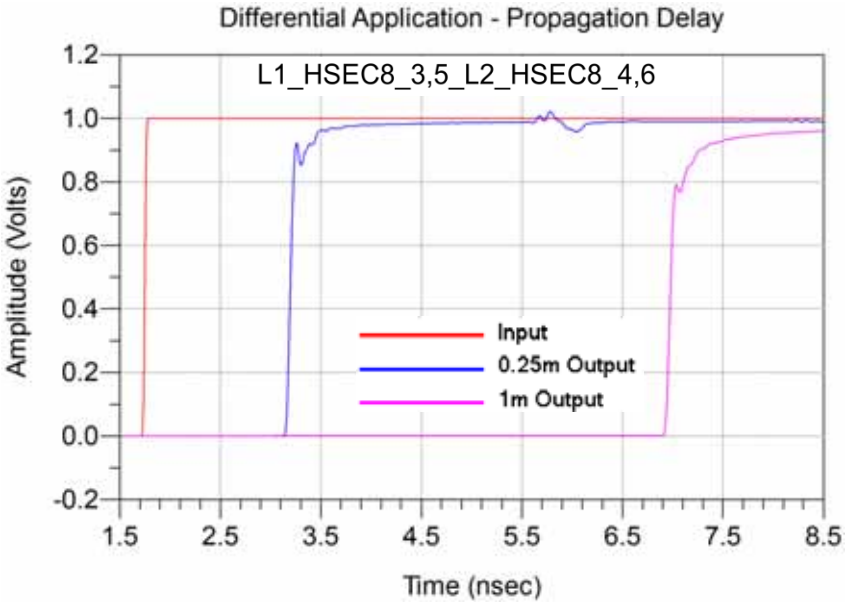
ECDP-16-39.37-L1-L2-2-1

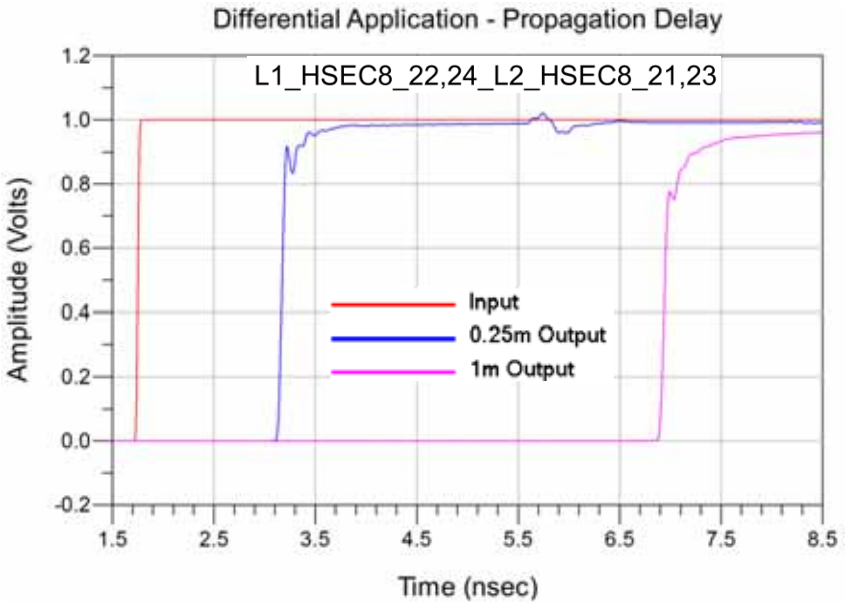




Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

Differential Application – Propagation Delay





Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

Appendix D – Product and Test System Descriptions

Product Description

Product test samples are 0.8mm Edge Rate coax cable assemblies. The part number are ECDP-16-09.80-L1-L2-2-1and ECDP-16-39.37-L1-L2-2-1, they mate with HSEC8-125-XX-XX-DV-X-XX. The cable assembly has two rows of 10 signal pairs evenly spaced on a 0.8 mm (0.0315") pitch. A photo of the mated test article mounted to SI test boards is shown below.

The coax cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in table below. There are a total of 16 positions per row. SMA jack numbers on the test boards correspond to the assembly line numbers. All adjacent lines are terminated where applicable.

G	**3**	**5**	G	9	11	KEY	G	15	17	G	21	23	G	27	29	G
G	4	6	G	10	12		G	16	18	G	**22**	**24**	G	28	30	G

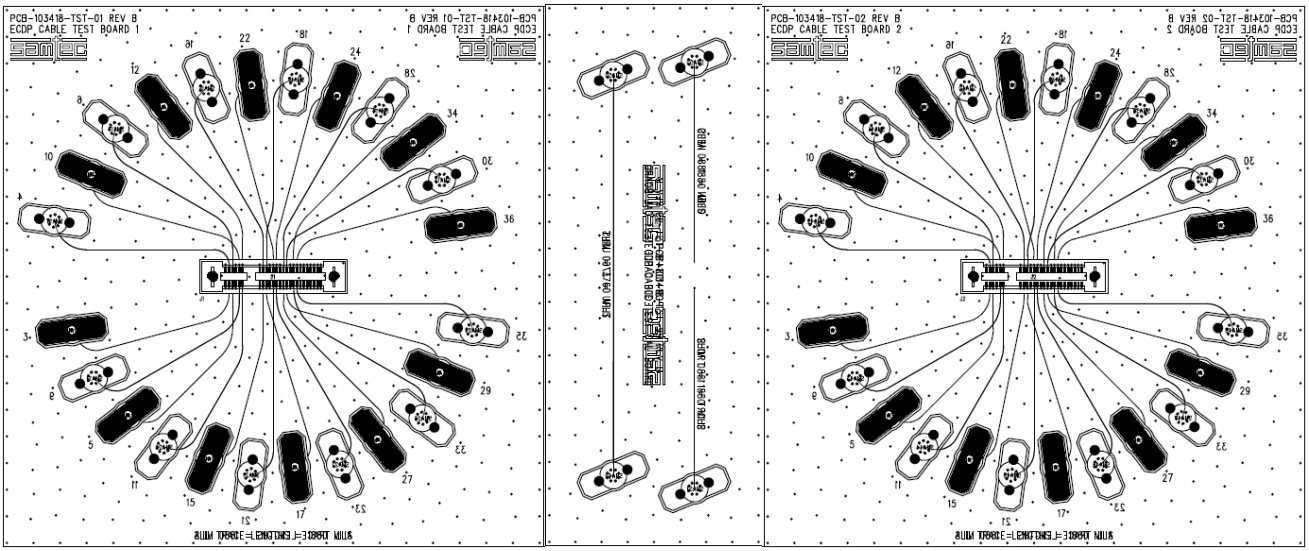
Table 5: Respective signal line numbers as viewed from End 1

Test System Description

The test fixtures are composed of six-layer FR-406 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Two test fixture specific to the ECDP series cable assembly identified by part PCB-103418-TST-01 and PCB-103418-TST-02. The Auto Fixture Removal (AFR) calibration structures designed specifically for the ECDP series are on the same test fixture. Displayed on the following pages is information for the ECDP/AFR calibration structure and directives for mating ECDP fixtures.

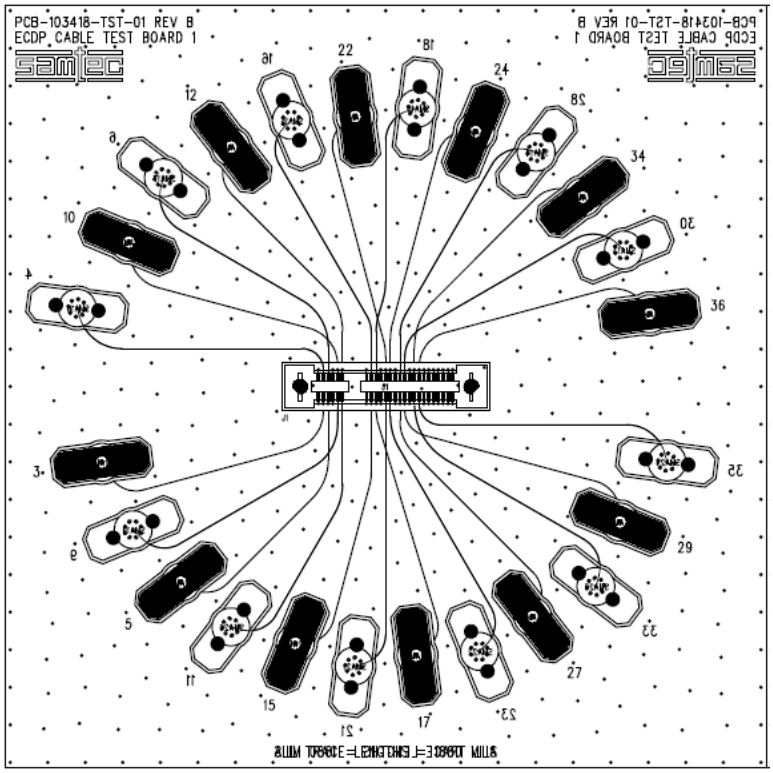
PCB-103418-TST-XX Test Fixtures

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable
Artwork of the PCB design is shown below.

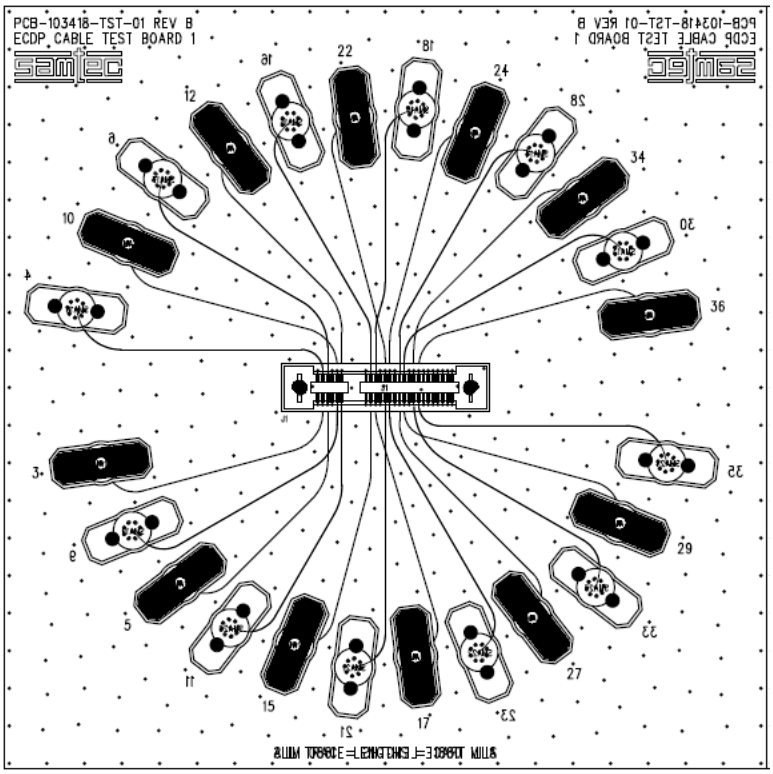


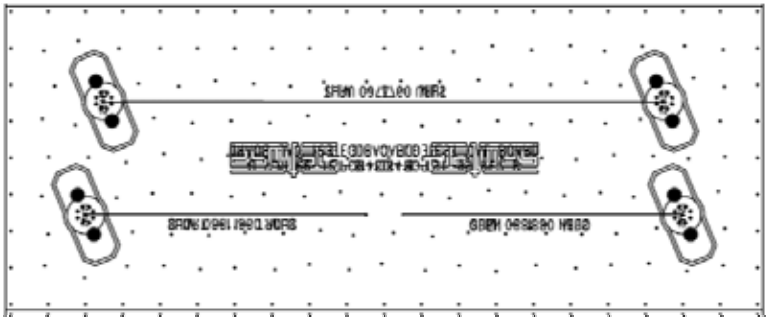
PCB Fixtures

The test fixtures used are as follows:



Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable





PCB-103418-TST-01 – ECDP Cable Test Board 1
PCB-103418-TST-02 – ECDP Cable Test Board 2
PCB-103418-TST-99 – Through

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

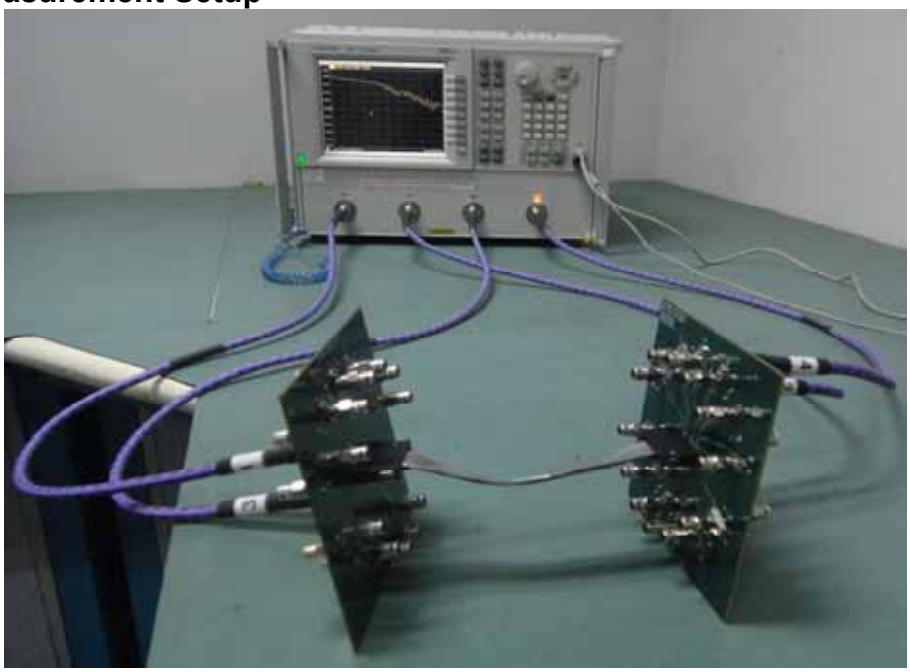
Appendix E – Test and Measurement Setup

The test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz	Number of points -1601
Stop Frequency – 20 GHz	IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable
For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale: 10 ohm / Div:
Offset: Default / Scroll
Horizontal Scale: 200ps/ Div
Record Length: 4000
Averages: ≥ 16

DSA8200 Measurement Setup

Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

Appendix F - Frequency and Time Domain Measurements

Eye Diagram Procedures

Eye Diagrams and statistical eye diagram metrics such as eye height can be generated by post-processing Frequency Domain measurements using Agilent ADS. Simulated data is sent over a touchstone model and the bits are overlain into an eye pattern.

Currently, no CEI specification is available for 7Gbps, so *CEI-28-VSR Working Clause Proposal, CEI Implementation agreement Draft 7.0*, dated May 14, 2012 was used for this report.

The simulation circuit is modeled as:
Agilent's Advanced Design System Tx and Rx modules that are configured to the *CEI-28-VSR Working Clause Proposal, CEI Implementation agreement Draft 7.0*, dated May 14, 2012.

- Tx parameters are specified in Section 1.3.3, *Module-to-Host Specifications*, Table 1-4, Page 7.
- Rx parameters defined in Section 1.3.2 *Host-to-Module Electrical Specifications*, Table 1-1, Page 5.
- A 1.0 inch length of Tx interconnect trace segment at the transmitter.
- SUT Cable Assembly S-Parameter measurements
  - 6.5 mils of 7.5 mil wide differential stripline signal trace
  - Test board vias, pads (footprint effects) for the HSEC8 connector
  - The HSEC8 series connector J1
  - The ECDP cable assembly
  - The HSEC8 series connector J2
  - Test board vias, pads (footprint effects) for the HSEC8 connector
  - 6.5 mils of 7.5 mil wide differential stripline signal trace
- A 1.0 inch length of Rx interconnect trace segment at the receiver.

All traces were modeled as microstrip on FR4 with the following parameters:

- The FR4 parameters are modeled using:
  - Er = 4.2 @ 1 GHz
  - Loss Tangent = 0.02 @ 1 GHz

- Copper is modeled as:
  - Conductivity = 4.5E+7 S-m
  - Surface roughness = 0.6 micron

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

- Traces are microstrip with the following geometry:
  - 7.5 mil trace width
  - 2 mil trace copper thickness
  - 4.4 mil FR4 dielectric thickness

Eye Mask

The eye mask is set for 50mVpp, with a jitter margin of 0.5 UI.

Rise Time

The 10-90 risetime of the 18Gbps signal was determined to be 19 psec, using the following formula:

Risetime = 0.35/Bandwidth

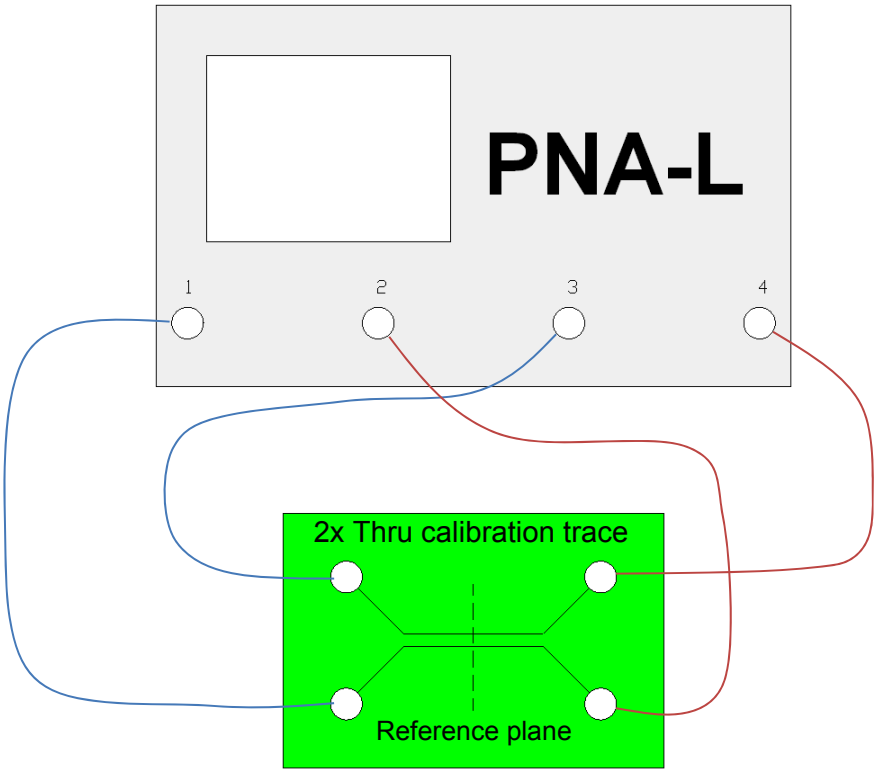
Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-cal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the ECDP test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.

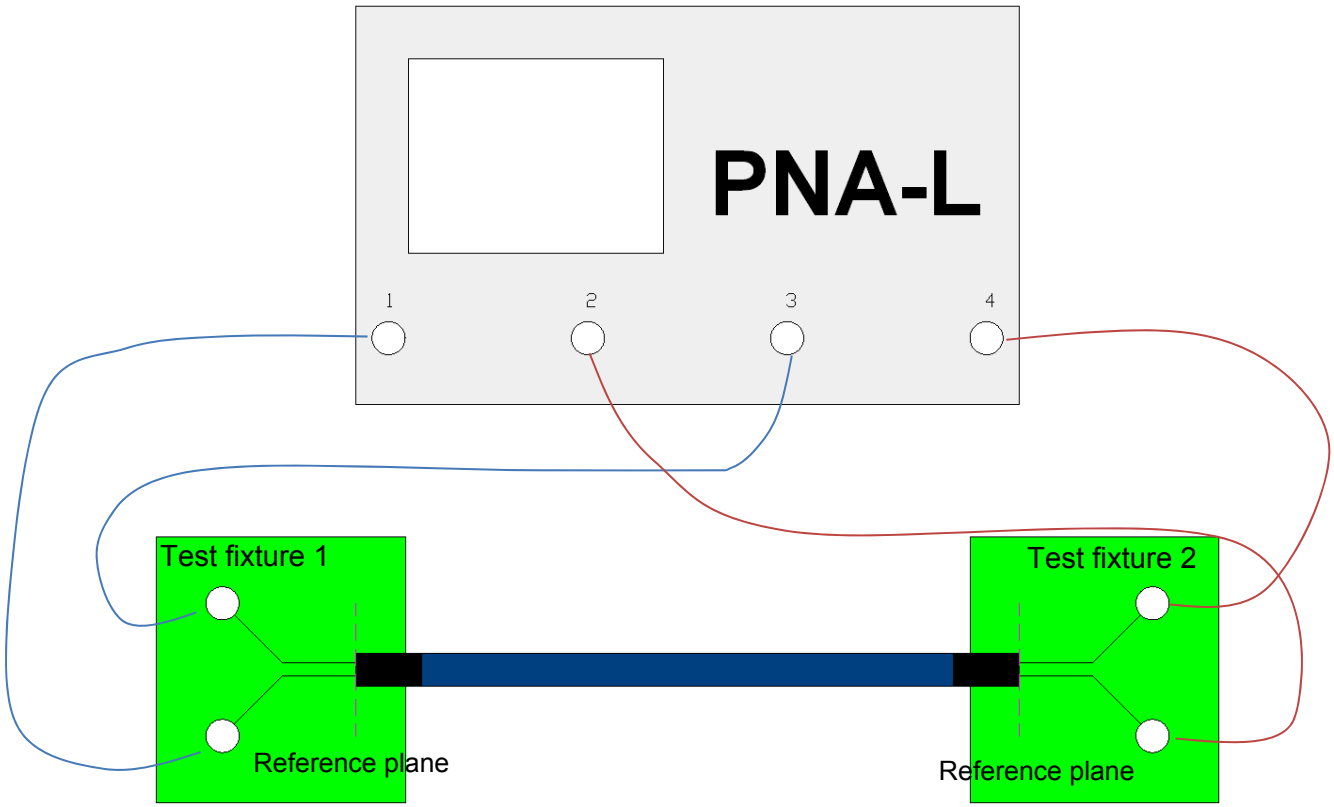


Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable
Measurements are then performed using the test boards as shown below. The test board effects are removed in post-processing via AFR in Agilent PLTS. The calibrated reference plane is located 6.5 mils from the connector footprint on each side. The S-Parameter measurements include:

A. 6.5 mils of 7.5 mil wide differential stripline signal trace
B. Test board vias, pads (footprint effects) for the HSEC8 connector
C. The HSEC8 series connector J1
D. The ECDP test cable
E. The HSEC8 series connector J2
F. Test board vias, pads (footprint effects) for the HSEC8 connector
G. 6.5 mils of 7.5 mil wide differential stripline signal trace

The test boards used for this characterization had a differential trace impedance of 112 ohms. Unfortunately, this impedance offset cascades through the AFR process and distorting the impedance and return loss measurements. For this reason, AFR was not applied to the impedance and return loss data in this report.

The figure below shows the location of the measurement reference plane.



Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with band-width-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)

A step pulse is applied to the touchstone model of the cable assembly and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Series: 0,80 mm (.0315") pitch ECDP
Description: High-Speed, 100Ω differential signal routing, Edge Card Cable Assembly,30 AWG ACCELERATE™ Twinax Cable

Appendix G – Glossary of Terms

ADS – Agilent Advanced Design System
AFR – Automatic Fixture Removal
CTLE – Continuous Time Linear Analyzer
CuFireFly™ - Copper FireFly™ assembly
DUT – Device under test
FD – Frequency domain
FEXT – Far-End Crosstalk
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PLTS – Agilent Physical Layer Design System
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
UI – Unit Interval
XROW – Across Row
Z – Impedance (expressed in ohms)