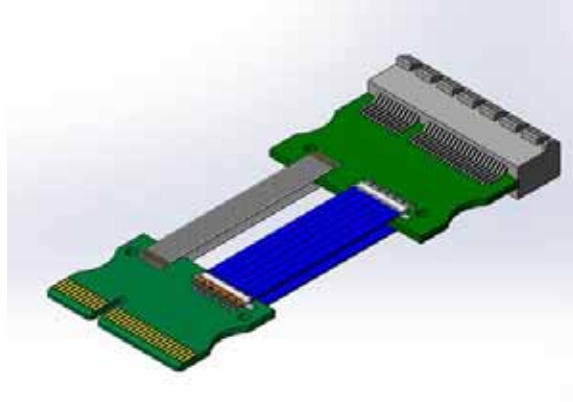




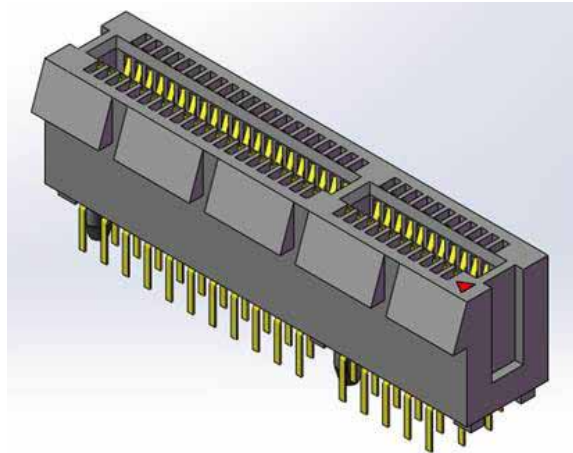
High Speed Characterization Report

PCIEC-XXX-XXXX-EC-EM-P-85



Mated with:

PCIE-XXX-02-X-D-TH



Description:

**1.00 mm PCI Express® Internal Cable Assembly,
32 AWG 85ohm Twinax Ribbon Cable**

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Table of Contents

Cable Assembly Overview	1
Cable Assembly Speed Rating.....	2
Eye Pattern Summary	3
Frequency Domain Data Summary	5
Bandwidth Chart – Differential Insertion Loss	6
Time Domain Data Summary	7
Characterization Details	9
Differential and Single-Ended Data.....	9
Cable assembly Signal to Ground Ratio	9
Eye Diagram Data	11
Frequency Domain Data.....	11
Time Domain Data.....	11
Appendix A – Eye Diagrams	13
Appendix B – Frequency Domain Response Graphs.....	17
Differential Application – Insertion Loss.....	17
Differential Application – Return Loss.....	18
Differential Application – NEXT Configurations	19
Differential Application – FEXT Configurations.....	21
Differential Application – Differential to Common Mode Conversion.....	23
Appendix C – Time Domain Response Graphs.....	24
Differential Application – Input Pulse	24
Differential Application – Cable Assembly Impedance.....	25
Differential Application – Cable assembly Impedance.....	26
Differential Application – Propagation Delay.....	28
Appendix D – Product and Test System Descriptions	29
Product Description	29
Test System Description.....	29
PCB-106420-SIG-XX Test Fixtures	29
PCB Fixtures	31
Appendix E – Test and Measurement Setup.....	32
N5230C Measurement Setup	32
Test Instruments.....	32
Test Cables & Adapters.....	32
DSA8200 Measurement Setup	33
Test Instruments.....	33
Test Cables & Adapters.....	33
Appendix F - Frequency and Time Domain Measurements	34
Eye Diagram Procedures.....	34
Eye Mask	35



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Rise Time	35
Frequency (S-Parameter) Domain Procedures	36
Time Domain Procedures	38
Propagation Delay (TDT)	38
Impedance (TDR).....	38
Appendix G – Glossary of Terms	39

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Cable Assembly Overview

The 1.00 mm (.0394") PCIEC Cable Assembly is constructed using Samtec 32 AWG, 85 Ω Twinax Ribbon Cable. The cable is terminated at the first end with an 85 Ω edge card connector and terminated at the second end with a PCIEC edge mount connector on an 85 Ω printed circuit board. The cable assembly is wired to facilitate a Pin 1 to Pin 1 mapping between the cable terminations. The PCIEC series cable assemblies are available in 36, 64, 98 and 164 positions. The data in this report is only applicable to 250 mm and 1000 mm length cable assembly.

Each PCIEC cable assembly was tested by mating it to a PCI Express Card Socket at the first end and edge-card test board at the second end. One sample of each assembly was tested. The actual part numbers that were tested are shown in Table 1, which also identifies End 1 and End 2 of each assembly. A relative sample picture is shown in Figure 1. Two differential pairs, a Long Path and a Short Path, of each assembly type were tested.

Length	Part Number	End 1	End 2
250 mm	PCIEC-064-0250-EC-EM-P-85	Edge-Card	Edge Mount Connector
1000 mm	PCIEC-064-1000-EC-EM-P-85	Edge-Card	Edge Mount Connector

Table 1: Sample Description

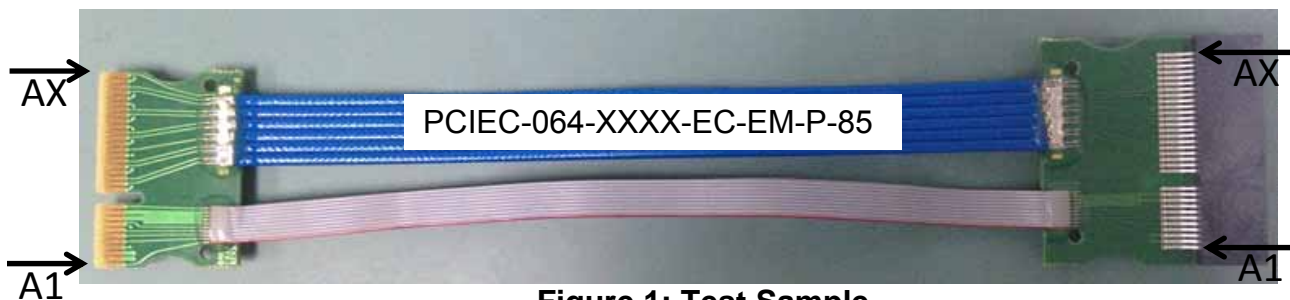


Figure 1: Test Sample

Series: PCIEC-85**Description:** PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Cable Assembly Speed Rating

The cable assembly Speed Rating is based on the -7 dB insertion loss point of the mated cable assembly. The -7 dB point can be used to estimate usable system bandwidth in a typical two-level signaling environment.

To calculate the Speed Rating, the measured -7 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for any loss from the test board traces. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps). The following table summarizes the Cable Assembly Speed Ratings for the PCIEC cable assemblies tested.

Assembly		-7 dB Frequency	Speed Rating
PCIEC-064-0250-EC-EM-P	Long Row	4.5 GHz	9 Gbps
	Short Row	4.5 GHz	9 Gbps
PCIEC-064-1000-EC-EM-P	Long Row	4.0 GHz	8 Gbps
	Short Row	4.0 GHz	8 Gbps

Table 2: Cable Assembly Speed Rating

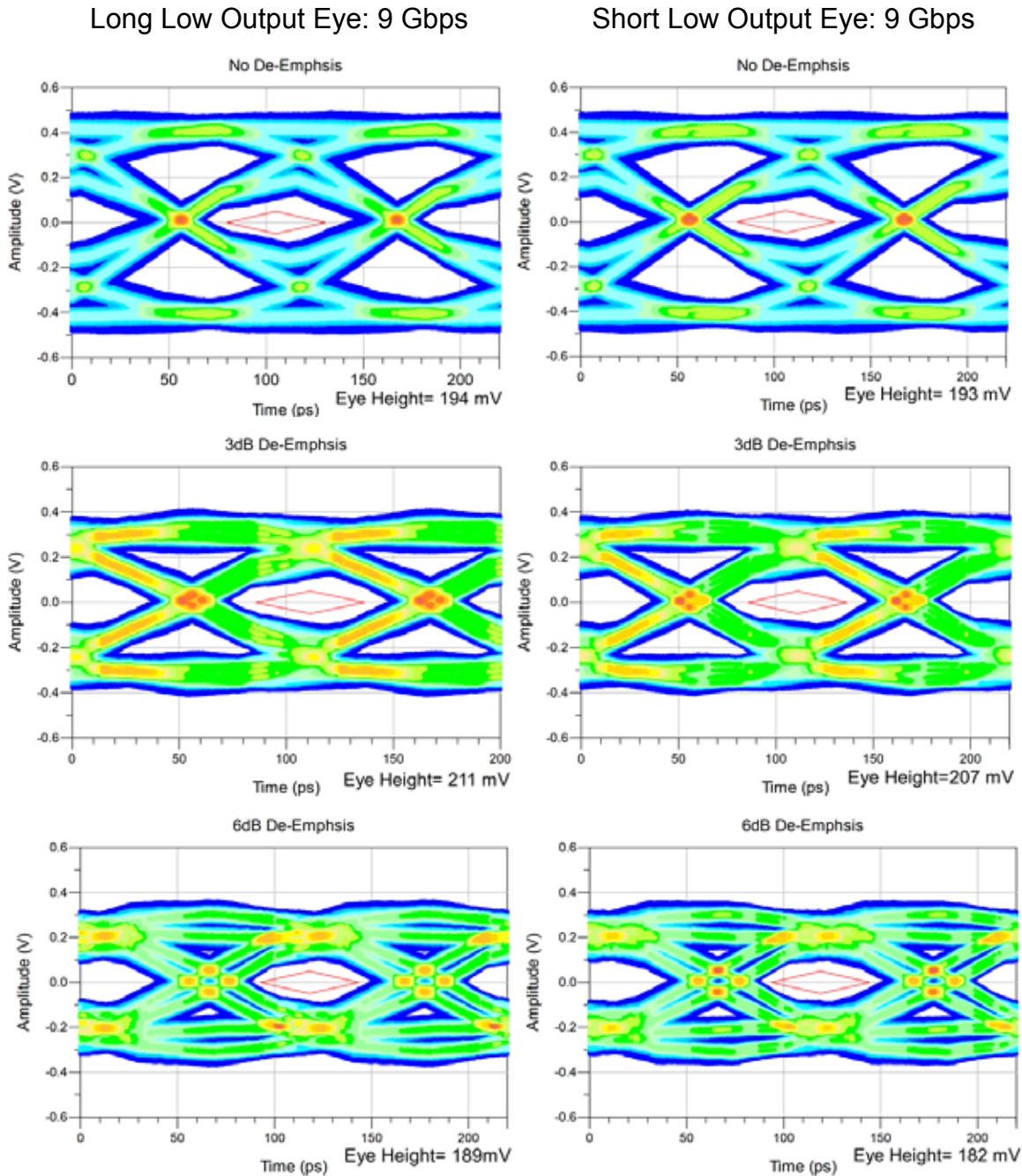
The Samtec Speed Rating is best considered a figure of merit for comparing relative performance between cable assemblies. The Speed Rating becomes less meaningful in systems using multi-level signaling or where crosstalk or impedance mismatch are more critical parameters. Modern high-speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The -7 dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Eye Pattern Summary

PCIEC-064-0250-EC-EM-P-85



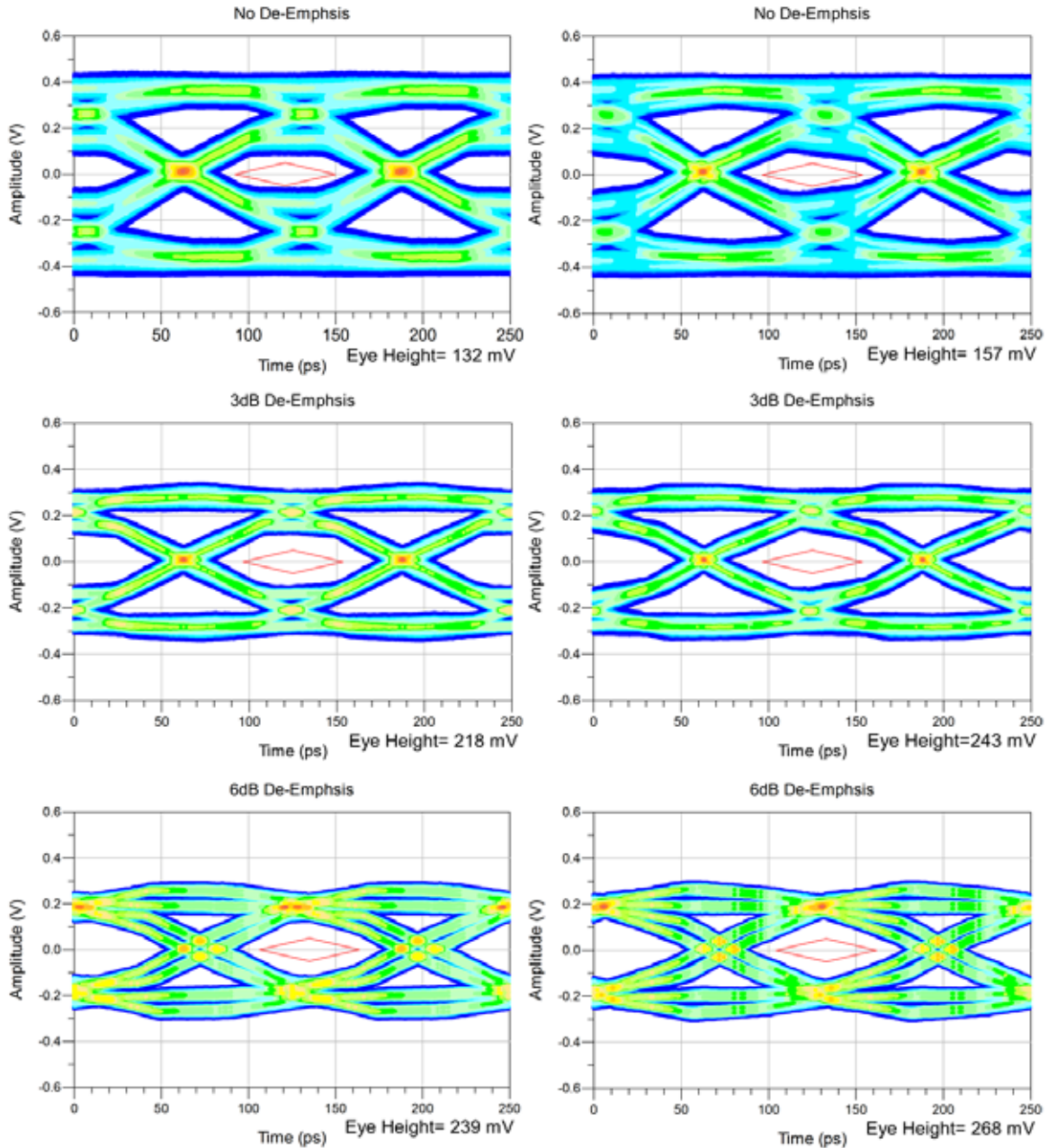
Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

PCIEC-064-1000-EC-EM-P-85

Long Low Output Eye: 8 Gbps

Short Low Output Eye: 8 Gbps



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

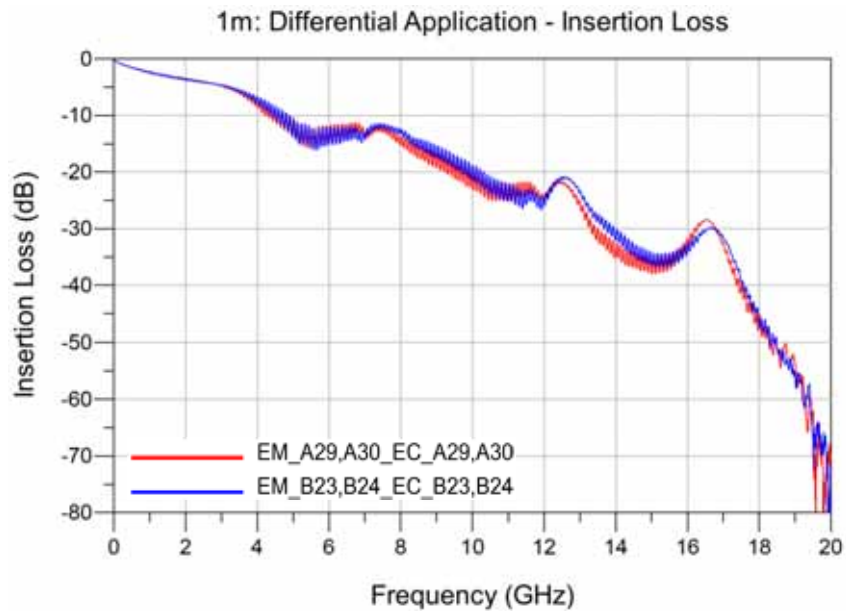
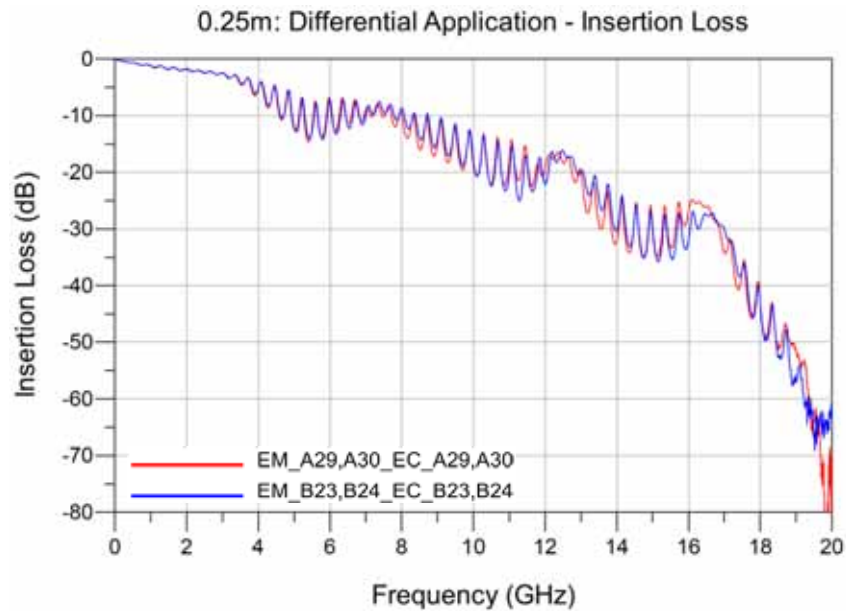
Frequency Domain Data Summary

Table 3 - Single-Ended Connector System Performance					
Test Parameter	Configuration	Driver	Receiver	0.25m	1m
Insertion Loss	Long Row	EM_A29,A30	EC_A29,A30	7dB@ 4.2 GHz	7dB@ 3.7 GHz
	Short Row	EM_B23,B24	EC_B23,B24	7dB@ 4.2 GHz	7dB@ 3.8 GHz
Return Loss	Long Row	EM_A29,A30	EM_A29,A30	>10dB to 3.2 GHz	>10dB to 3.3 GHz
	Short Row	EM_B23,B24	EM_B23,B24	>10dB to 3.2 GHz	>10dB to 3.4 GHz
Near-End Crosstalk	In Row: Long Row	EM_A25,A26	EM_A29,A30	<-20dB to 5.3 GHz	<-20dB to 18.0 GHz
	In Row: Long Row	EM_A13,A14	EM_A16,A17	<-20dB to 5.3 GHz	<-20dB to 5.3 GHz
	Across Row	EM_A13,A14	EM_B14,B15	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Short Row	EM_B23,B24	EM_B27,B28	<-20dB to 20 GHz	<-20dB to 5.6 GHz
	Across Row	EM_A25,A26	EM_B23,B24	<-20dB to 20 GHz	<-20dB to 20 GHz
Far-End Crosstalk	In Row: Long Row	EM_A25,A26	EC_A29,A30	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Long Row	EM_A13,A14	EC_A16,A17	<-20dB to 20 GHz	<-20dB to 20 GHz
	Across Row	EM_A13,A14	EC_B14,B15	<-20dB to 20 GHz	<-20dB to 20 GHz
	In Row: Short Row	EM_B23,B24	EC_B27,B28	<-20dB to 20 GHz	<-20dB to 20 GHz
	Across Row	EM_A25,A26	EC_B23,B24	<-20dB to 20 GHz	<-20dB to 20 GHz

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Bandwidth Chart – Differential Insertion Loss

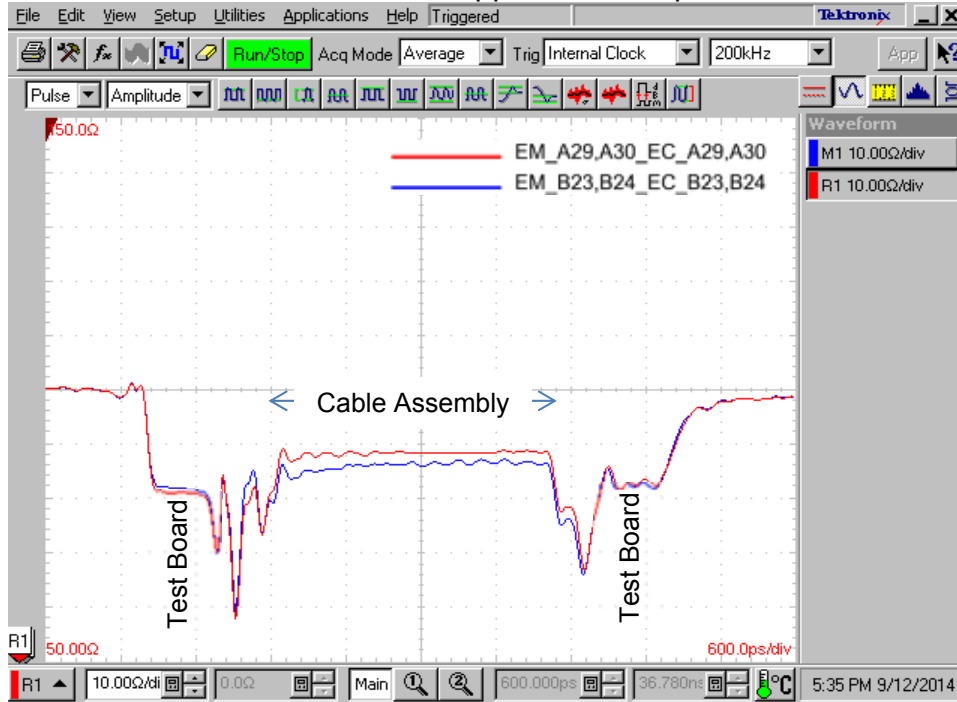


Series: PCIEC-85

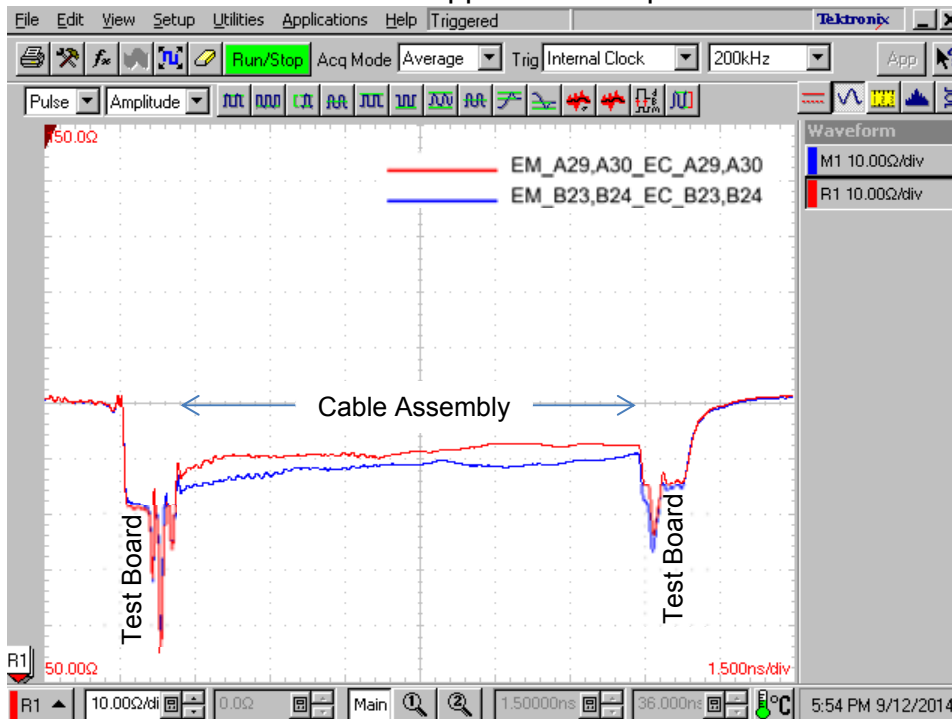
Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Time Domain Data Summary

0.25m: Differential Application - Impedance



1m: Differential Application - Impedance



Series: PCIEC-85**Description:** PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Table 4 - Propagation Delay (Cable Assembly)		
Cable length	Driver/ Receiver	Driver/ Receiver
		EM_A29,A30/ EC_A29,A30
0.25m	1.571ns	1.566ns
1m	5.132ns	5.121ns

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal the typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GSSG" differential drive configuration only.

Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

For this cable assembly, the following array configurations are evaluated:

Differential Impedance:

- Long Row (upper terminals, furthest from test fixture)
- Short Row (bottom terminals, closest to test fixture)

Differential Crosstalk:

- In Row: Long Row (adjacent terminals in the long row)
- In Row: Short Row (adjacent terminals in the short row)
- Across Row: “Xrow”: (from one row of terminals to the other row)

See Appendix D – Product and Test System Descriptions for details

Only one differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time)

In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or the rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate the worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Eye Diagram Data

Eye patterns are a time domain characterization of system level performance. Eye patterns are generated by sending continuous streams of data from a transmitter to a receiver, and overlaying the received signals upon one another. Over time, the received data builds to resemble an eye. Negative SI effects in the transmission path can cause the signal to distort, which over time, will cause the eye to “close”. Specifications, such as an eyemask template, can be placed on the amount of open area required in the eye to ensure a functional system.

An eyemask template is a representation of the receiver’s sensitivity and is often used as a metric of performance. While there are lot-to-lot and vendor-to-vendor variations in receiver sensitivity, some general guidelines can be developed. After reviewing several major industry standards (PCIe, Gigabit Ethernet), we find similar eyemask requirements and we will use these as the basis for a generic template in this report. For this report, we will assume a receiver amplitude sensitivity of 50 mVpp and a jitter margin of 0.5 UI. This results in a diamond shape eyemask template that is 50 mV high and 0.5 UI wide.

Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system’s signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time and crosstalk in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in [Appendix C](#) of this report.

The measured S-Parameters from the network analyzer are post-processed using Agilent Advanced Design System to obtain the time domain response for signal propaga-

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable
tion time and crosstalk. The Time Domain procedure is provided in [Appendix F](#) of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 10 mils of PCB trace on each connector side. Delay is measured at 30 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: PCIEC-85

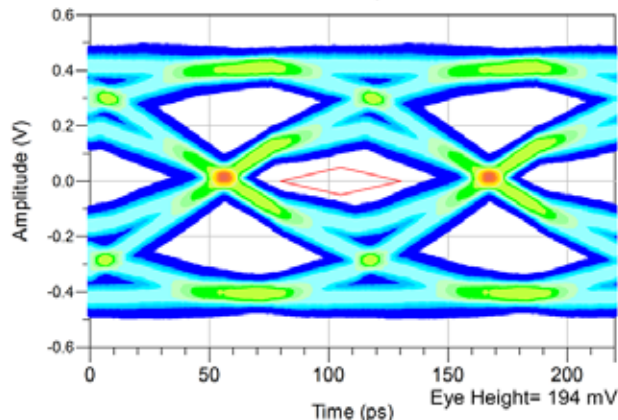
Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix A – Eye Diagrams

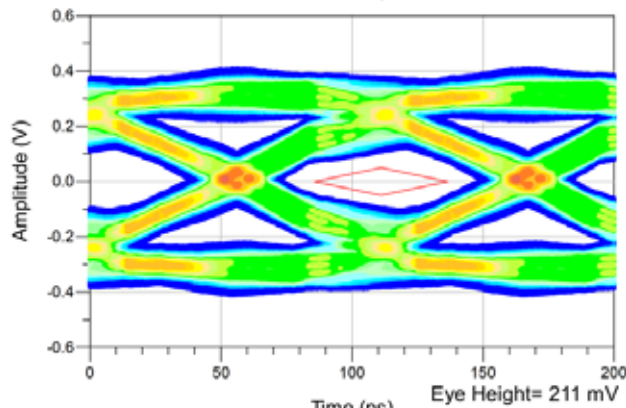
PCIEC-064-0250-EC-EM-P-85

9Gbps: Long Row

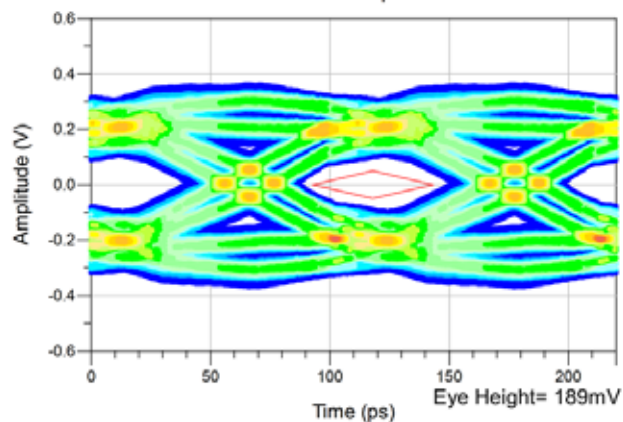
No De-Emphasis



3dB De-Emphasis



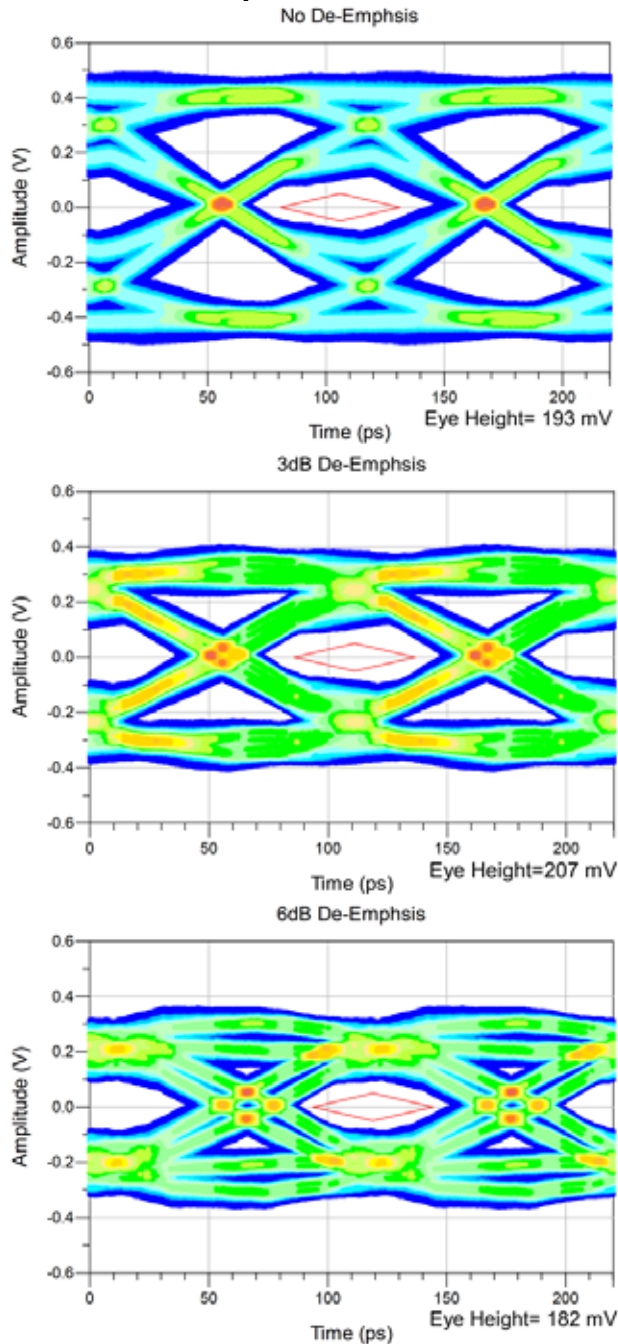
6dB De-Emphasis



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

9Gbps: Short Row

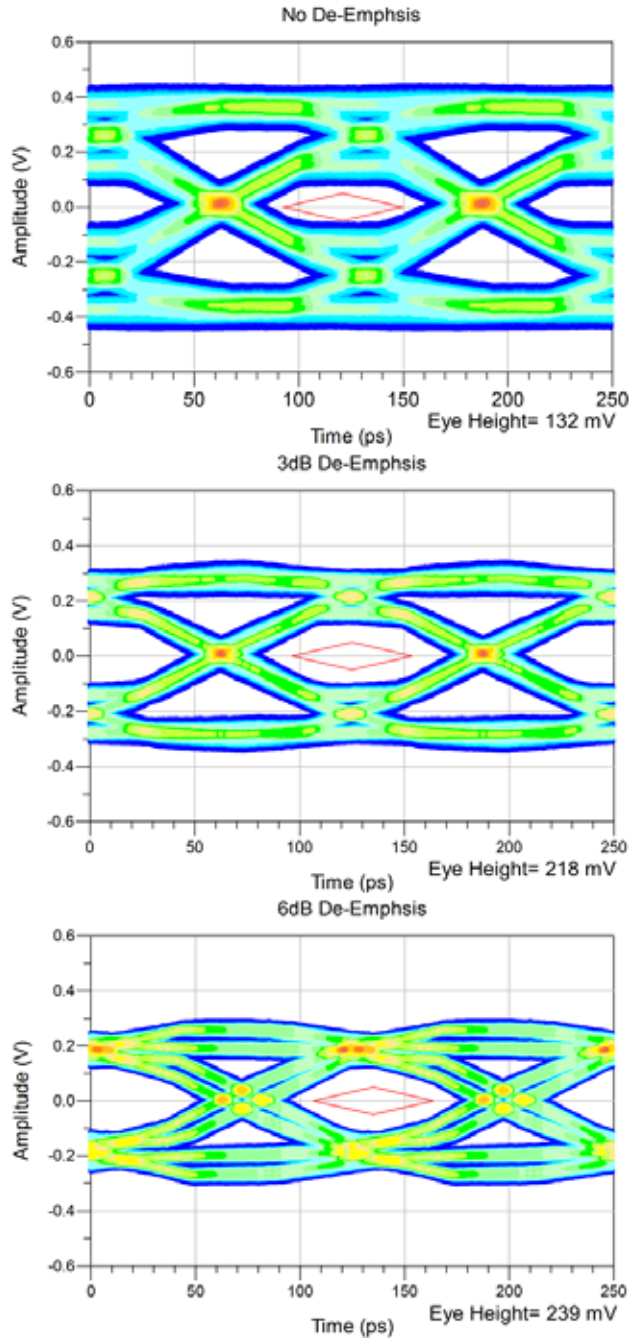


Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

PCIEC-064-1000-EC-EM-P-85

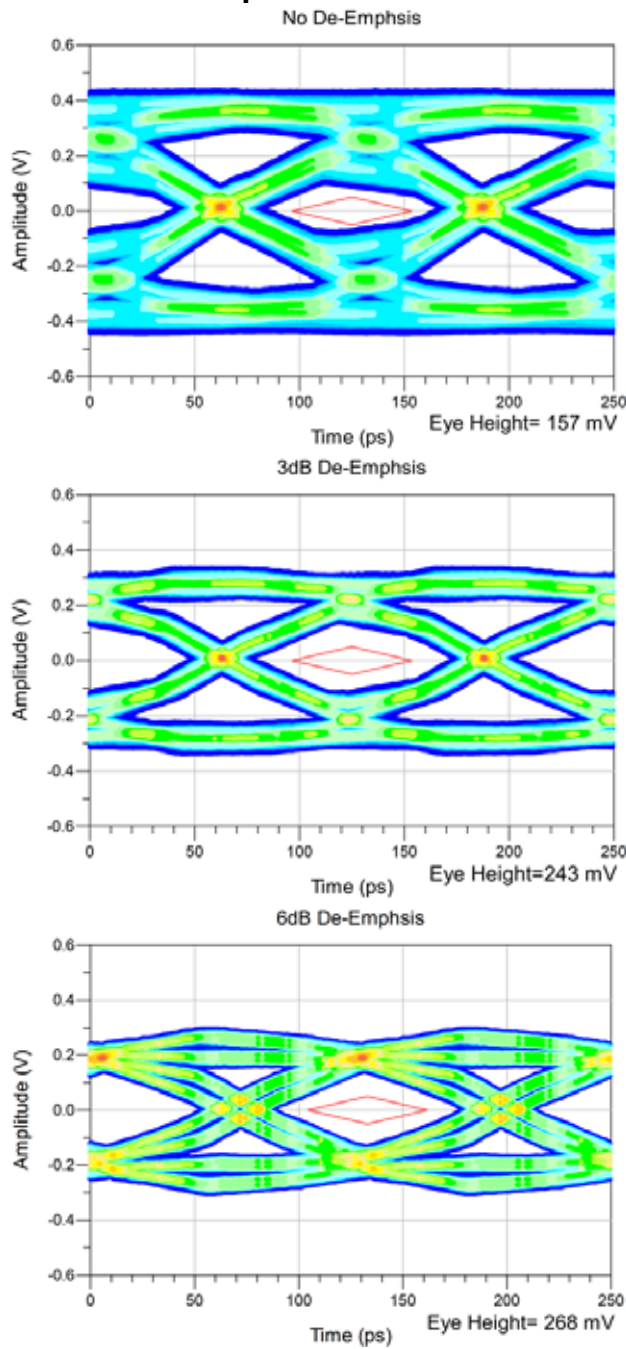
8Gbps: Long Row



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

8Gbps: Short Row

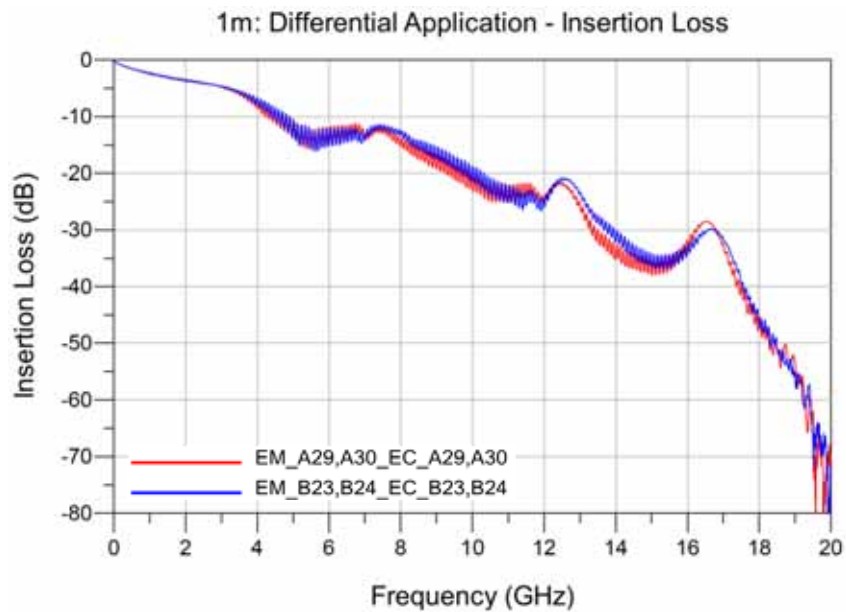
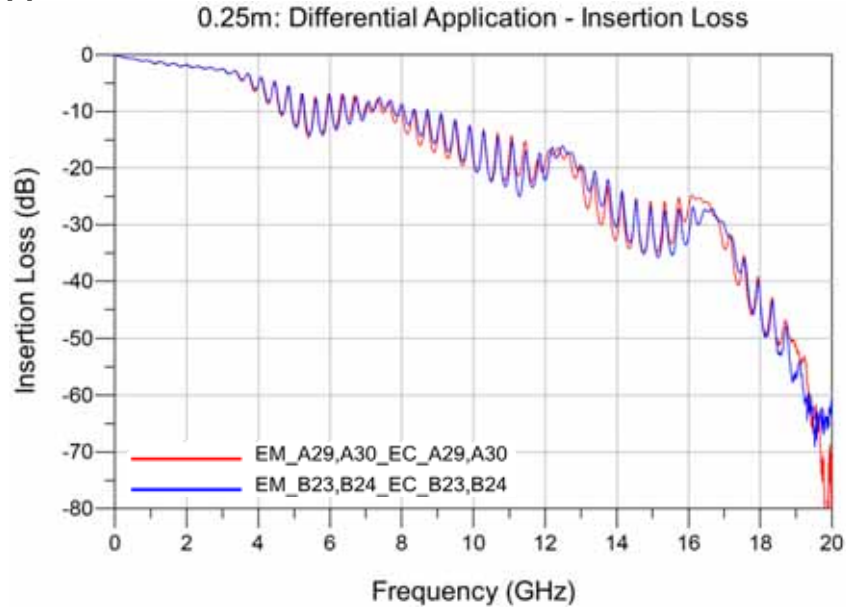


Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix B – Frequency Domain Response Graphs

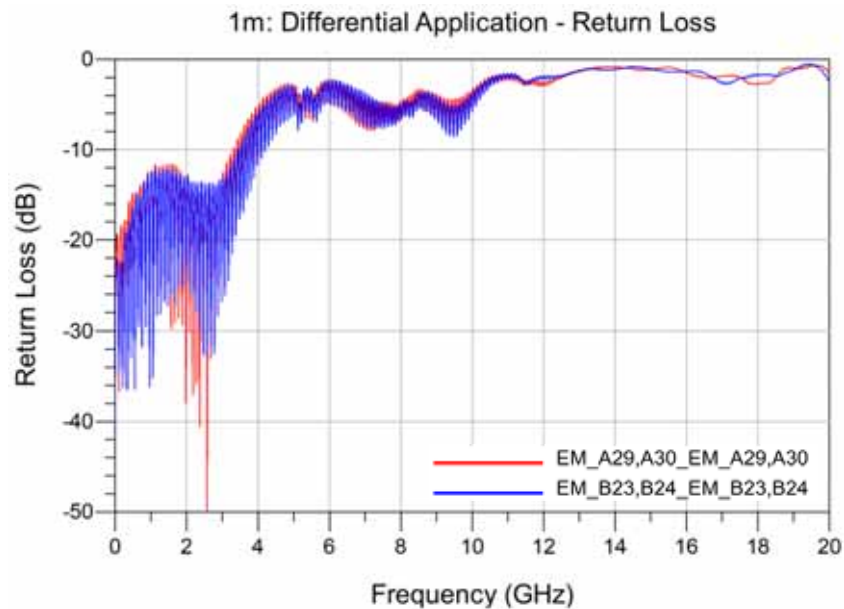
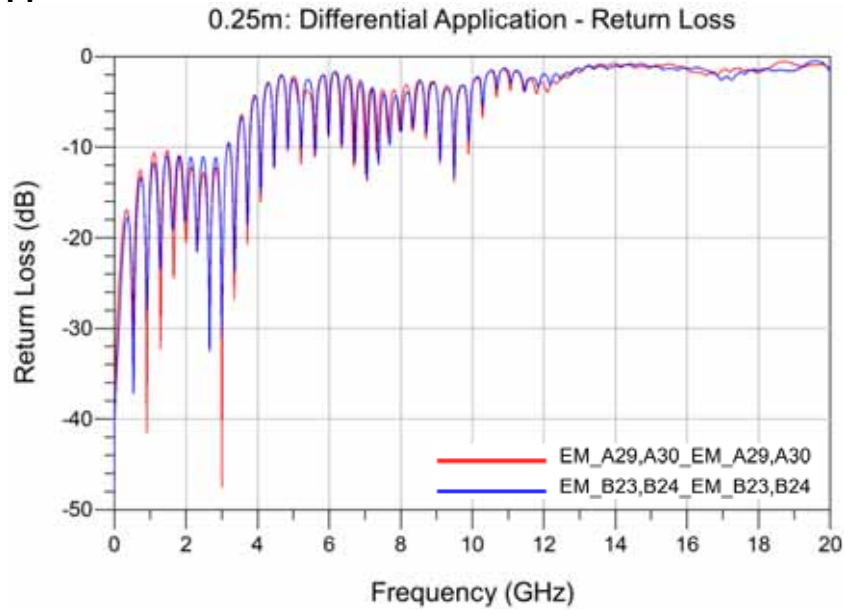
Differential Application – Insertion Loss



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Differential Application – Return Loss

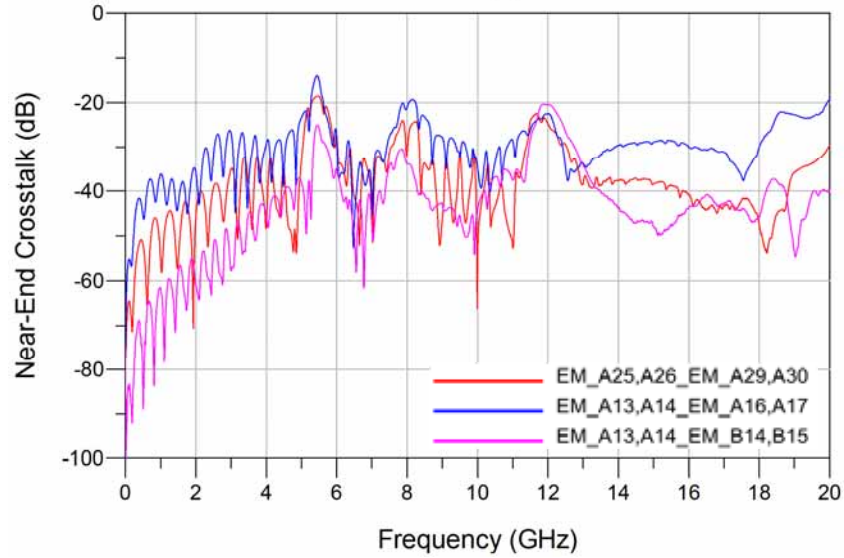


Series: PCIEC-85

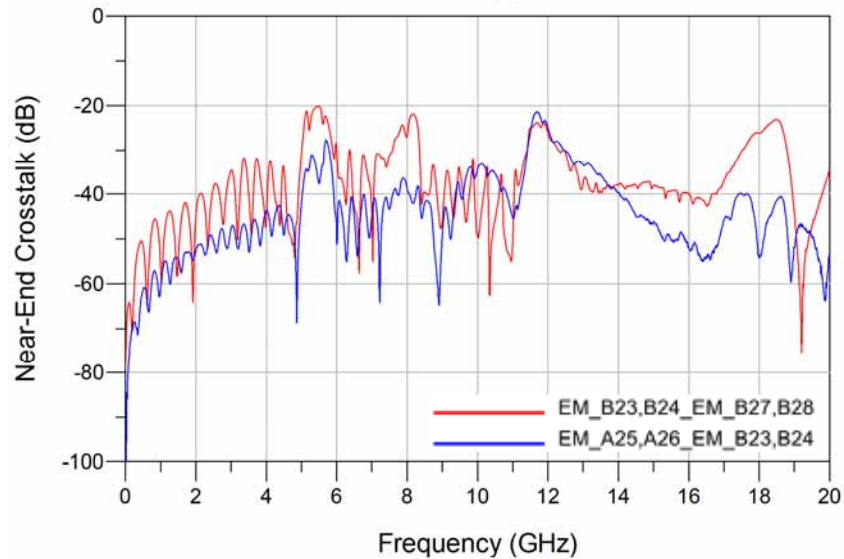
Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Differential Application – NEXT Configurations

0.25m: Differential Application - NEXT



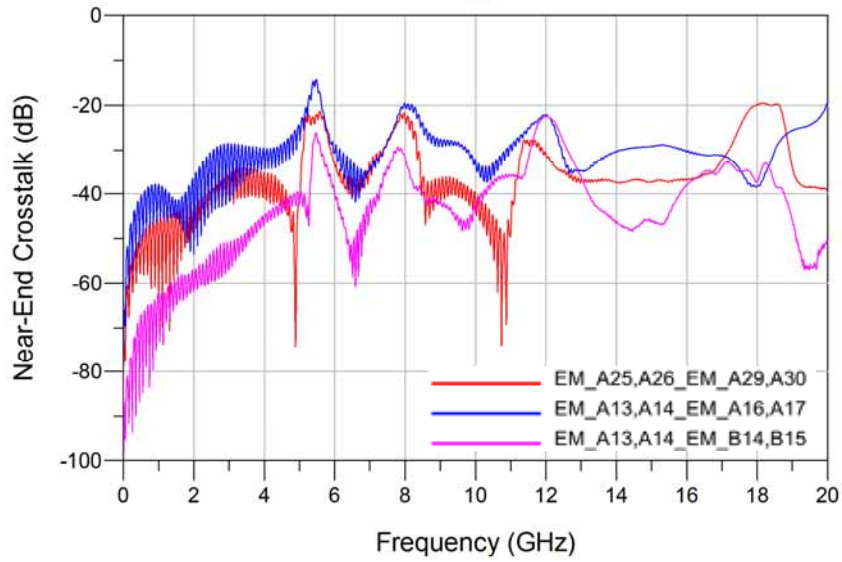
0.25m: Differential Application - NEXT



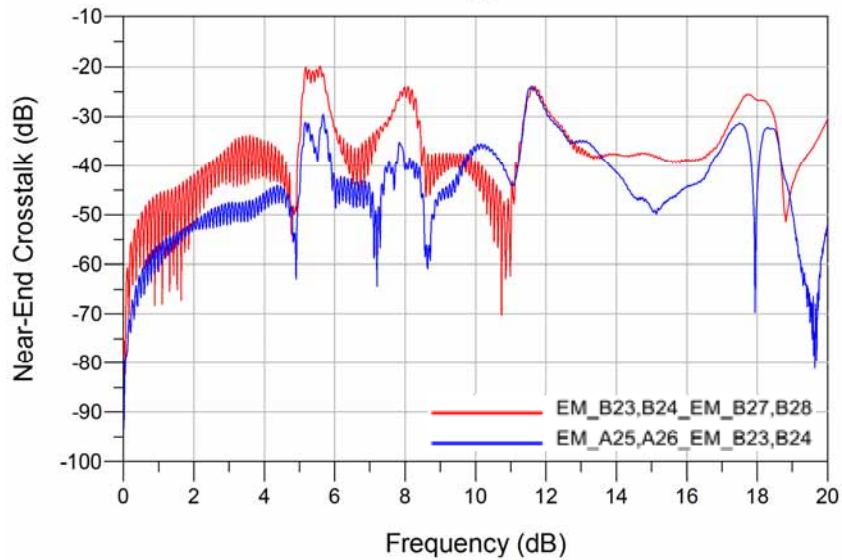
Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

1m: Differential Application - NEXT



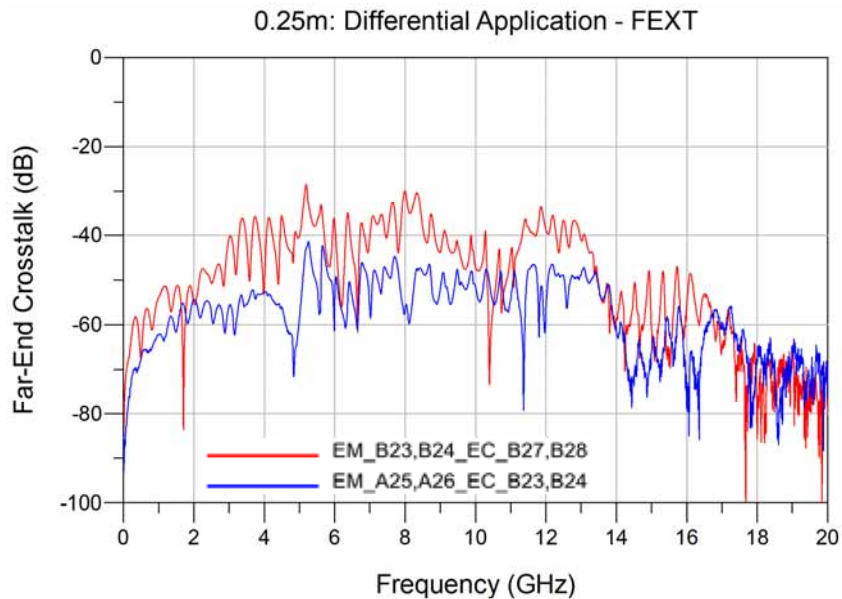
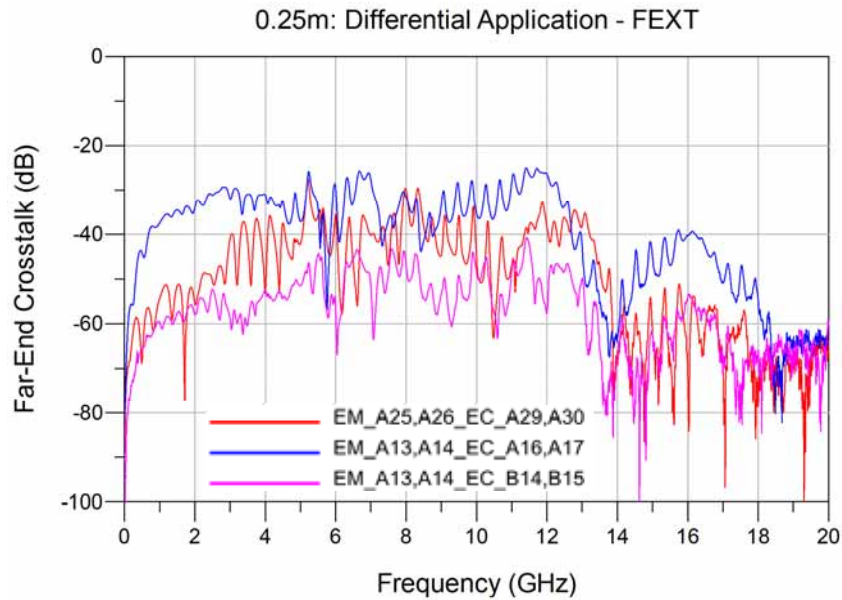
1m: Differential Application - NEXT



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

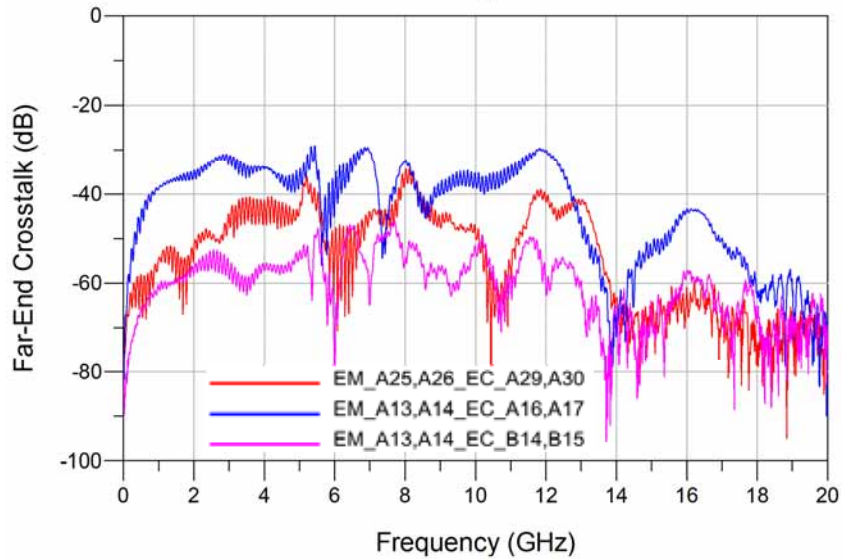
Differential Application – FEXT Configurations



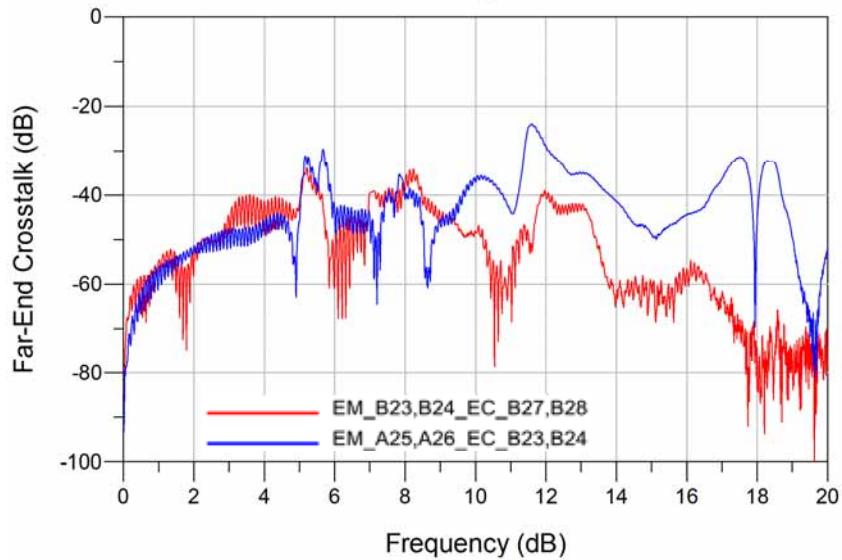
Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

1m: Differential Application - FEXT



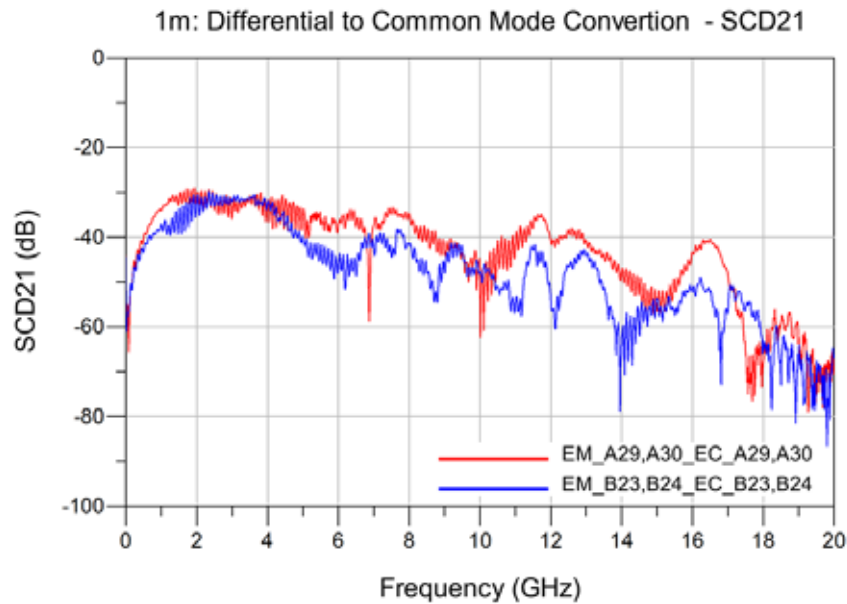
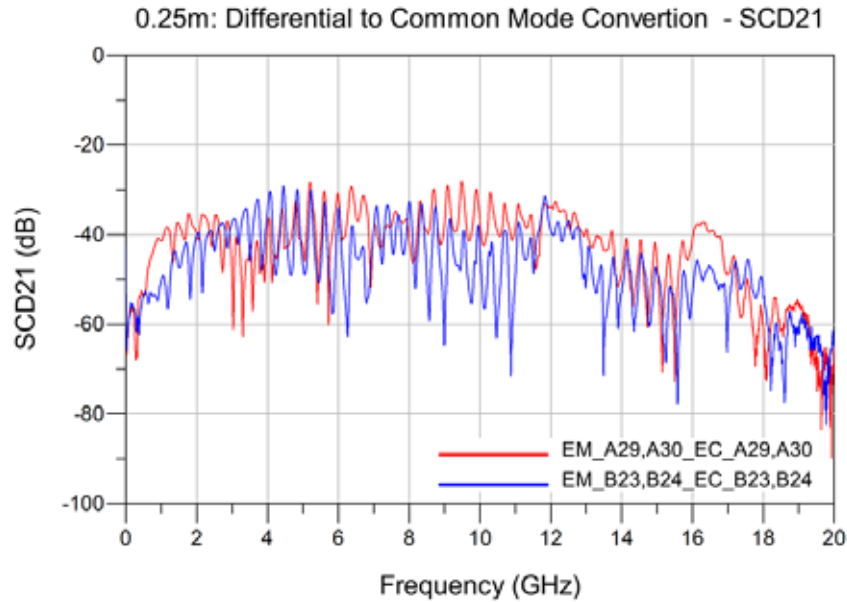
1m: Differential Application - FEXT



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Differential Application – Differential to Common Mode Conversion

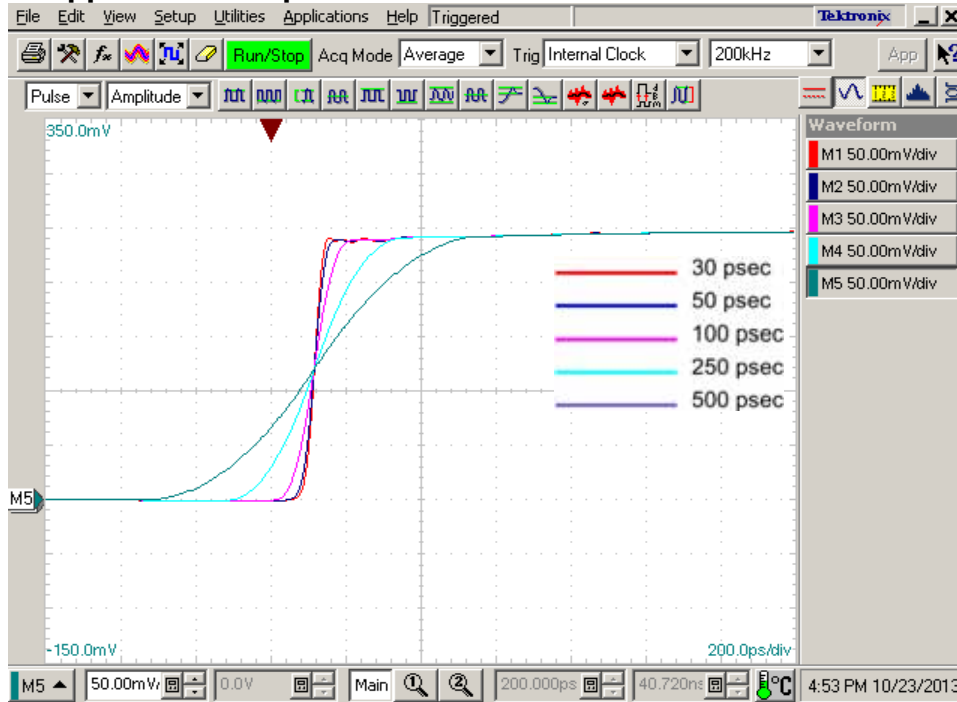


Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix C – Time Domain Response Graphs

Differential Application – Input Pulse

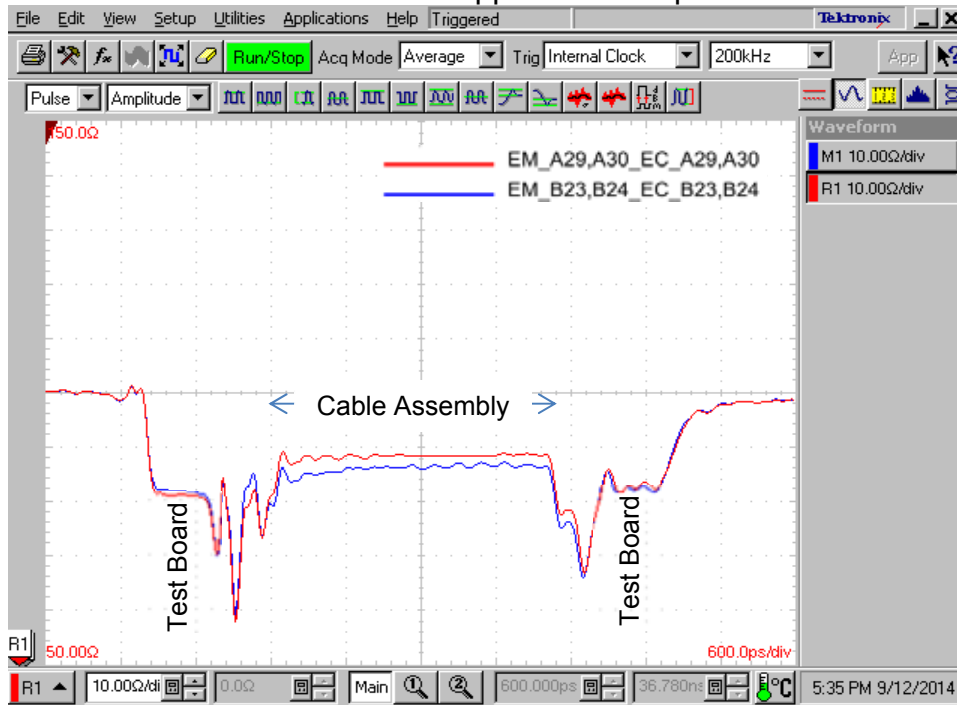


Series: PCIEC-85

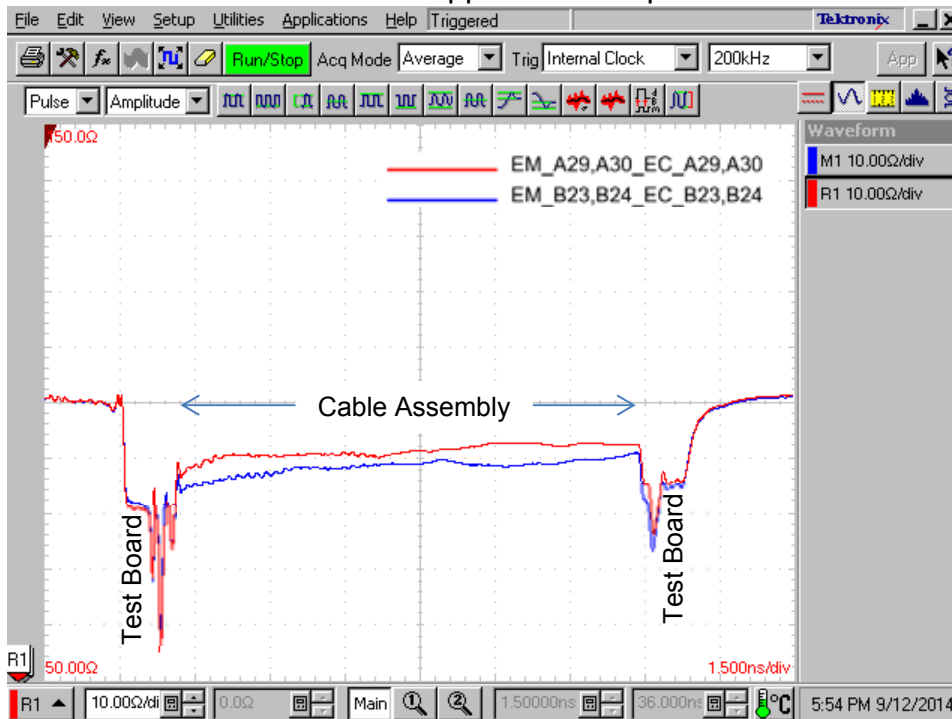
Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Differential Application – Cable Assembly Impedance

0.25m: Differential Application - Impedance



1m: Differential Application - Impedance

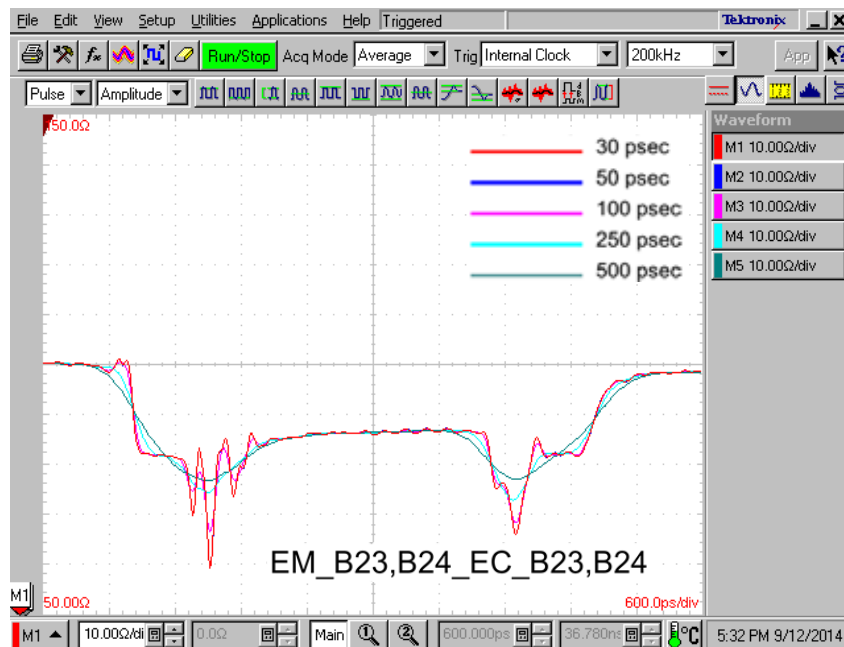
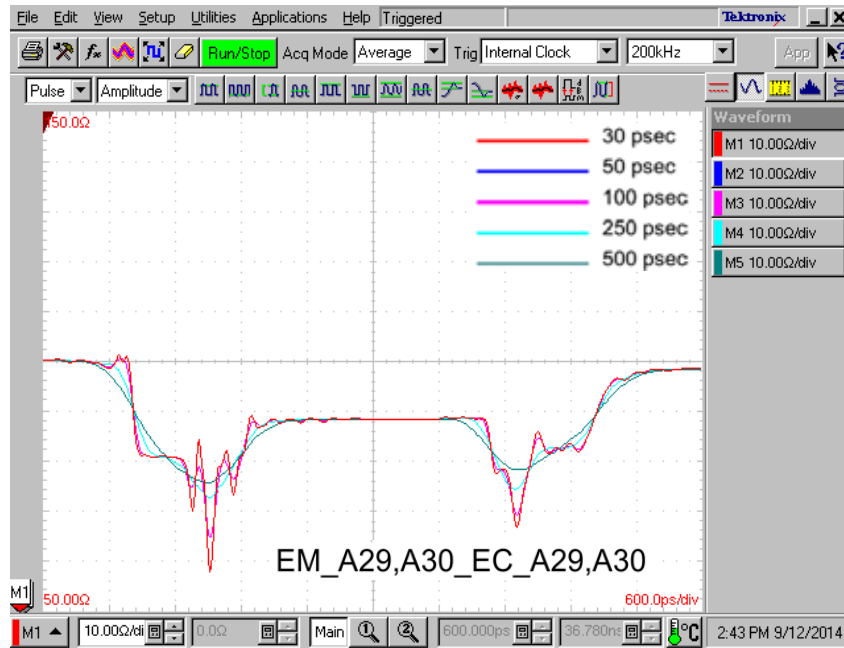


Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Differential Application – Cable assembly Impedance

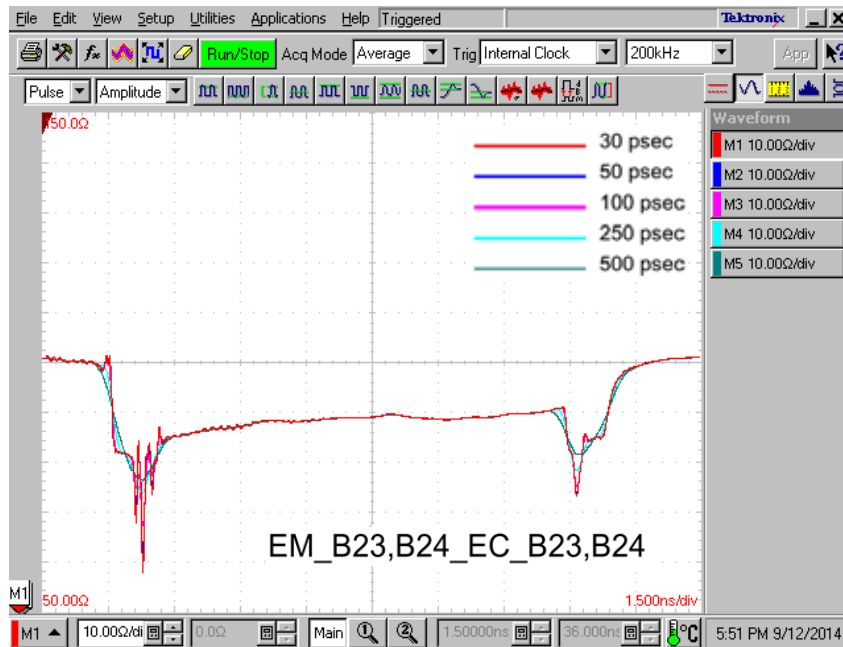
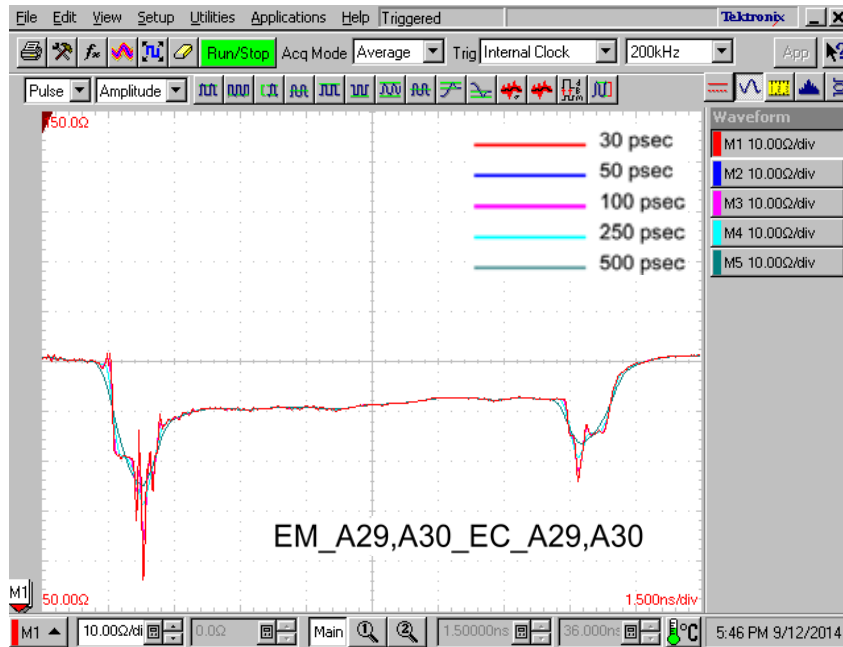
PCIEC-064-0250-EC-EM-P



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

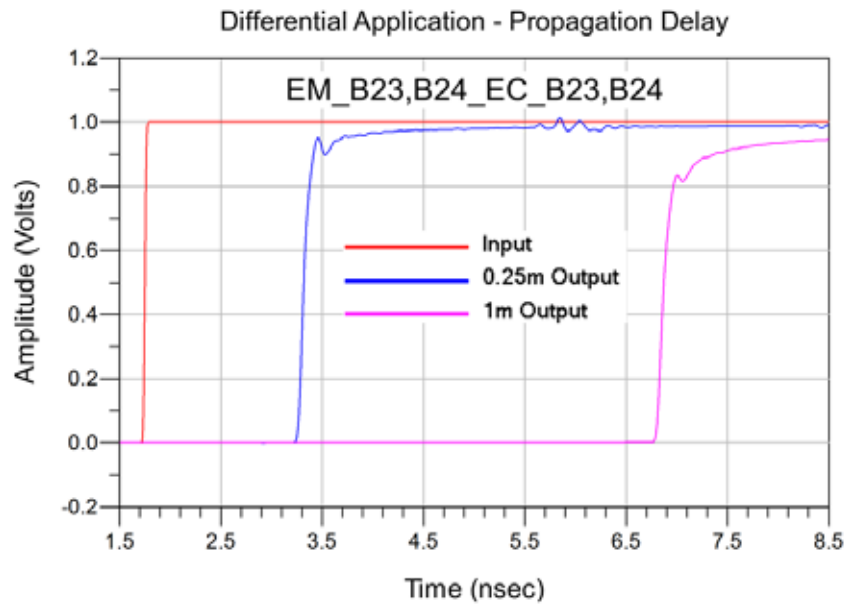
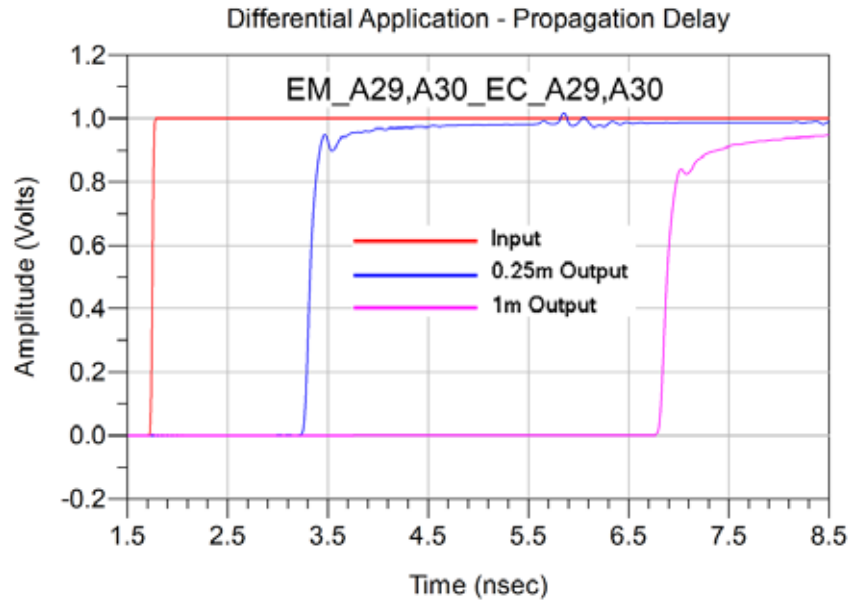
PCIEC-064-1000-EC-EM-P



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Differential Application – Propagation Delay



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix D – Product and Test System Descriptions

Product Description

Product test samples are 1.00mm PCI Express® Internal Cable Assemblies. The part numbers are PCIEC-064-0250-EC-EM-P-85 and PCIEC-064-1000-EC-EM-P-85. They mate with PCIE-064-02-F-D-TH and the 85 ohm edge card test board. A photo of the mated test article mounted to SI test boards is shown below.

The cable assembly terminations had a particular signal line configuration. The respective signal line numbers are shown in Table 5. There are a total of 32 positions per row but all are not shown. Positions 1 – 11 terminate to the PVC power cable. All Side B pairs are Transmitter pairs. All Side A pairs are Receiver pairs except for pair A13-A14, which is the Reference Clock Pair. SMA jack numbers on the test boards correspond to the assembly line numbers. All adjacent lines are terminated where applicable.

Side A	G	13	14	G	16	17	G	19	G	21	22	G	G	25	26	G	G	29	30	G	32
Side B	12	G	14	15	G	17	G	19	20	G	G	23	24	G	G	27	28	G	30	31	G

Table 5: Respective signal line numbers as viewed from End 1

Test System Description

The test fixtures are composed of four-layer FR-4 material with 42.5Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Four test fixtures are specific to PCIEC-85 series cable assembly and identified by part numbers PCB-106420-SIG-03A and B to PCB-106420-SIG-04A and B. The Auto Fixture Removal (AFR) calibration structures designed specifically for the PCIEC series are located on the calibration board PCB-106420-SIG-08. Displayed on the following pages is the information for the PCIEC and AFR calibration structure and directives for the mating PCIEC fixtures.

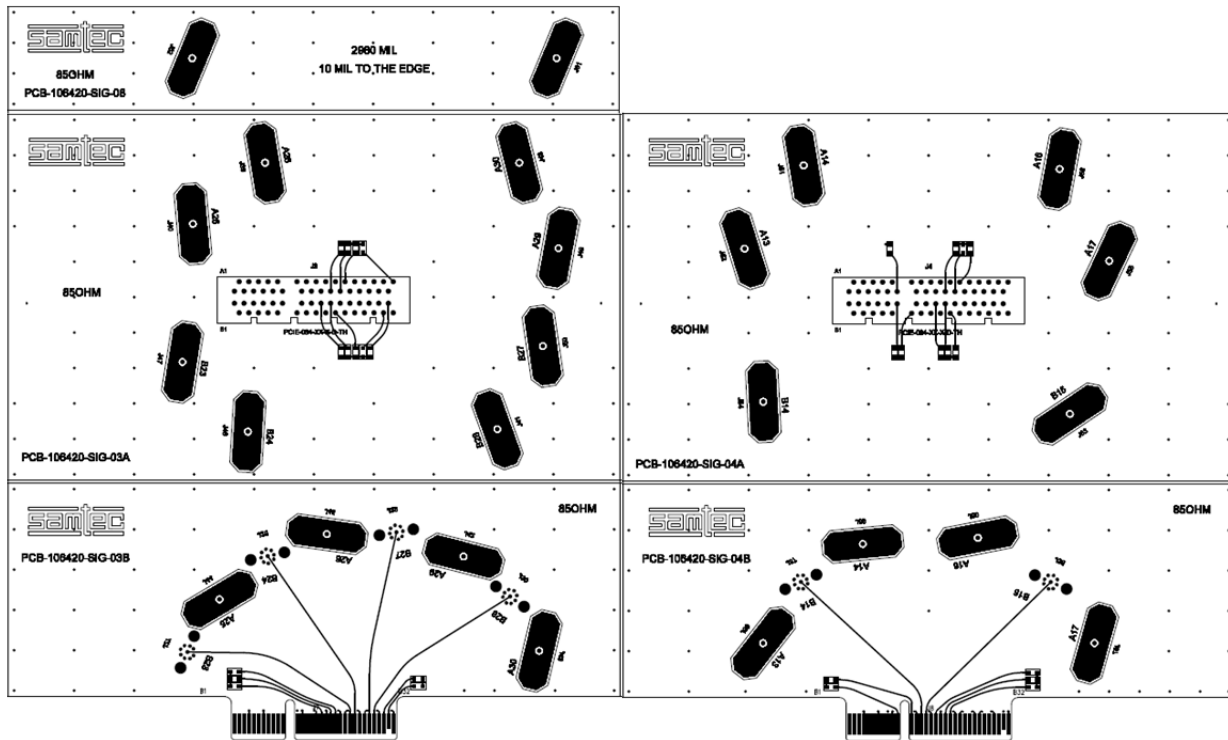
PCB-106420-SIG-XX Test Fixtures



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Artwork of the PCB design is shown below.

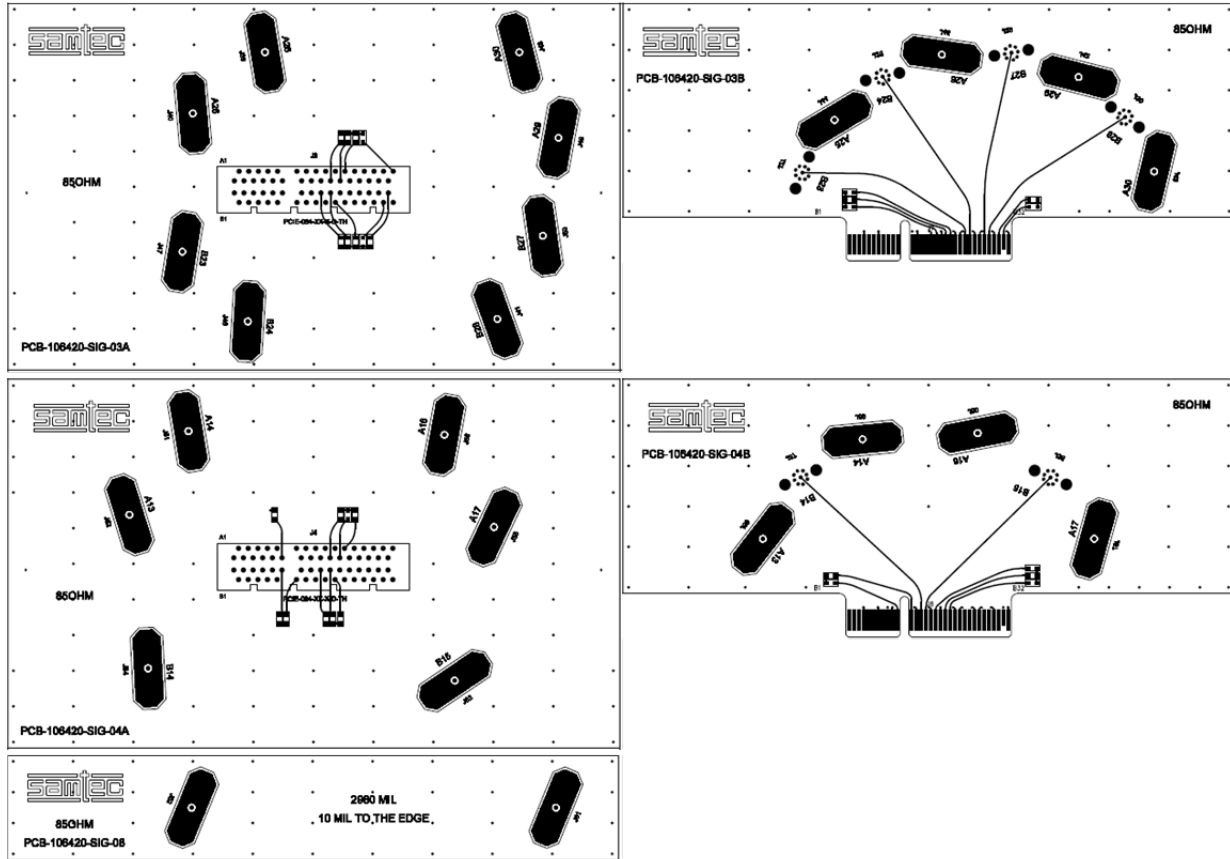


Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

PCB Fixtures

The test fixtures used are as follows:



- PCB-106420-SIG-03A – PCIEC-85 Cable Test Board 1
- PCB-106420-SIG-03B – PCIEC-85 Cable Test Board 2
- PCB-106420-SIG-04A – PCIEC-85 Cable Test Board 3
- PCB-106420-SIG-04B – PCIEC-85 Cable Test Board 4
- PCB-106420-SIG-08 – Through

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix E – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are extracted from the instrument by AFR application. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz

Number of points -1601

Stop Frequency – 20 GHz

IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

<u>QTY</u>	<u>Description</u>
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ECAL Module (300 KHz to 20 GHz)

Test Cables & Adapters

<u>QTY</u>	<u>Description</u>
4	Gore OWD01D02039-4 (DC-26.5 GHz)

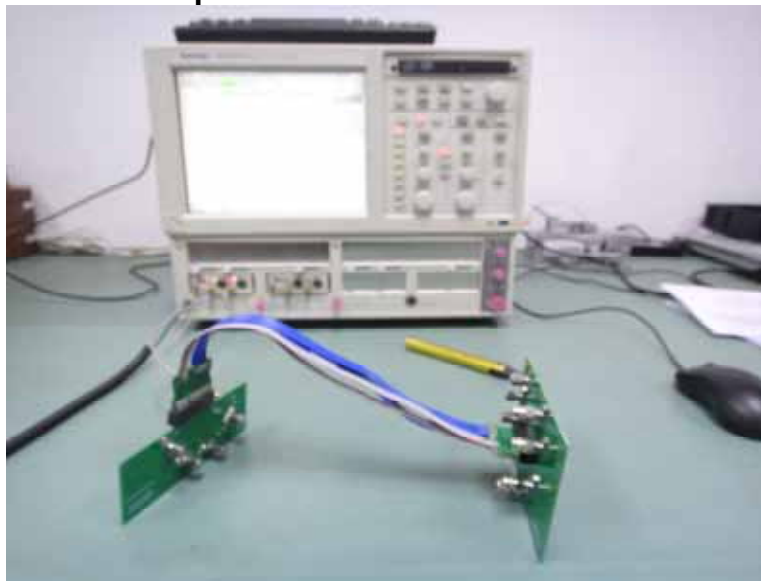
Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

Vertical Scale: 10 ohm / Div:
Offset: Default / Scroll
Horizontal Scale: 500ps/ Div or 1.5ns/ Div
Record Length: 4000
Averages: ≥ 16

DSA8200 Measurement Setup



Test Instruments

<u>QTY</u>	<u>Description</u>
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

<u>QTY</u>	<u>Description</u>
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix F - Frequency and Time Domain Measurements

Eye Diagram Procedures

Eye Diagrams and statistical eye diagram metrics such as eye height can be generated by post-processing Frequency Domain measurements using Agilent ADS. Simulated data is sent over a touchstone model and the bits are overlain into an eye pattern.

Currently, no CEI specification is available for 7Gbps, so *CEI-28-VSR Working Clause Proposal, CEI Implementation agreement Draft 7.0*, dated May 14, 2012 was used for this report.

The simulation circuit is modeled as:

Agilent's Advanced Design System Tx and Rx modules that are configured to the *CEI-28-VSR Working Clause Proposal, CEI Implementation agreement Draft 7.0*, dated May 14, 2012.

- Tx parameters are specified in Section 1.3.3, *Module-to-Host Specifications*, Table 1-4, Page 7.
- Rx parameters defined in Section 1.3.2 *Host-to-Module Electrical Specifications*, Table 1-1, Page 5.
- A 1.0 inch length of Tx interconnect trace segment at the transmitter.
- SUT Cable Assembly S-Parameter measurements
 - 10 mils of 10.2 mil wide differential microstrip signal trace
 - Test board vias, pads (footprint effects) for the PCIE connector
 - The PCIE series connector
 - The PCIE-85 cable assembly
 - The Edge Card
 - Test board vias, pads (footprint effects) for the edge card
 - 10 mils of 10.2 mil wide differential microstrip signal trace
- A 1.0 inch length of Rx interconnect trace segment at the receiver.

All traces were modeled as microstrip on FR4 with the following parameters:

- The FR4 parameters are modeled using:
 - $E_r = 4.2 @ 1 \text{ GHz}$
 - Loss Tangent = $0.02 @ 1 \text{ GHz}$
- Copper is modeled as:
 - Conductivity = $4.5E+7 \text{ S-m}$
 - Surface roughness = 0.6 micron
- Traces are microstrip with the following geometry:
 - 10.2 mil trace width

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

- 1.9 mil trace copper thickness
- 5.8 mil FR4 dielectric thickness

Eye Mask

The eye mask is set for 50mVpp, with a jitter margin of 0.5 UI.

Rise Time

The 10-90 risetime of the 9Gbps signal was determined to be 78psec, using the following formula:

$$\text{Risetime} = 0.35/\text{Bandwidth}$$

Series: PCIEC-85

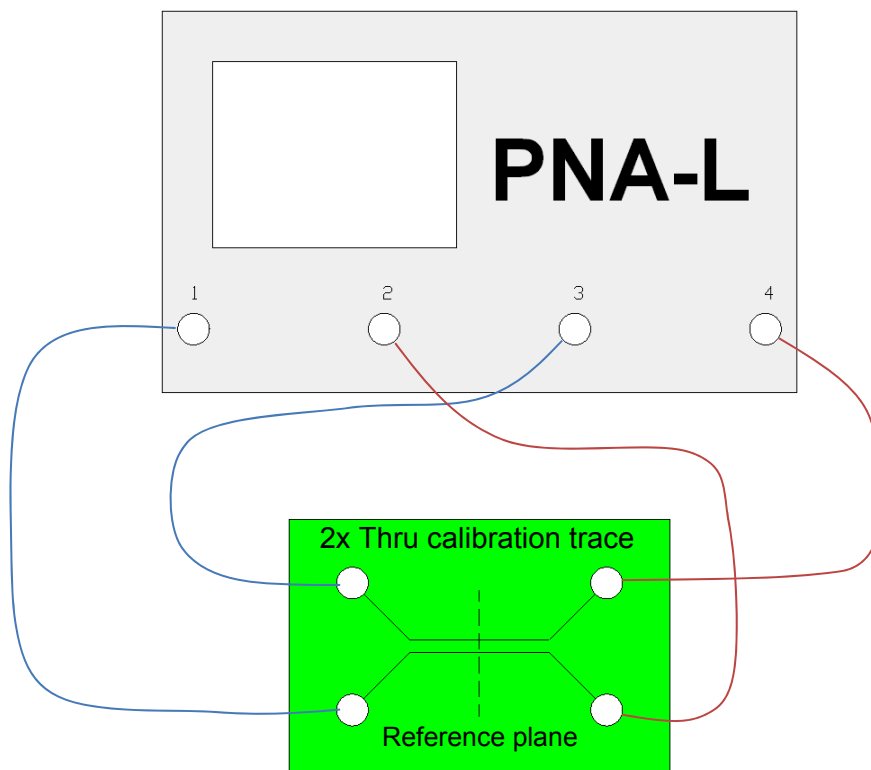
Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-CAL module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the PCIEC test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.



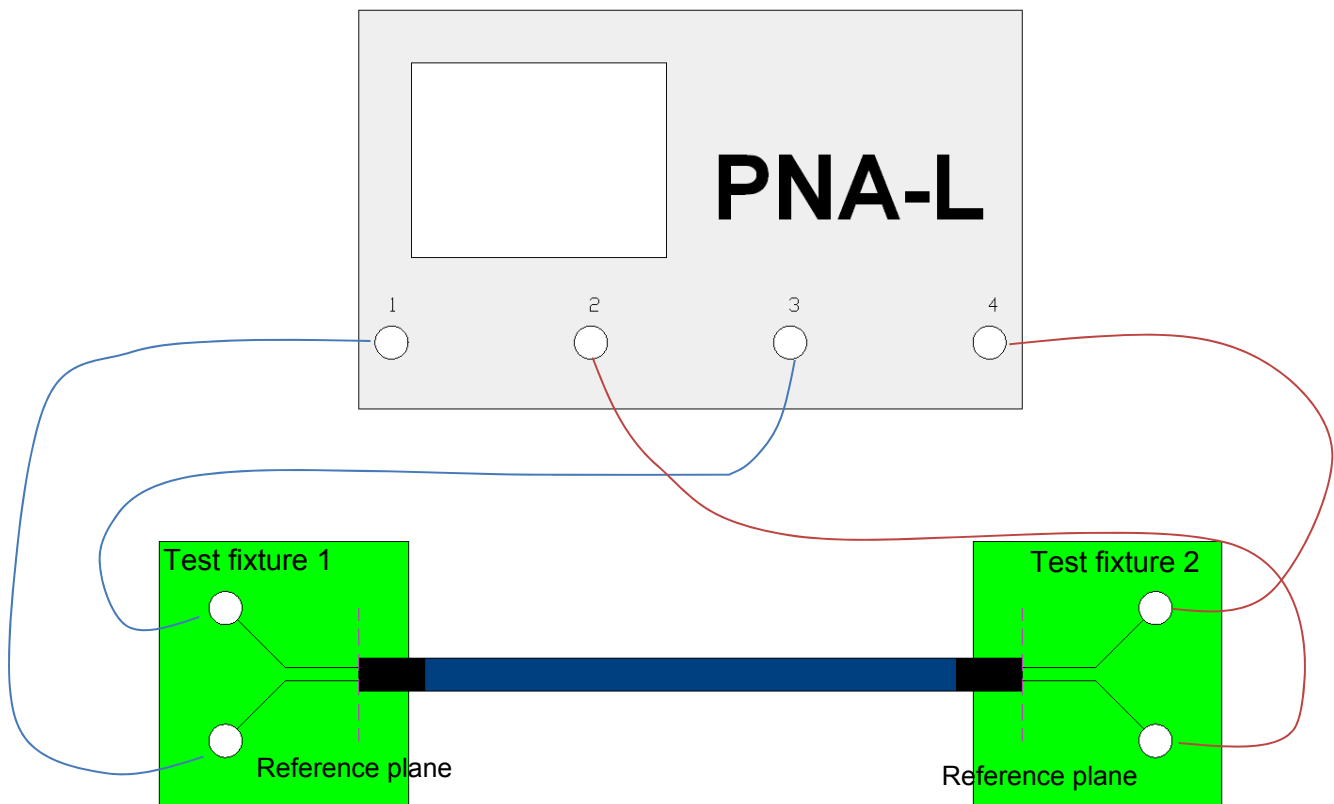
Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Measurements are then performed using the test boards as shown below. The test board effects are removed in post-processing via AFR in Agilent PLTS. The calibrated reference plane is located 10 mils from the connector footprint on each side. The S-Parameter measurements include:

- A. 10 mils of 10.2 mil wide differential microstrip signal trace
- B. Test board vias, pads (footprint effects) for the PCIE connector
- C. The PCIE series connector
- D. The PCIEC-85 test cable
- E. The Edge Card
- F. Test board vias, pads (footprint effects) for the edge card
- G. 10 mils of 10.2 mil wide differential microstrip signal trace

The figure below shows the location of the measurement reference plane.



Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.

http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Impedance (TDR)

Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

Series: PCIEC-85

Description: PCI Express® Internal Cable Assembly, 32 AWG 85ohm Twinax Ribbon Cable

Appendix G – Glossary of Terms

ADS – Agilent Advanced Design System

AFR – Automatic Fixture Removal

CTLE – Continuous Time Linear Analyzer

CuFireFly™ - Copper FireFly™ assembly

DUT – Device under test

FD – Frequency domain

FEXT – Far-End Crosstalk

HDV – High Density Vertical

NEXT – Near-End Crosstalk

OV – Optimal Vertical

OH – Optimal Horizontal

PCB – Printed Circuit Board

PLTS – Agilent Physical Layer Design System

PPO – Pin Population Option

SE – Single-Ended

SI – Signal Integrity

SUT – System Under Test

S – Static (independent of PCB ground)

SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards

TD – Time Domain

TDA – Time Domain Analysis

TDR – Time Domain Reflectometry

TDT – Time Domain Transmission

UI – Unit Interval

XROW – Across Row

Z – Impedance (expressed in ohms)