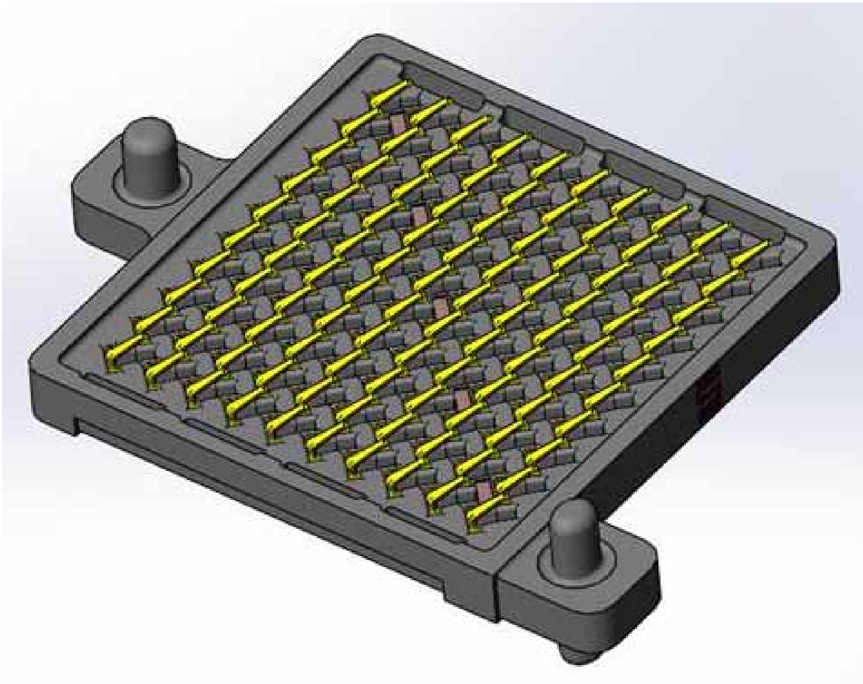
High Speed Characterization Report

GMI-XX-2-1.27-X-10



Description:
Low Profile One Piece Array,
1.0mm x 1.0mm Pitch, 1.27mm Stack Height

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Report Revision: 9/11/2015

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

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Connector Overview

GMI is a low profile, 1.0mm x 1.0mm (.0394" x .0394") pitch one-piece interconnect system for high-speed board-to-board applications. The GMI is ideal for board stacking, module-to-board and LGA interfaces. It has been designed for up to 400 I/Os. This report reflects the hi-speed electrical characteristics specific to a mated 1.27mm stack height.

Connector System Speed Rating

GMI Series, 1.0mm x 1.0mm pitch interconnect, 1.27mm Stack Height.

Signaling	Speed Rating
Single-Ended: 1:1 S/G	**20 GHz/ 40Gbps**
Single-Ended: 2:1 S/G	**12 GHz/ 24Gbps**
Differential: Optimal Horizontal	**20 GHz/ 40Gbps**
Differential: Optimal Vertical	**20 GHz/ 40Gbps**
Differential: High Density Vertical	**16.5 GHz/ 33Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board's trace loss, since a short length of trace loss is included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

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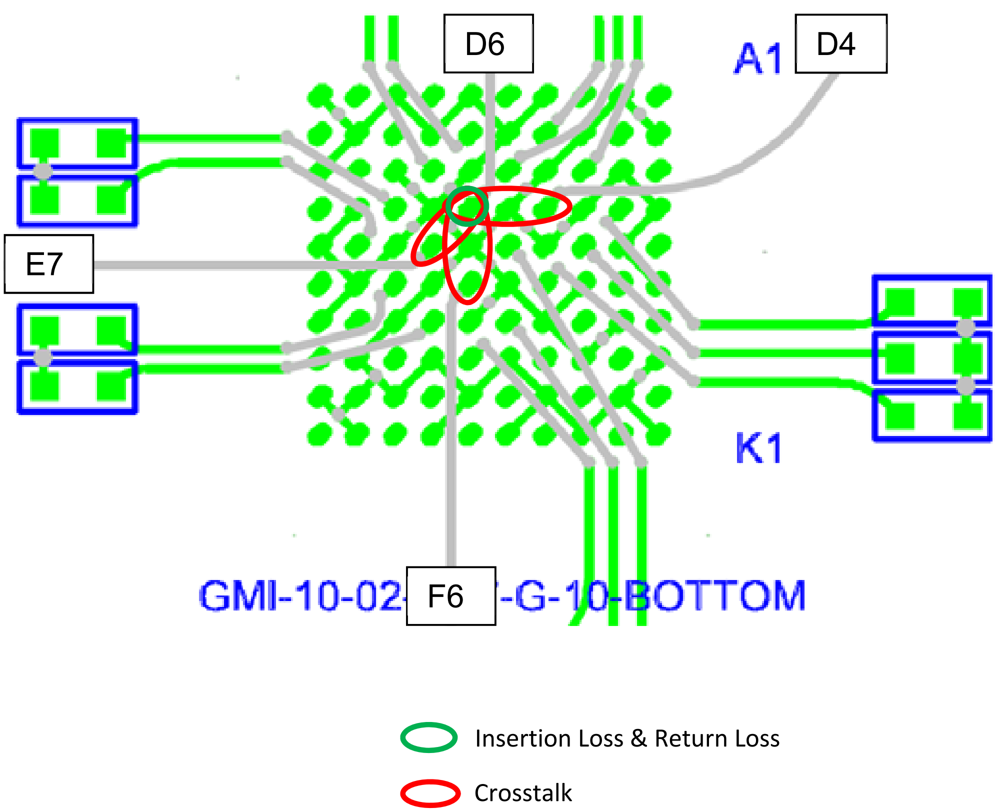
Frequency Domain Data Summary

Table 1 - Single-Ended 1:1 S/G Pattern Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	AD6	BD6	<-3dB to 20 GHz
Return Loss	AD6	AD6	>10dB to 20 GHz
Near-End Crosstalk	AD6	AD4	<-20dB to 20 GHz
	AD6	AF6	<-20dB to 20 GHz
	AD6	AE7	<-20dB to 20 GHz
Far-End Crosstalk	AD6	BD4	<-20dB to 20 GHz
	AD6	BF6	<-20dB to 20 GHz
	AD6	BE7	<-20dB to 20 GHz

Single-Ended 1:1 S/G Pattern Pin Map



Series: GMI
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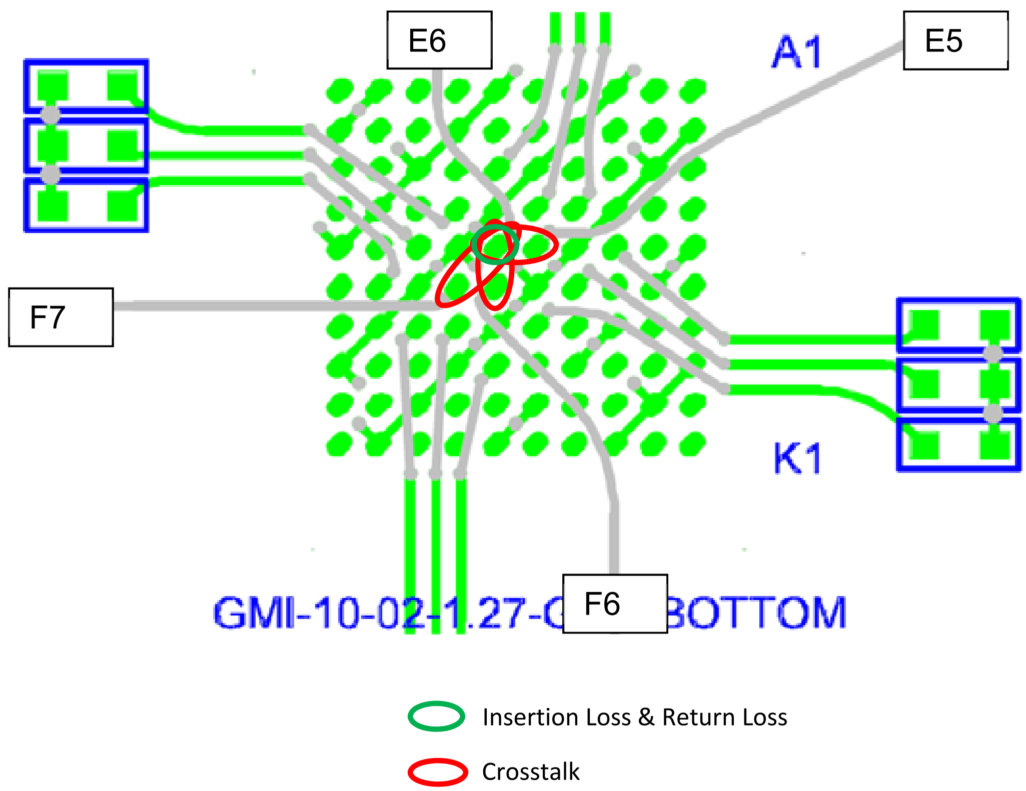
Table 2 - Single-Ended 2:1 S/G Pattern Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	AE6	BE6	-3dB @ 11.64 GHz
Return Loss	AE6	AE6	>10dB to 20 GHz
Near-End Crosstalk	AE6	AE5	<-20dB to 2.64 GHz
	AE6	AF6	<-20dB to 8.15 GHz
	AE6	AF7	<-20dB to 10.58 GHz
Far-End Crosstalk	AE6	BE5	<-20dB to 7.41 GHz
	AE6	BF6	<-20dB to 20 GHz
	AE6	BF7	<-20dB to 11.28 GHz

Single-Ended 2:1 S/G Pattern Pin Map



Series: GMI
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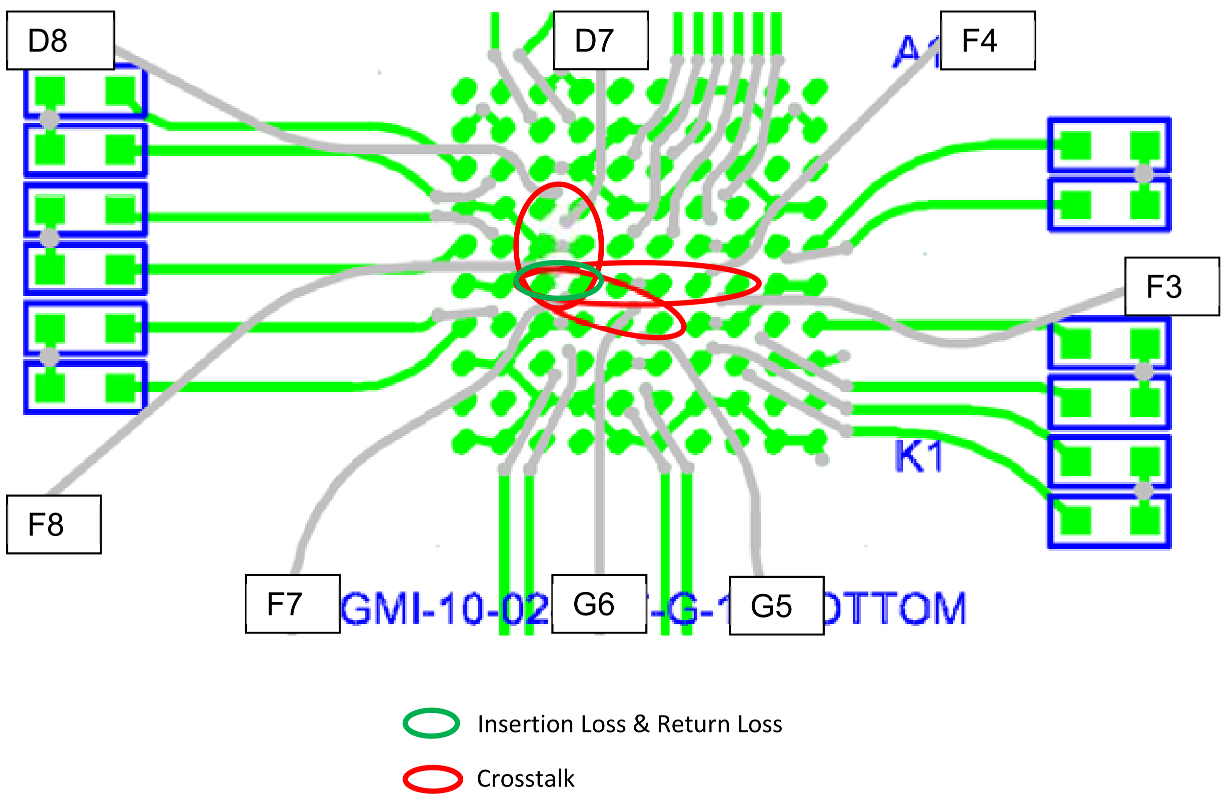
Table 3 - Differential Optimal Horizontal Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	AF7,AF8	BF7,BF8	-3dB @ 20 GHz
Return Loss	AF7,AF8	AF7,AF8	>10dB to 20 GHz
Near-End Crosstalk	AF7,AF8	AF3,AF4	<-20dB to 20 GHz
	AF7,AF8	AD7,AD8	<-20dB to 20 GHz
	AF7,AF8	AG5,AG6	<-20dB to 20 GHz
Far-End Crosstalk	AF7,AF8	BF3,BF4	<-20dB to 20 GHz
	AF7,AF8	BD7,BD8	<-20dB to 20 GHz
	AF7,AF8	BG5,BG6	<-20dB to 20 GHz

Differential Optimal Horizontal Pin Map



Series: GMI
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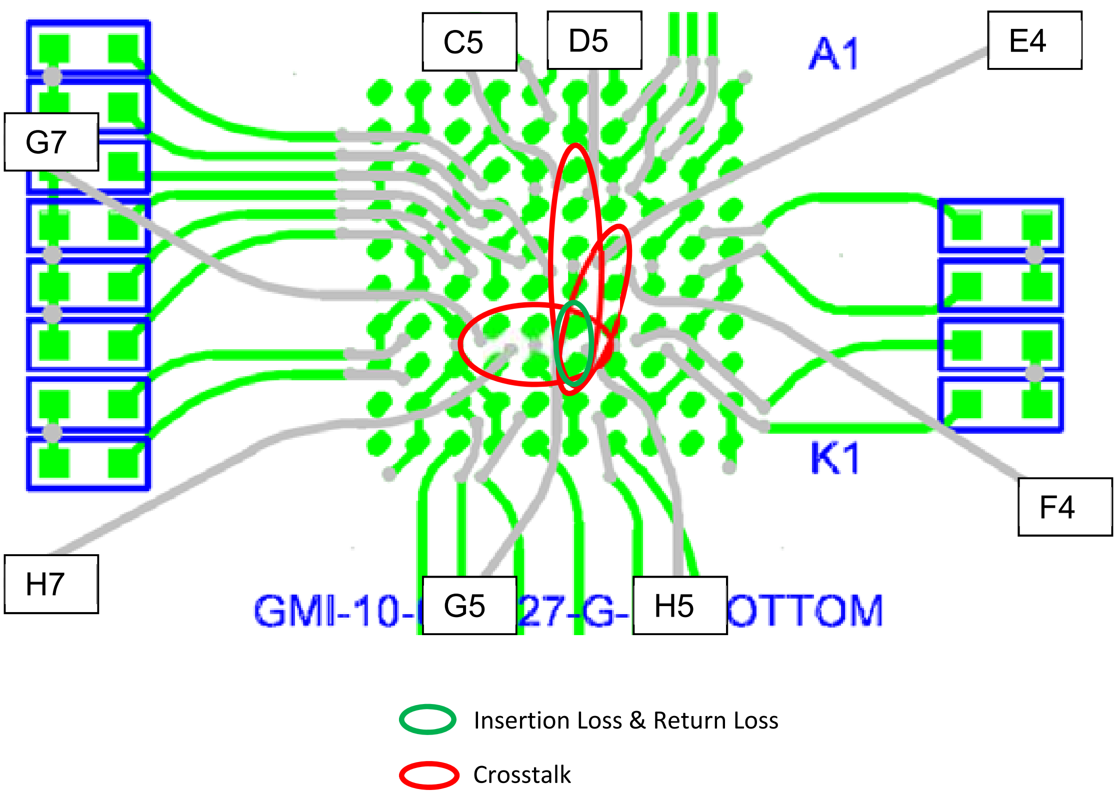
Table 4 - Differential Optimal Vertical Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	AG5,AH5	BG5,BH5	-3dB @ 20 GHz
Return Loss	AG5,AH5	AG5,AH5	>10dB to 20 GHz
Near-End Crosstalk	AG5,AH5	AG7,AH7	<-20dB to 20 GHz
	AG5,AH5	AC5,AD5	<-20dB to 20 GHz
	AG5,AH5	AE4,AF4	<-20dB to 20 GHz
Far-End Crosstalk	AG5,AH5	BG7,BH7	<-20dB to 20 GHz
	AG5,AH5	BC5,BD5	<-20dB to 20 GHz
	AG5,AH5	BE4,BF4	<-20dB to 20 GHz

Differential Optimal Vertical Pin Map



Series: GMI
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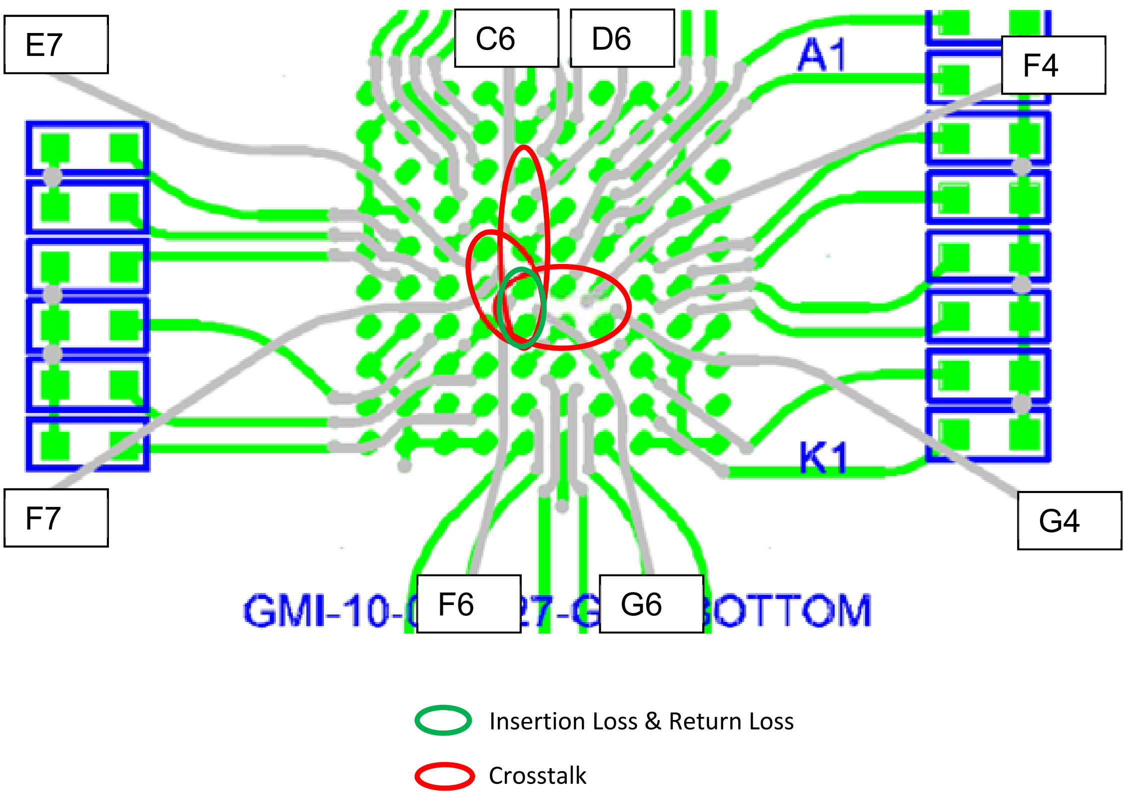
Table 5 - Differential High Density Vertical Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	AF6,AG6	BF6,BG6	-3dB @ 16.01 GHz
Return Loss	AF6,AG6	AF6,AG6	>10dB to 14.94 GHz
Near-End Crosstalk	AF6,AG6	AF4,AG4	<-20dB to 20 GHz
	AF6,AG6	AC6,AD6	<-20dB to 20 GHz
	AF6,AG6	AE7,AF7	<-20dB to 16.15 GHz
Far-End Crosstalk	AF6,AG6	BF4,BG4	<-20dB to 20 GHz
	AF6,AG6	BC6,BD6	<-20dB to 20 GHz
	AF6,AG6	BE7,BF7	<-20dB to 15.91 GHz

Differential High Density Vertical Pin Map



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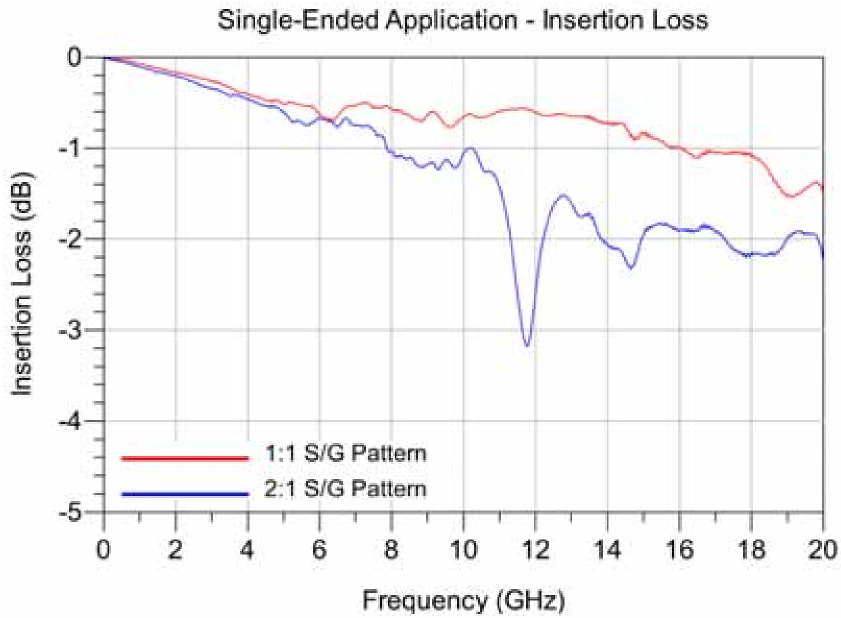
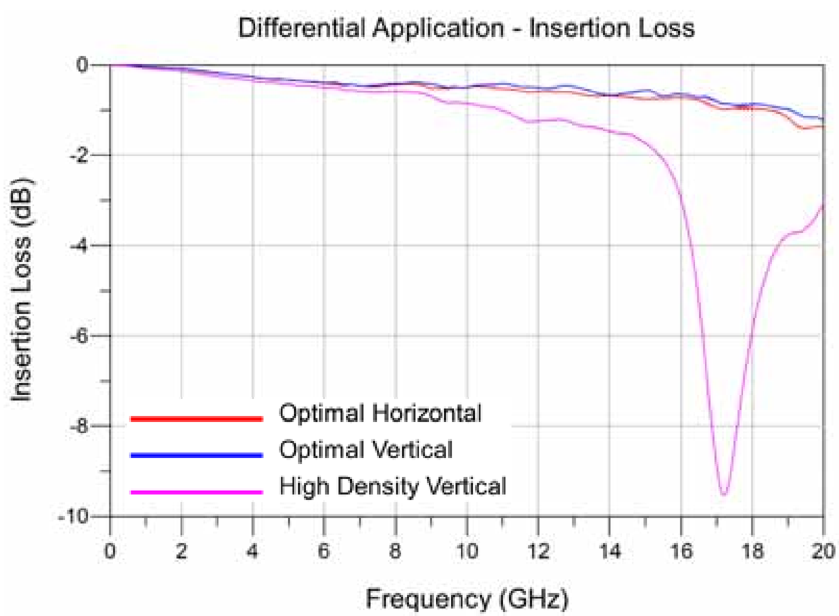
Bandwidth Charts – Single-Ended & Differential Insertion Loss

GMI Array Series





Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Time Domain Data Summary

Table 6 – Single-End Impedance (Ω) – 1:1 S/G Pattern					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	50.7	50.7	50	48.6	48.4
Minimum Impedance	45.4	45.5	45.7	46.1	47.0

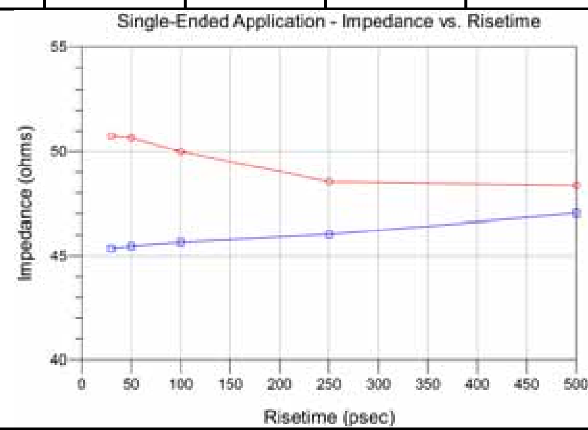
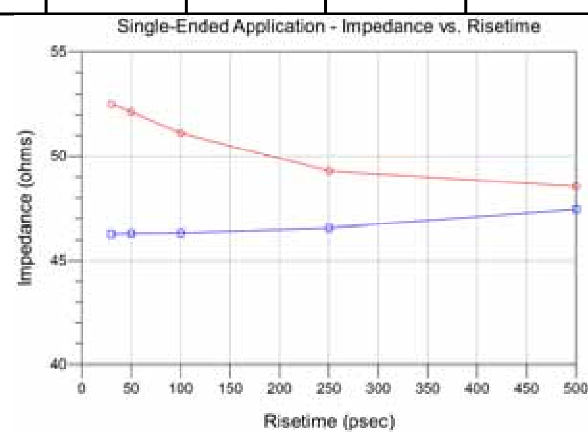


Table 7 – Single-End Impedance (Ω) – 2:1 S/G Pattern					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	52.5	52.1	51.1	49.3	48.5
Minimum Impedance	46.3	46.3	46.3	46.6	47.4



Series: GMI
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Table 8 – Differential Impedance (Ω) – Optimal Horizontal					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	100.5	99.9	99.5	99.1	98.8
Minimum Impedance	91.5	91.7	92.1	93.0	93.4

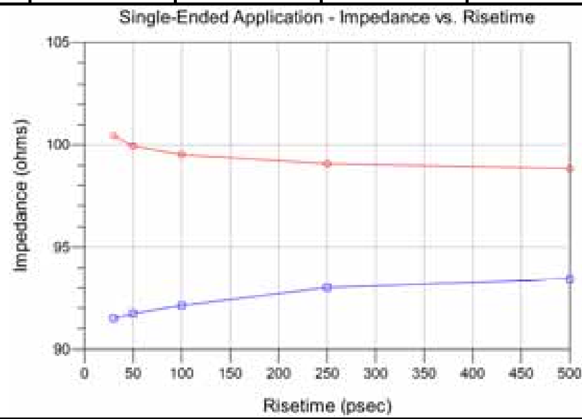
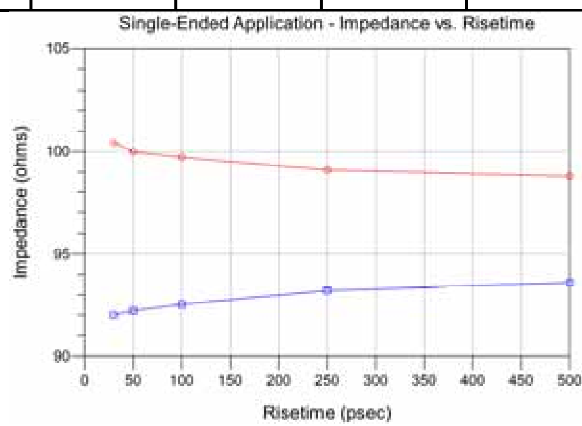


Table 9 – Differential Impedance (Ω) – Optimal Vertical					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	100.4	100	99.7	99.1	98.8
Minimum Impedance	92.0	92.2	92.5	93.2	93.6



Series: GMI
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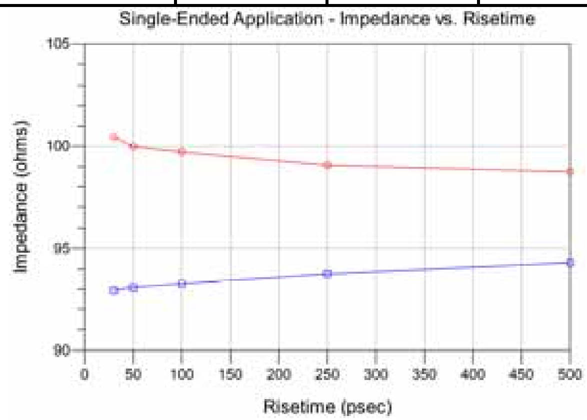
Table 10 – Differential Impedance (Ω) – High Density Vertical					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	100.5	100	99.7	99.1	98.7
Minimum Impedance	92.9	93.1	93.3	93.8	94.3



Series: GMI
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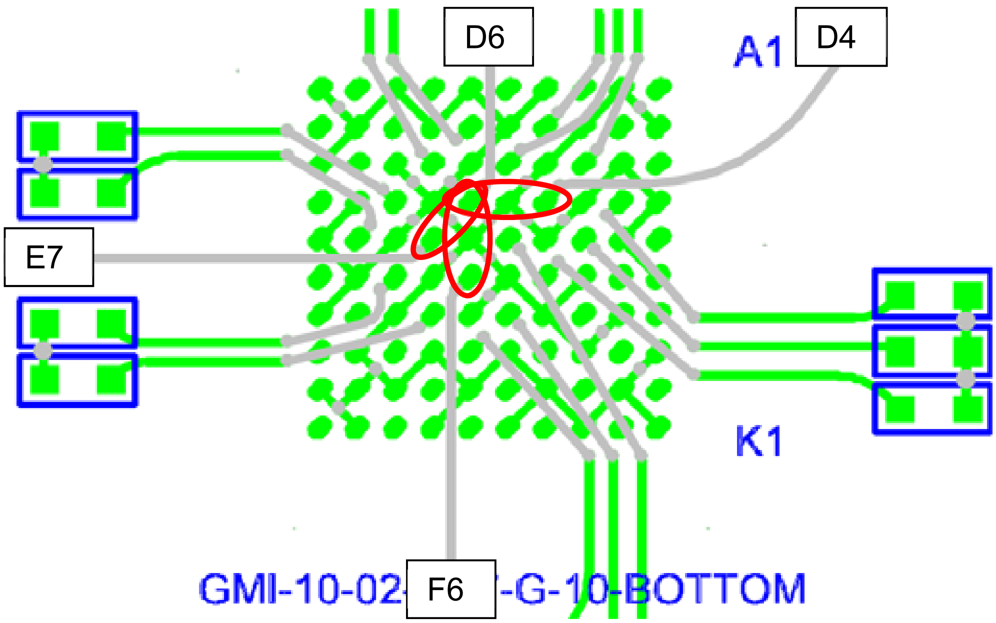
Table 11 - Single-Ended Crosstalk (%) – 1:1 S/G Pattern							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	AD6	AD4	0.75	0.68	0.61	0.31	0.16
	AD6	AF6	0.33	0.26	0.16	<0.1	<0.1
	AD6	AE7	1.65	1.12	0.58	0.25	0.16
FEXT	AD6	BD4	1.25	1.06	0.71	0.30	0.16
	AD6	BF6	0.30	0.23	0.15	<0.1	<0.1
	AD6	BE7	0.62	0.46	0.31	0.14	<0.1

Single-Ended 1:1 S/G Pattern Crosstalk Pin Map



Series: GMI
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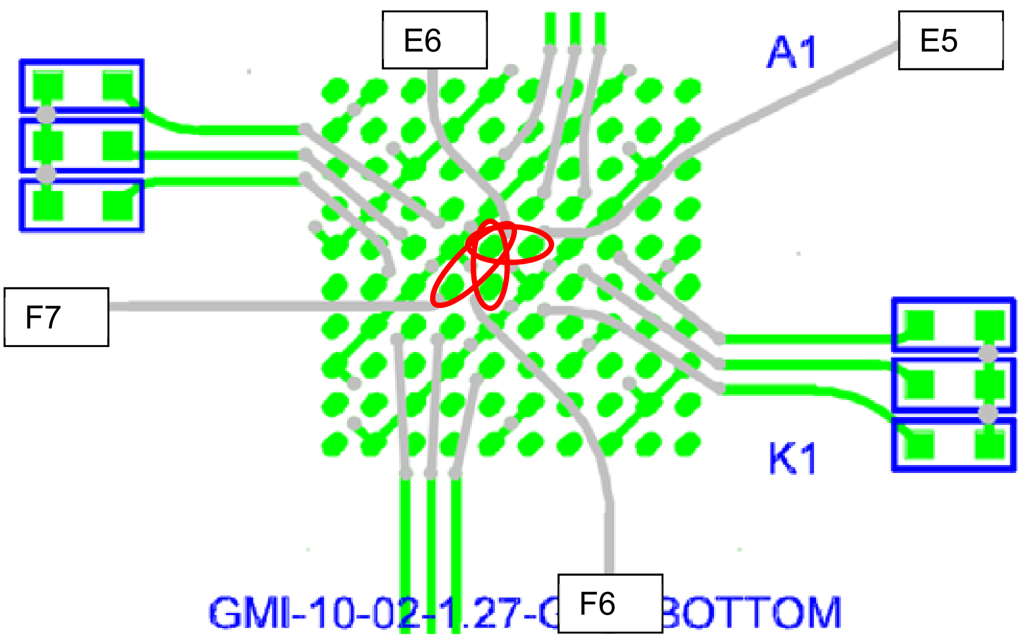
Table 12 - Single-Ended Crosstalk (%) – 2:1 S/G Pattern							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	AE6	AE5	7.97	7.35	5.59	2.81	1.48
	AE6	AF6	5.49	4.16	2.30	0.99	0.58
	AE6	AF7	2.67	2.23	1.31	0.60	0.32
FEXT	AE6	BE5	6.33	5.19	3.23	1.44	0.81
	AE6	BF6	1.96	1.73	1.13	0.52	0.28
	AE6	BF7	2.34	1.76	1.04	0.49	0.25

Single-Ended 2:1 S/G Pattern Crosstalk Pin Map



Series: GMI
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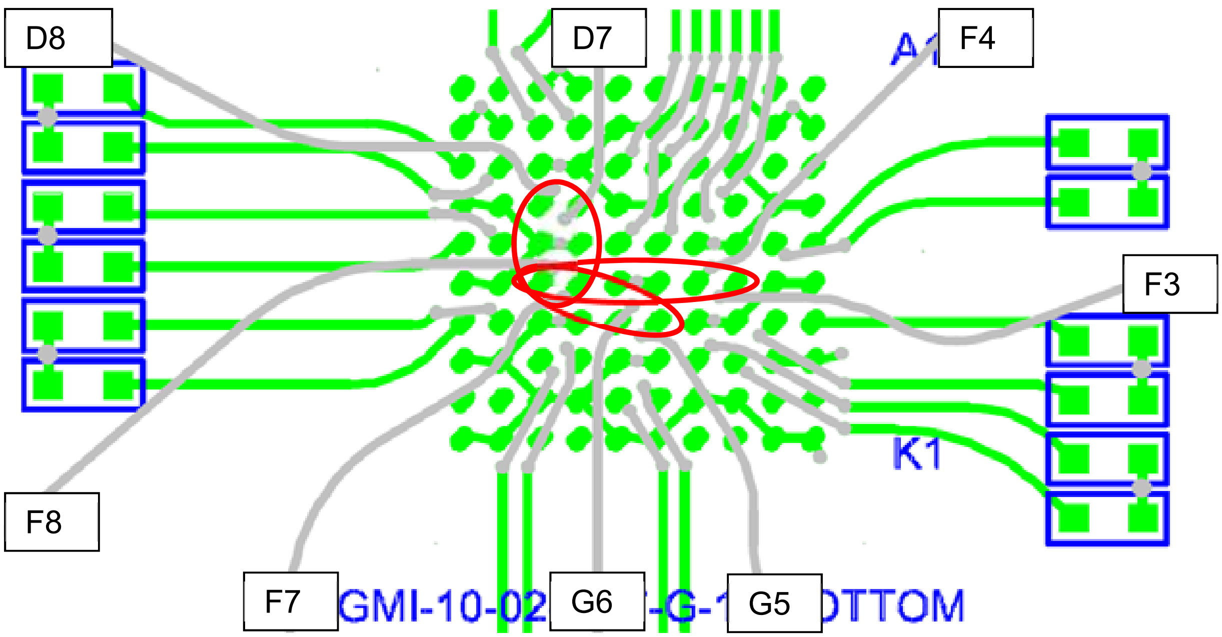
Table 13 - Differential Crosstalk (%) – Optimal Horizontal

Input(tr)	Driver	Receiver	30 ps	50 ps	100 ps	250 ps	500 ps
NEXT	AF7,AF8	AF3,AF4	<0.1	<0.1	<0.1	<0.1	<0.1
	AF7,AF8	AD7,AD8	0.20	<0.1	<0.1	<0.1	<0.1
	AF7,AF8	AG5,AG6	0.58	0.43	0.26	0.12	<0.1
FEXT	AF7,AF8	BF3,BF4	<0.1	<0.1	<0.1	<0.1	<0.1
	AF7,AF8	BD7,BD8	0.40	0.31	0.16	<0.1	<0.1
	AF7,AF8	BG5,BG6	0.76	0.47	0.19	<0.1	<0.1

Differential Optimal Horizontal Crosstalk Pin Map



Series: GMI
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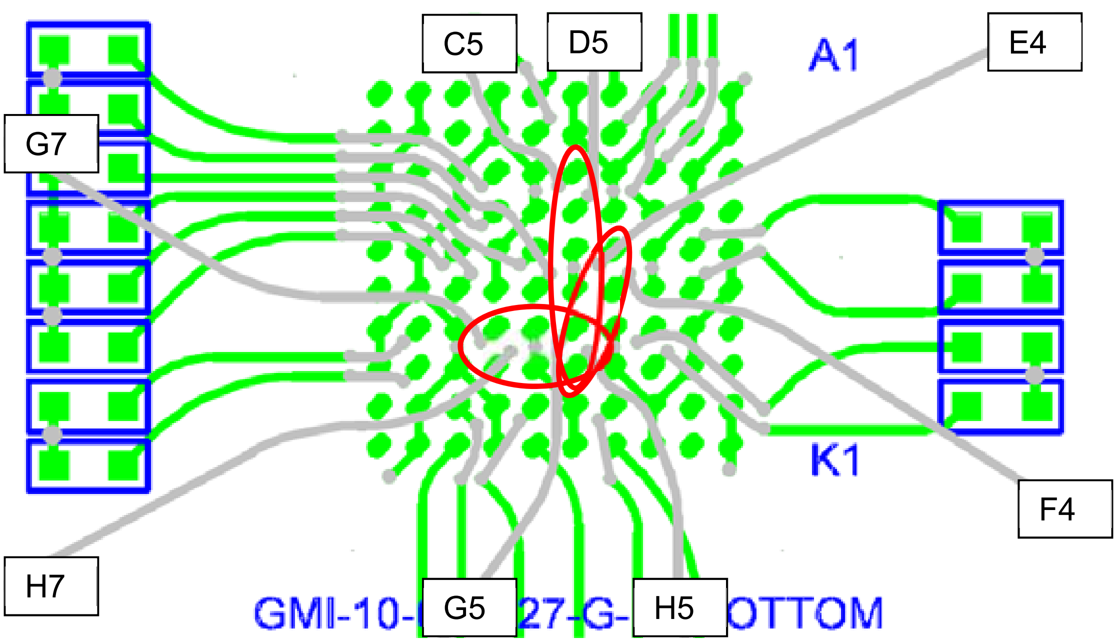
Table 14 - Differential Crosstalk (%) – Optimal Vertical							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	AG5,AH5	AG7,AH7	0.18	0.11	<0.1	<0.1	<0.1
	AG5,AH5	AC5,AD5	0.18	0.17	0.14	<0.1	<0.1
	AG5,AH5	AE4,AF4	0.70	0.40	0.15	<0.1	<0.1
FEXT	AG5,AH5	BG7,BH7	0.34	0.21	<0.1	<0.1	<0.1
	AG5,AH5	BC5,BD5	0.15	0.13	<0.1	<0.1	<0.1
	AG5,AH5	BE4,BF4	0.18	0.12	<0.1	<0.1	<0.1

Differential Optimal Vertical Crosstalk Pin Map



Series: GMI
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Table 15 - Differential Crosstalk (%) – High Density Vertical

Input(tr)	Driver	Receiver	30 ps	50 ps	100 ps	250 ps	500 ps
NEXT	AF6,AG6	AF4,AG4	0.91	0.41	0.36	0.18	<0.1
	AF6,AG6	AC6,AD6	0.32	0.23	<0.1	<0.1	<0.1
	AF6,AG6	AE7,AF7	3.38	2.57	2.03	1.07	0.52
FEXT	AF6,AG6	BF4,BG4	0.27	0.15	<0.1	<0.1	<0.1
	AF6,AG6	BC6,BD6	0.26	0.17	<0.1	<0.1	<0.1
	AF6,AG6	BE7,BF7	1.48	0.88	0.39	0.15	0.13

Differential High Density Vertical Crosstalk Pin Map

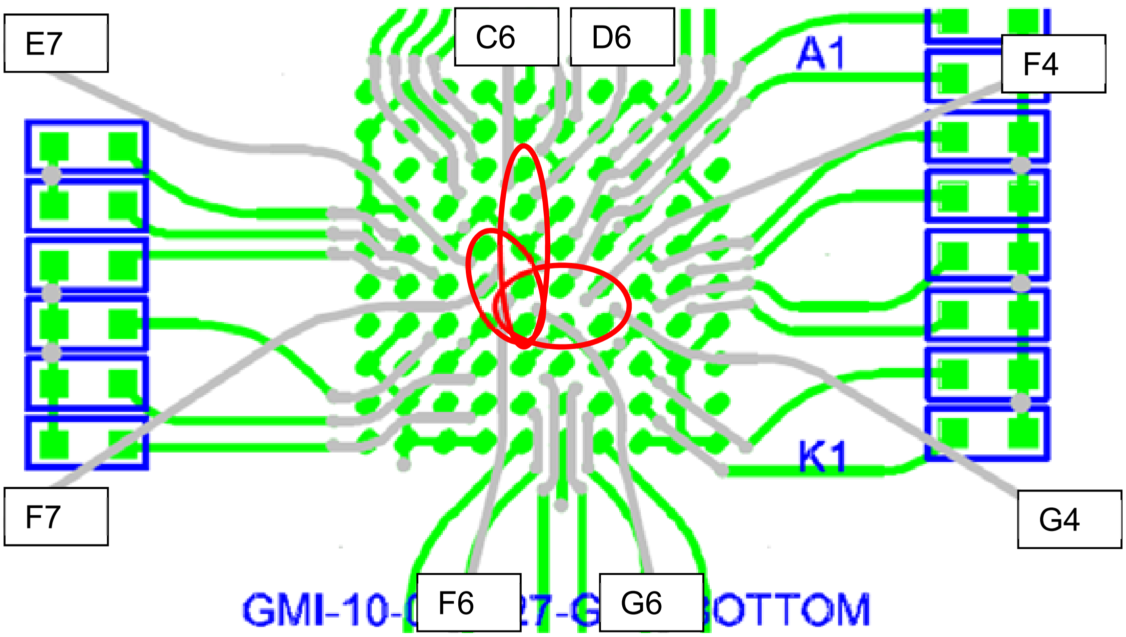

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Table 16 - Propagation Delay (Mated Connector)	
Single-Ended: 1:1 S/G	48 ps
Single-Ended: 2:1 S/G	50 ps
Differential: Optimal Horizontal	43 ps
Differential: Optimal Vertical	43 ps
Differential: High Density Vertical	46 ps

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as “ground”. In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. However dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

Series: GMI
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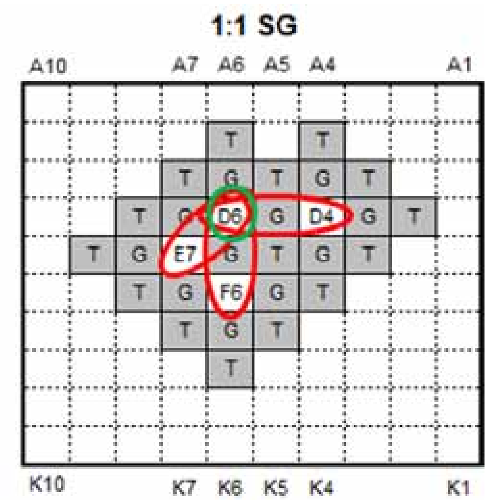
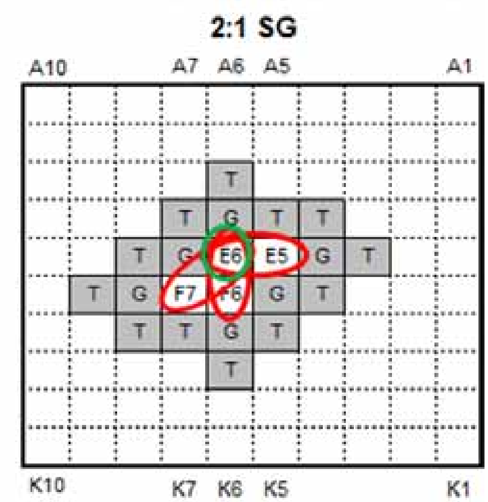
For this connector, the following array configurations are evaluated:

	Open pin field	G	Grounded pin field
	Signal pin field	T	50 ohm termination field





Single-Ended Impedance (denoted by green circles):
- 1:1 S/G ratio
- 2:1 S/G ratio

Single-Ended Crosstalk (denoted by red circles):
- 1:1 S/G ratio
- 2:1 S/G ratio

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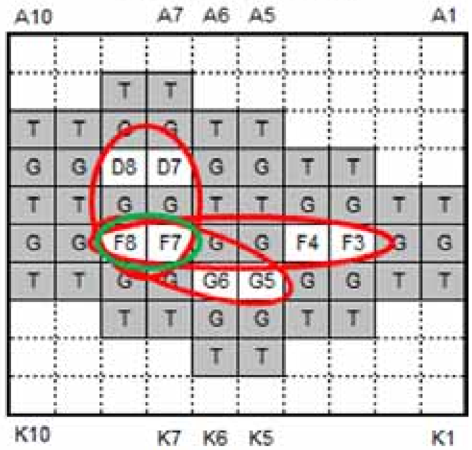
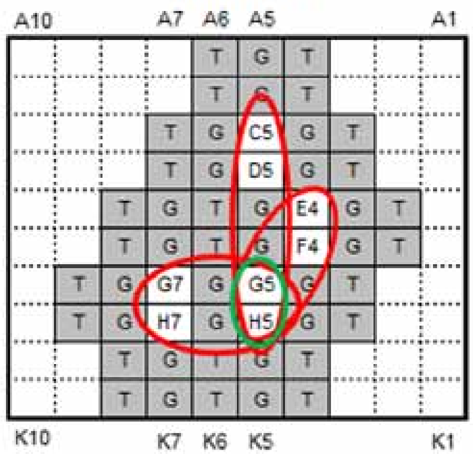
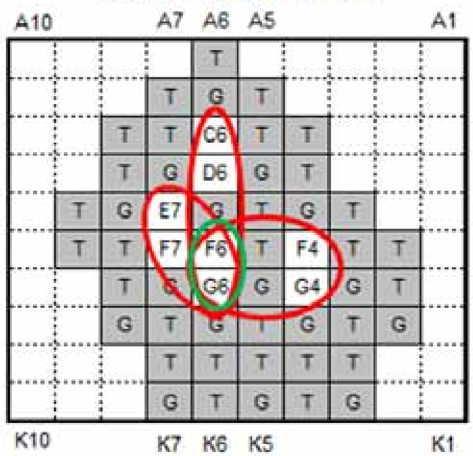
Optimal Horizontal



Optimal Vertical



High Density Vertical



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Differential Impedance (denoted by green circles)**:**

- Optimal Horizontal
- Optimal Vertical
- High Density Vertical

Differential Crosstalk (denoted by red circles)**:**

- Optimal Horizontal
- Optimal Vertical
- High Density Vertical

Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals might be encountered as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. However, in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate the worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data
Frequency Domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

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Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time and crosstalk in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix B of this report.

The measured S-Parameters from the network analyzer are post-processed using Agilent Advanced Design System to obtain the time domain response for signal propagation time and crosstalk. The Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 18 mils PCB trace on each side of the test board. Delay is measured at 100 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

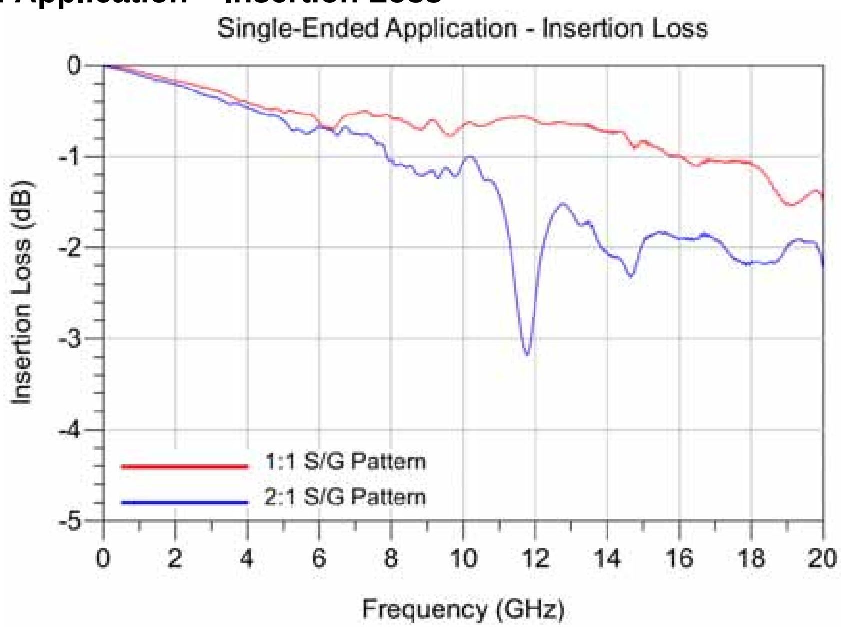
As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. However, modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

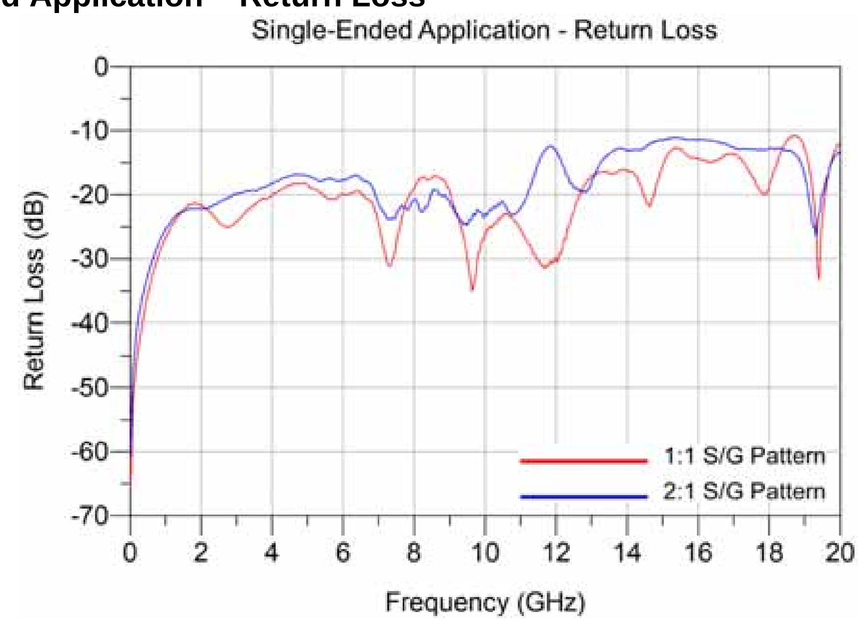
Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss

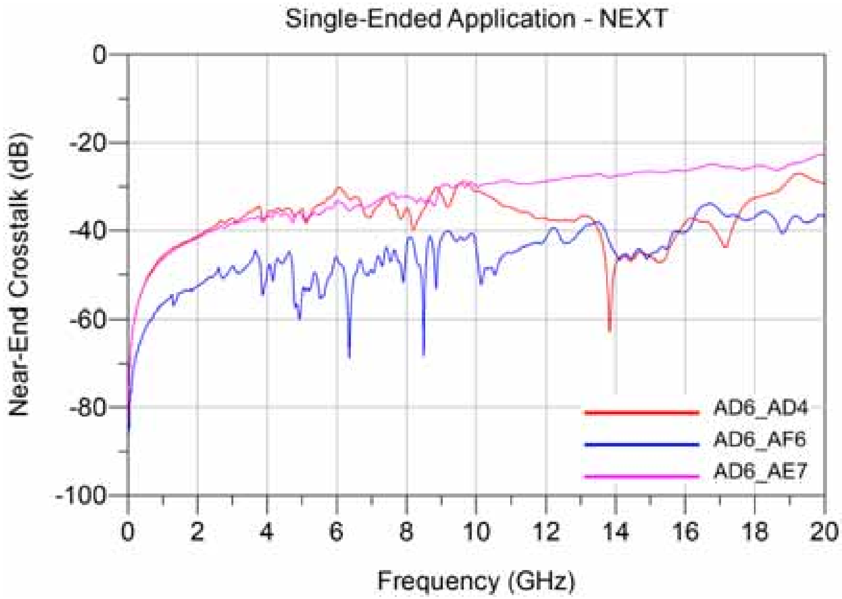


Single-Ended Application – Return Loss

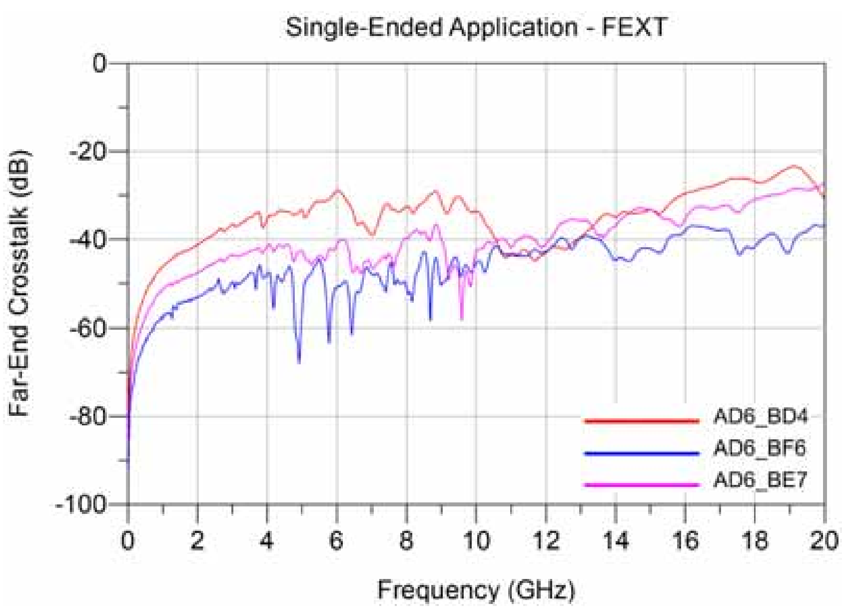


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 1:1 S/G Pattern Application – NEXT

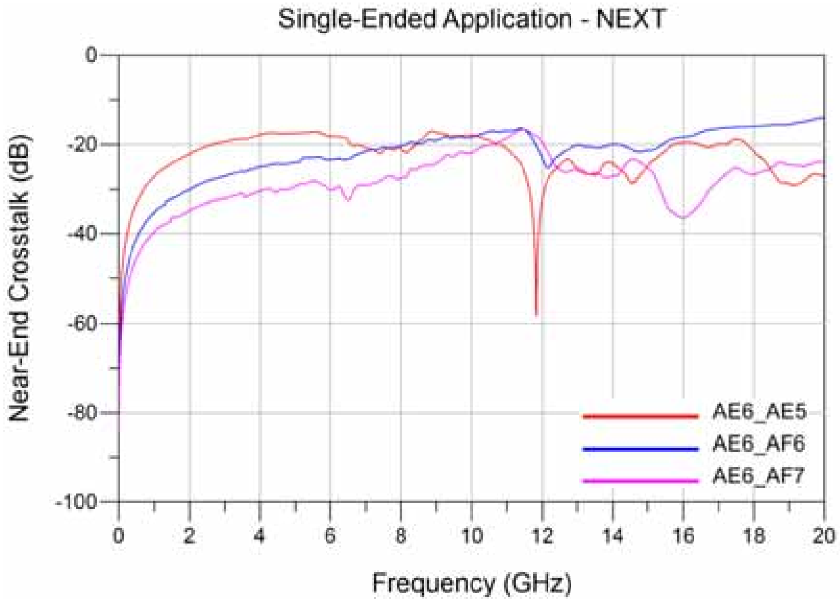


Single-Ended 1:1 S/G Pattern Application – FEXT

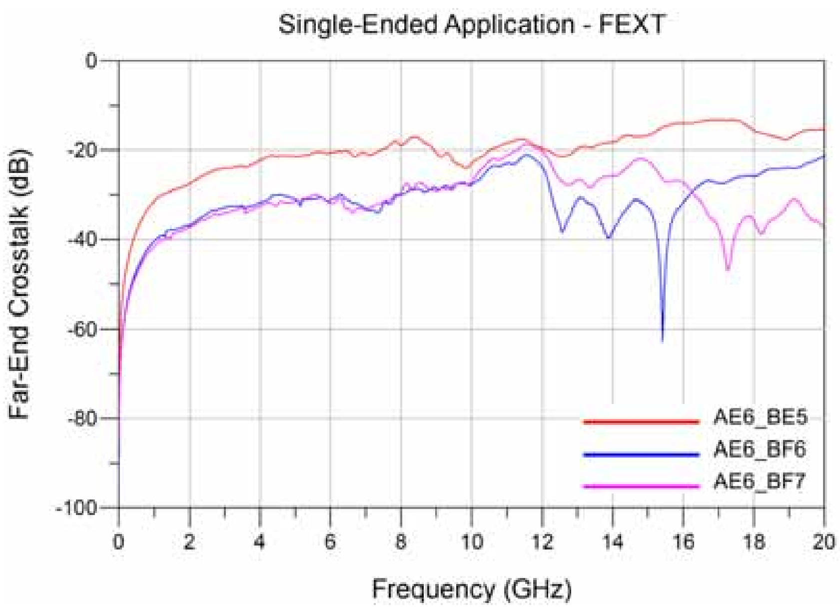


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 2:1 S/G Pattern Application – NEXT

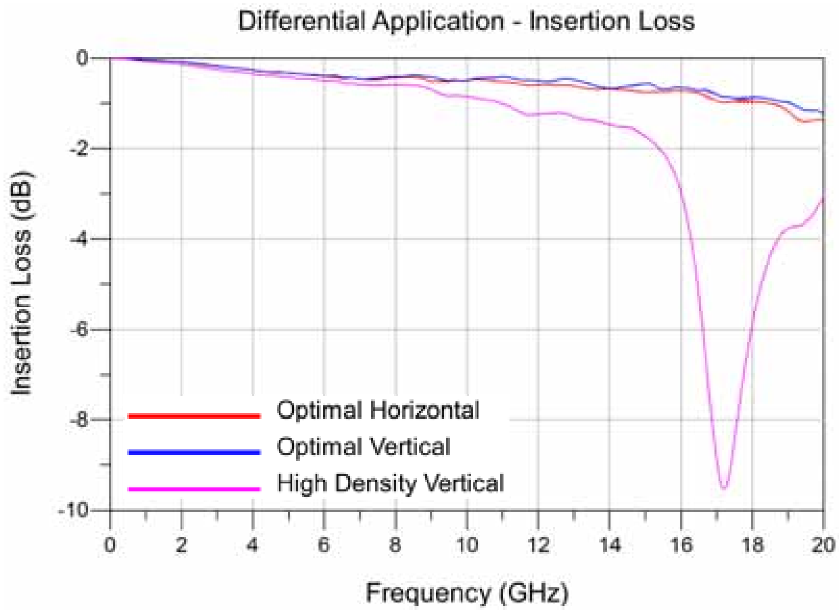


Single-Ended 2:1 S/G Pattern Application – FEXT

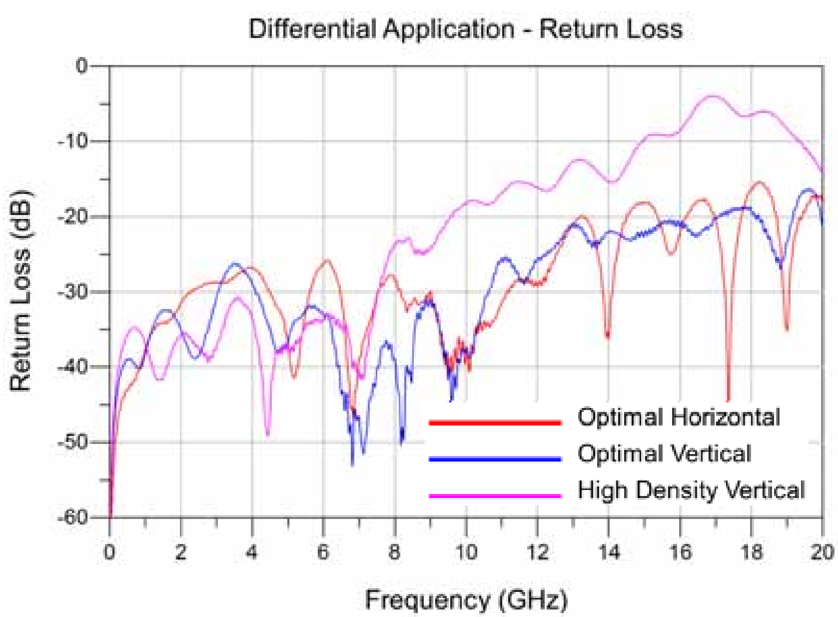


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential Application – Insertion Loss

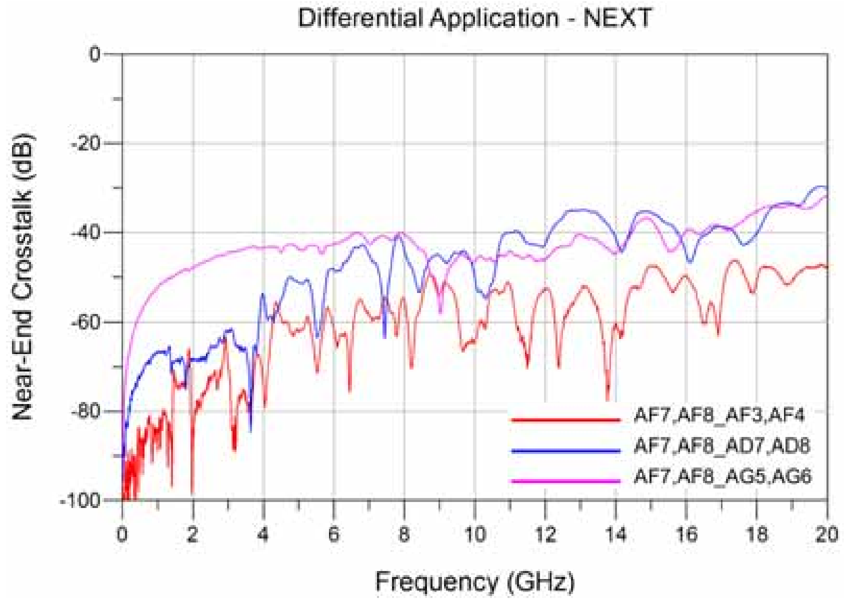


Differential Application – Return Loss

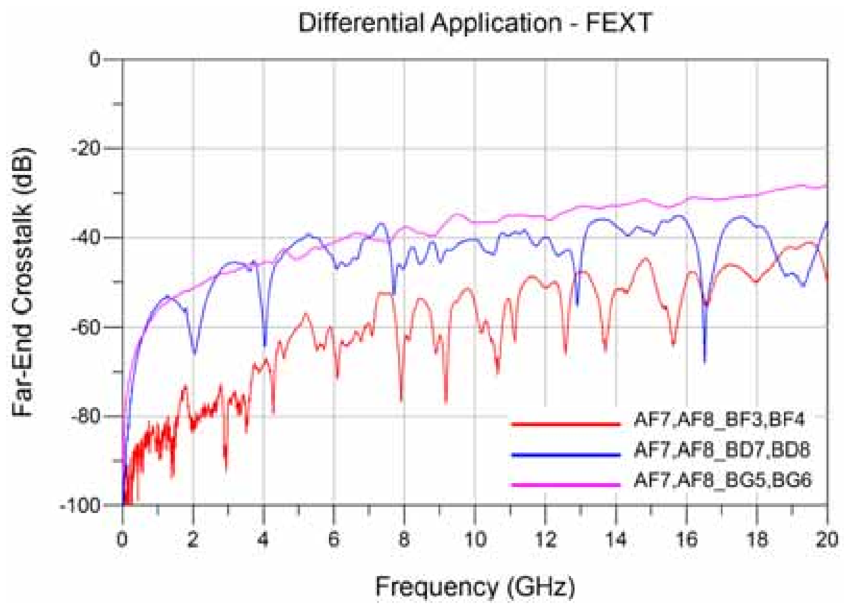


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential Optimal Horizontal Application – NEXT

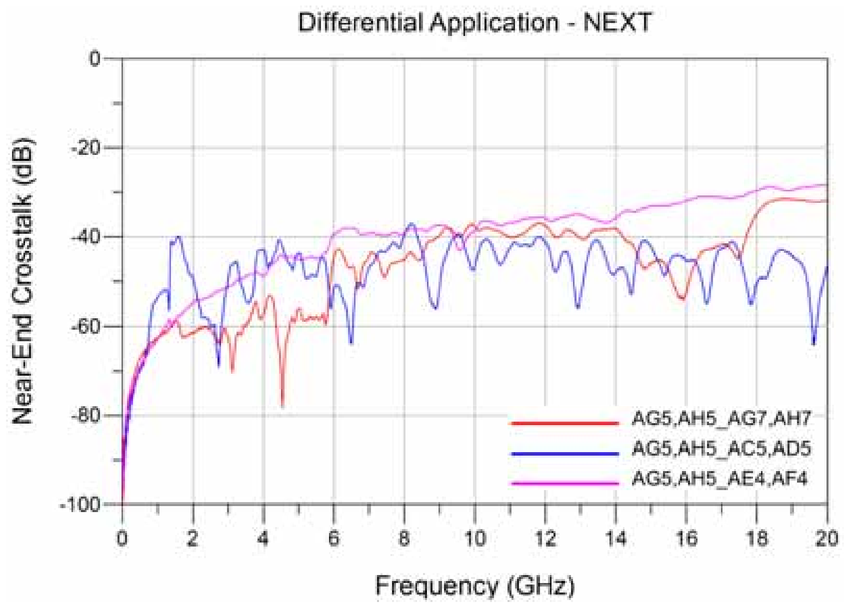


Differential Optimal Horizontal Application – FEXT

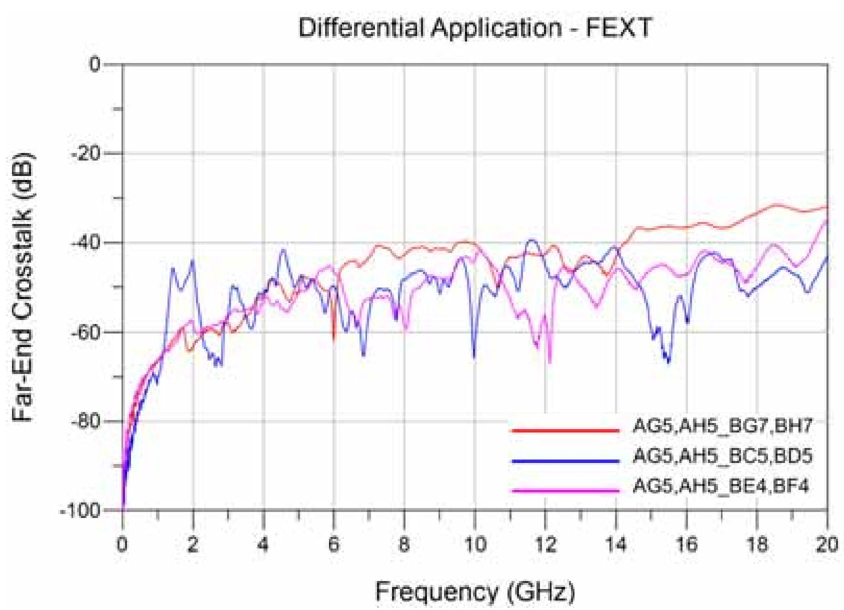


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential Optimal Vertical Application – NEXT

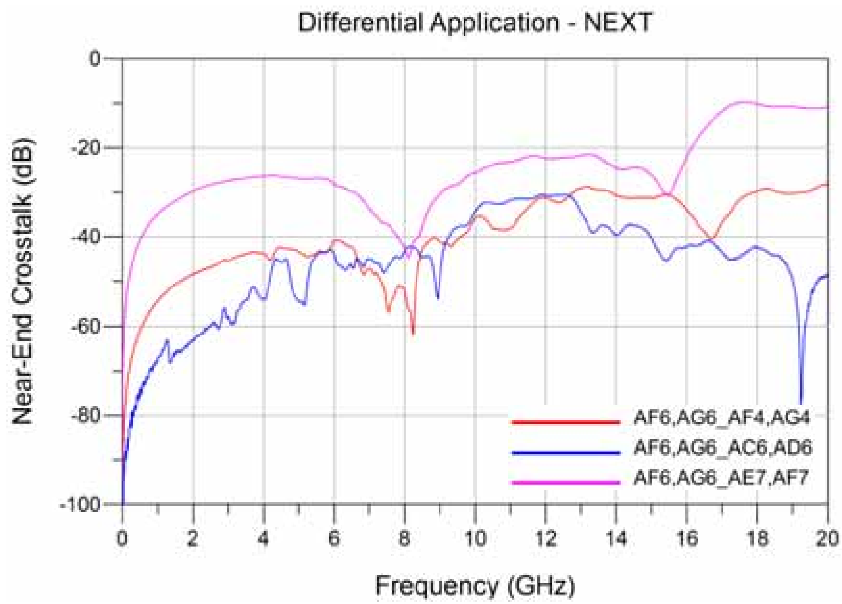


Differential Optimal Vertical Application – FEXT

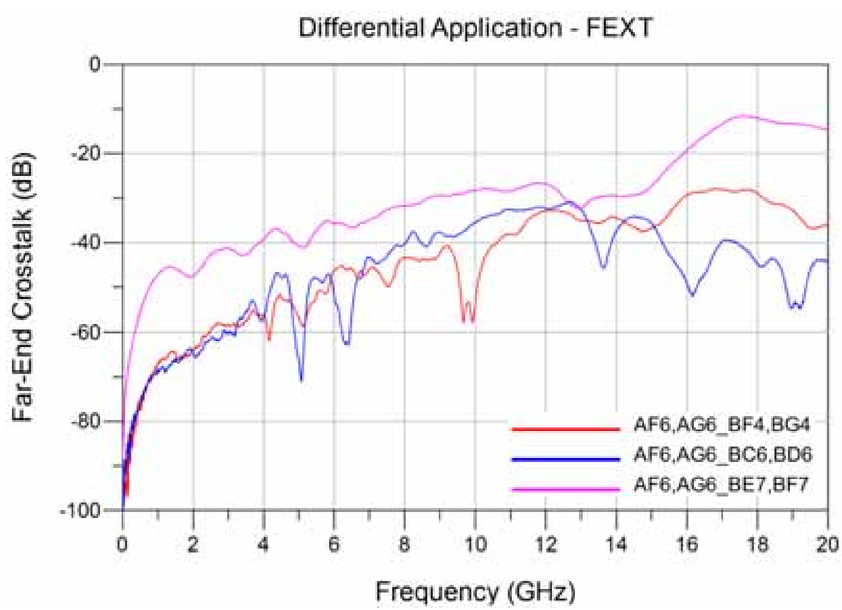


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential High Density Vertical Application – NEXT



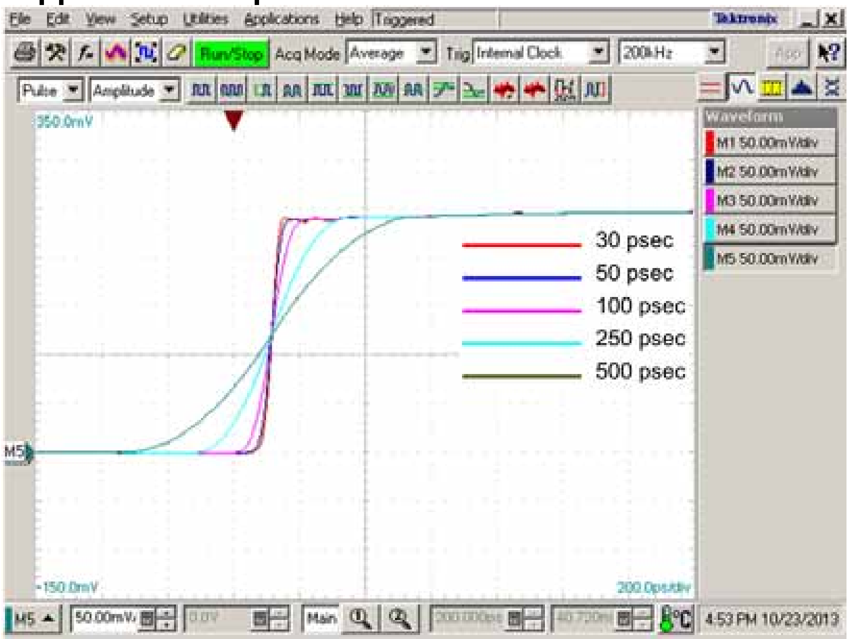
Differential High Density Vertical Application – FEXT



Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

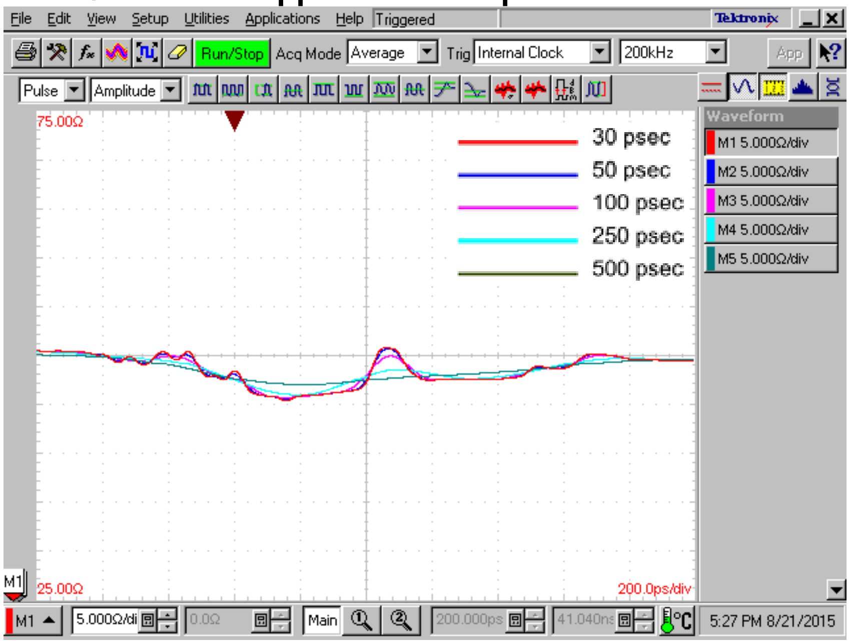
Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse

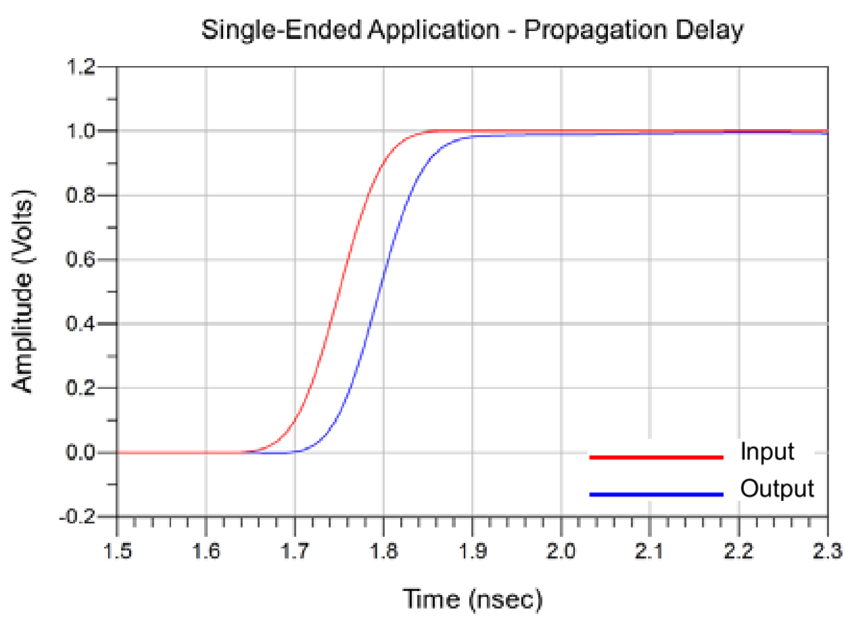


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 1:1 S/G Pattern Application – Impedance



Single-Ended 1:1 S/G Pattern Application – Propagation Delay



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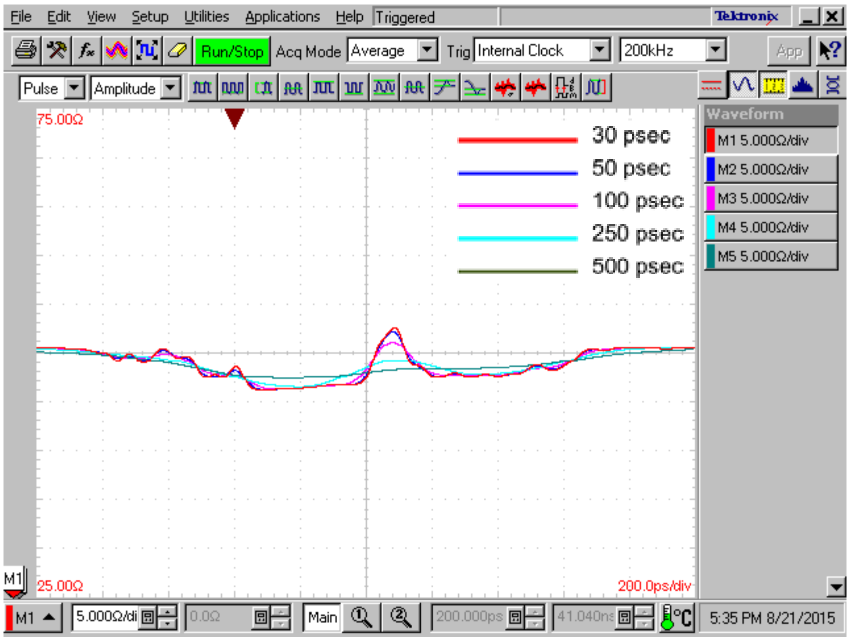
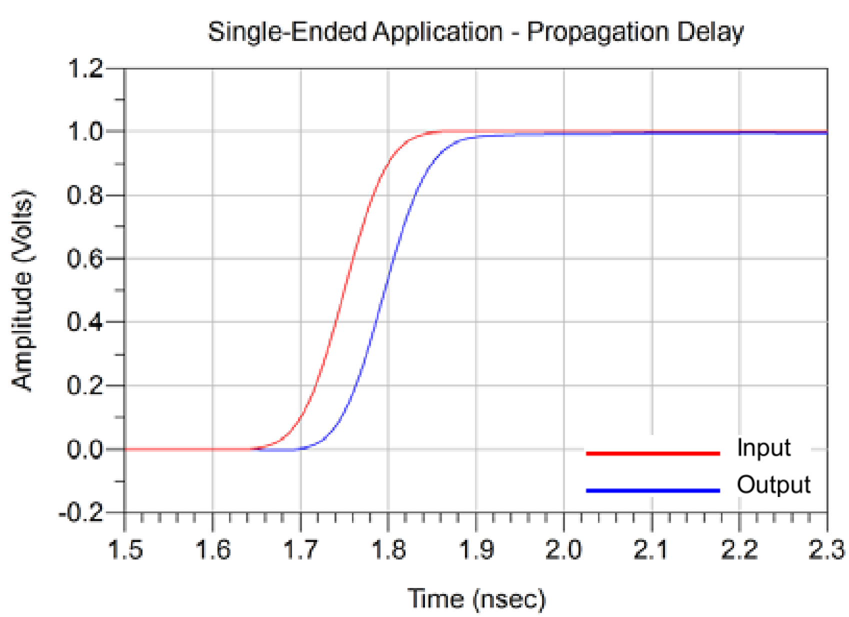
Report Revision: 9/11/2015

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 2:1 S/G Pattern Application – Impedance



Single-Ended 2:1 S/G Pattern Application – Propagation Delay



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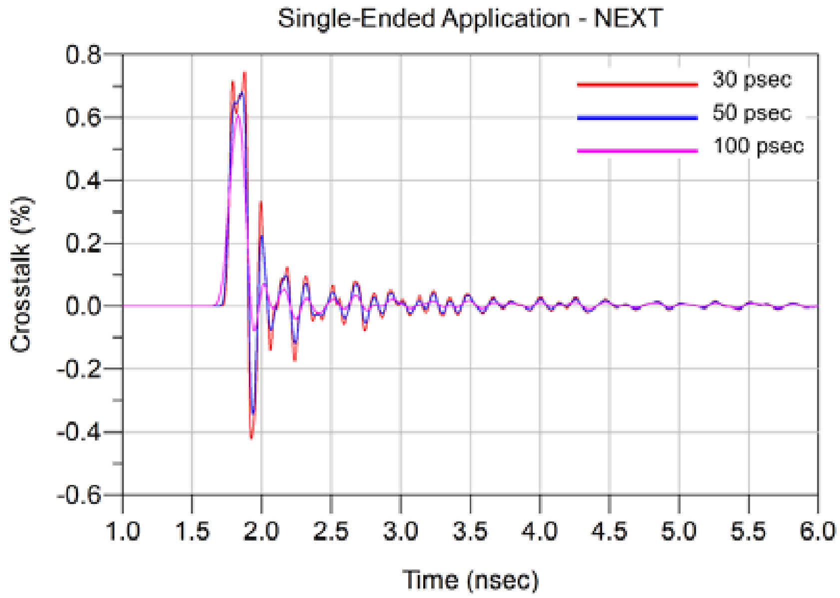
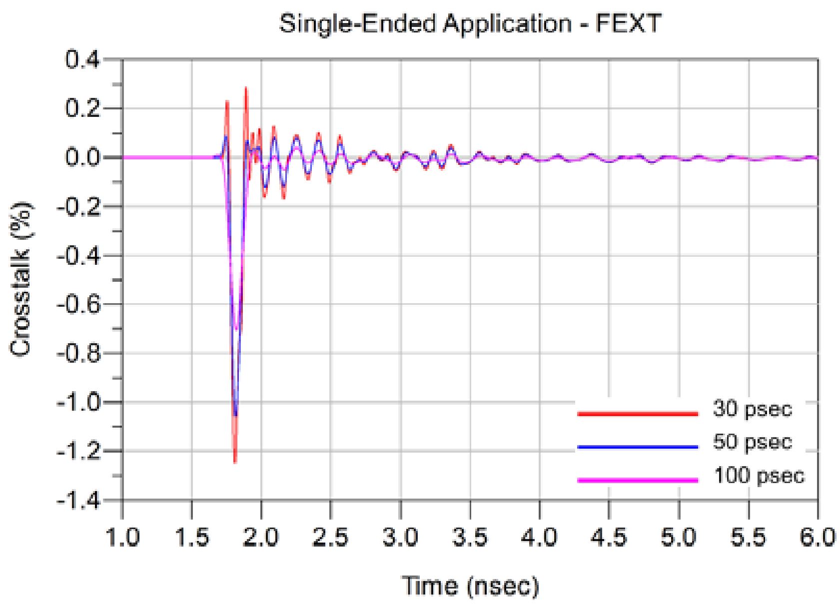
Report Revision: 9/11/2015

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 1:1 S/G Pattern Application – NEXT, AD6_AD4

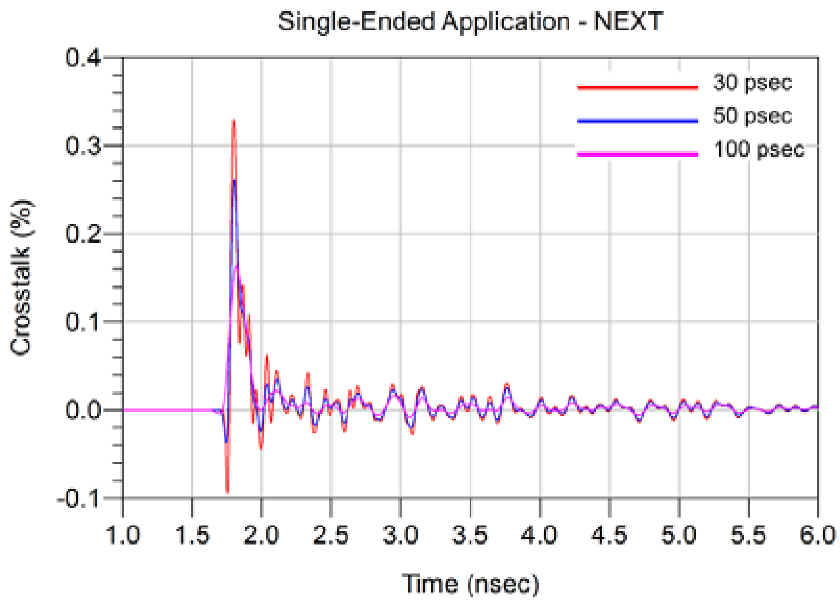


Single-Ended 1:1 S/G Pattern Application – FEXT, AD6_BD4

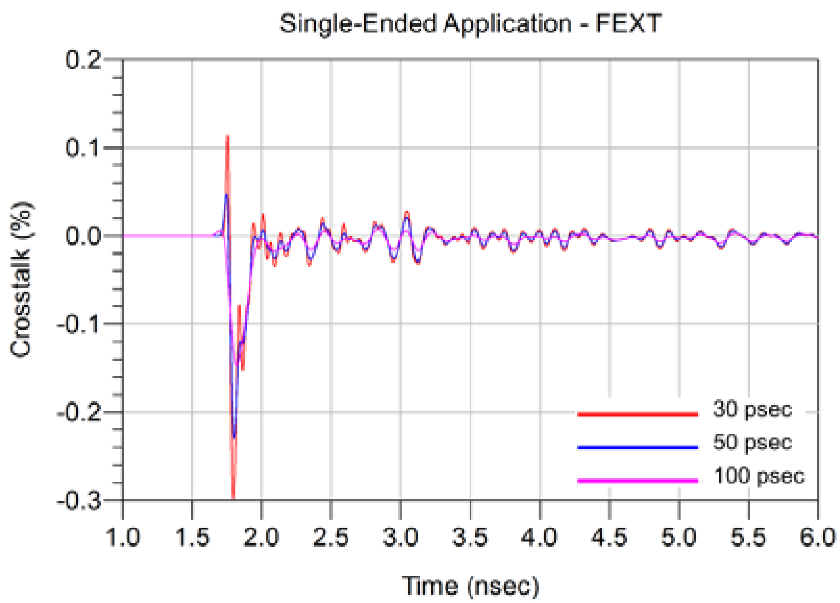


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 1:1 S/G Pattern Application – NEXT, AD6_AF6

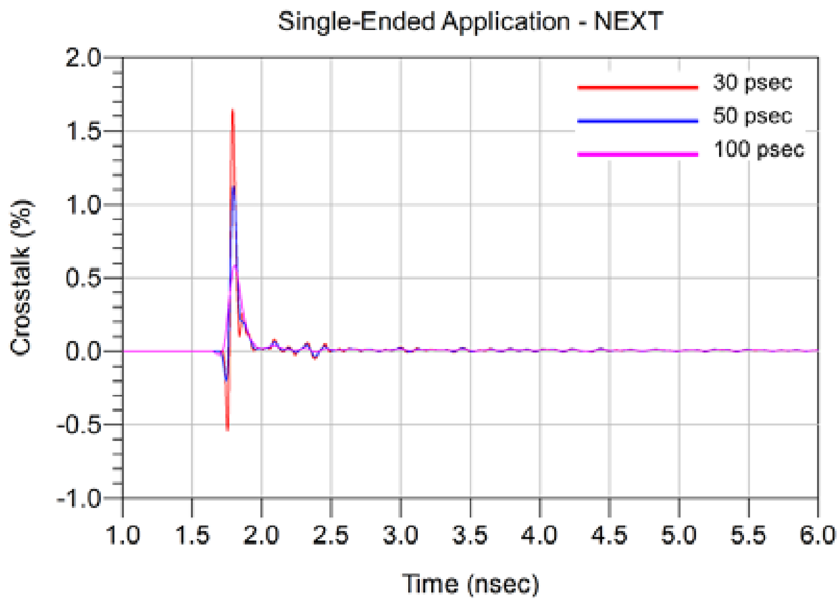


Single-Ended 1:1 S/G Pattern Application – FEXT, AD6_BF6

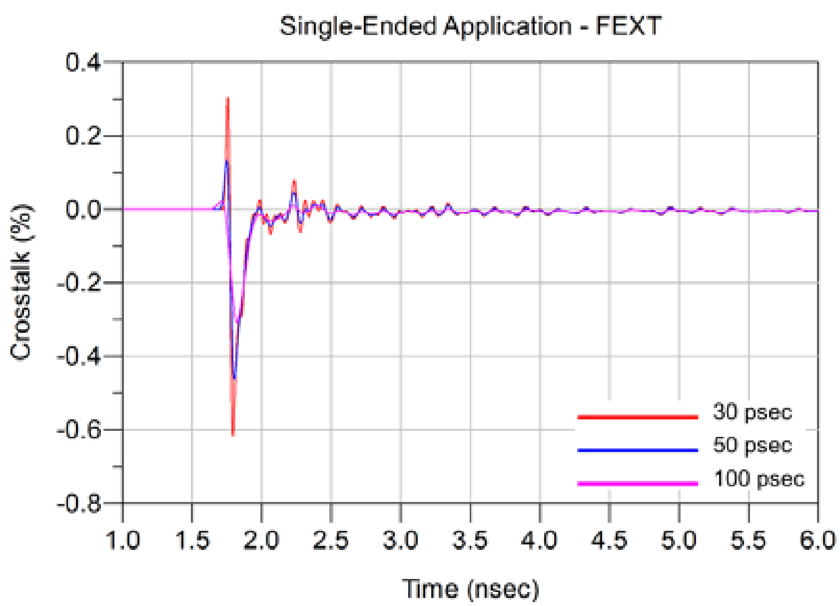


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 1:1 S/G Pattern Application – NEXT, AD6_AE7

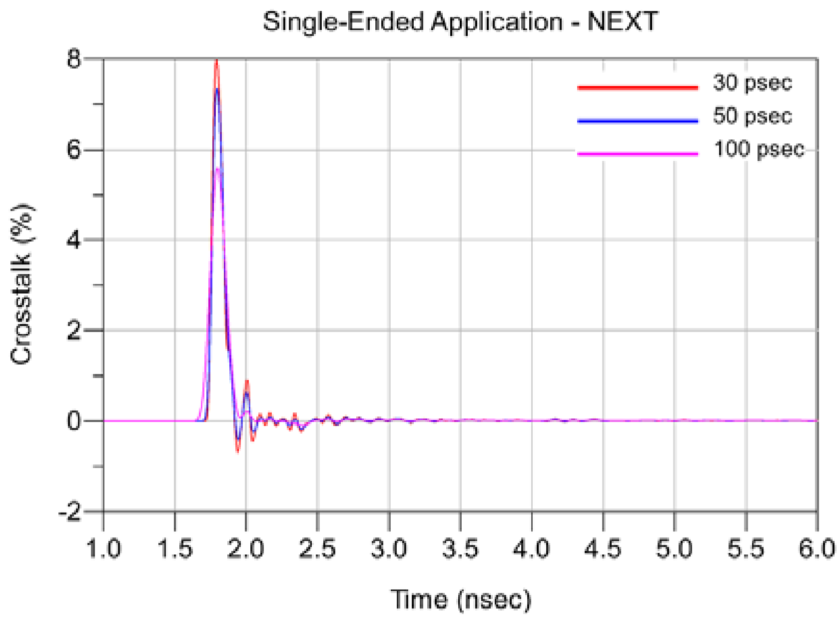


Single-Ended 1:1 S/G Pattern Application – FEXT, AD6_BE7

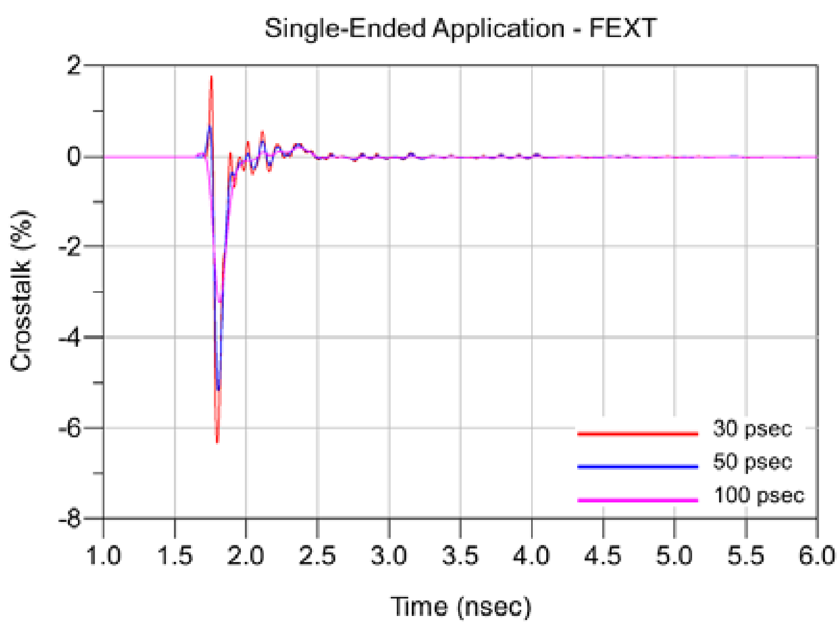


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 2:1 S/G Pattern Application – NEXT, AE6_AE5

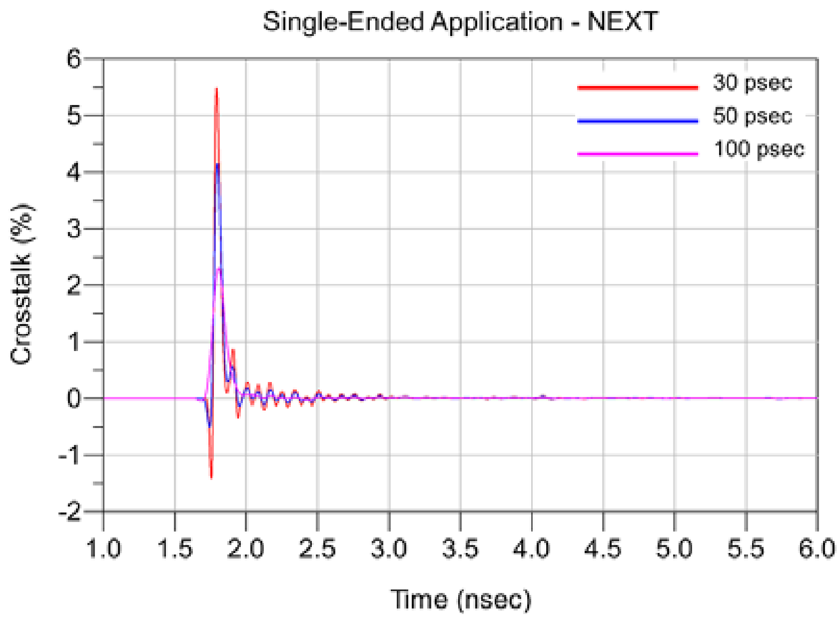


Single-Ended 2:1 S/G Pattern Application – FEXT, AE6_BE5

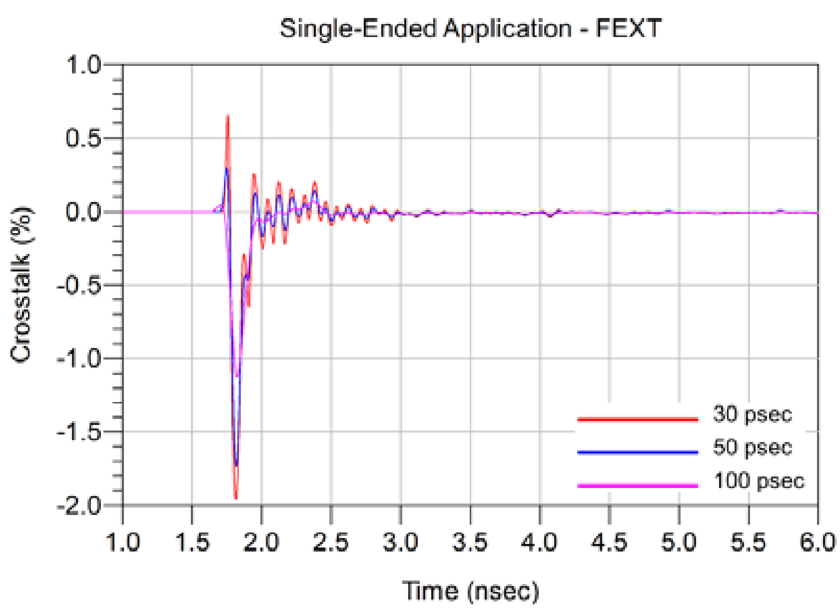


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 2:1 S/G Pattern Application – NEXT, AE6_AF6

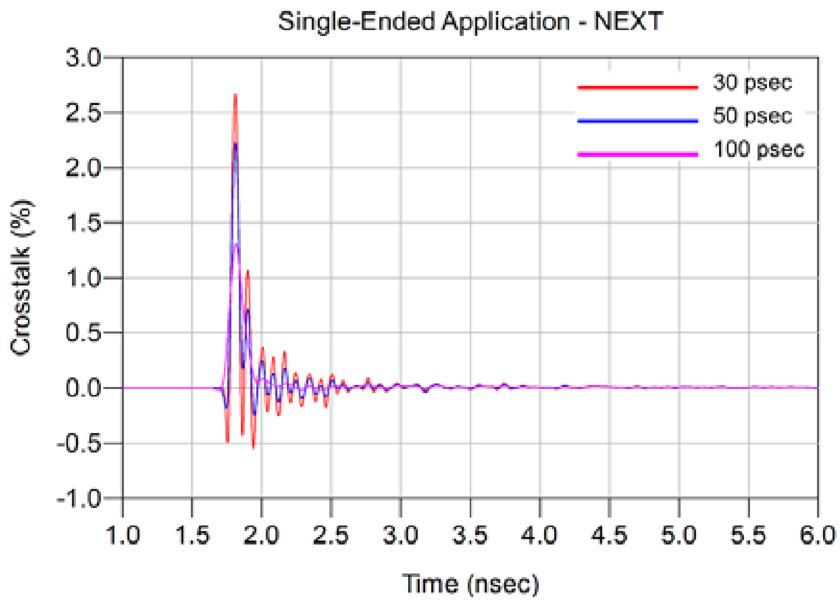


Single-Ended 2:1 S/G Pattern Application – FEXT, AE6_BF6

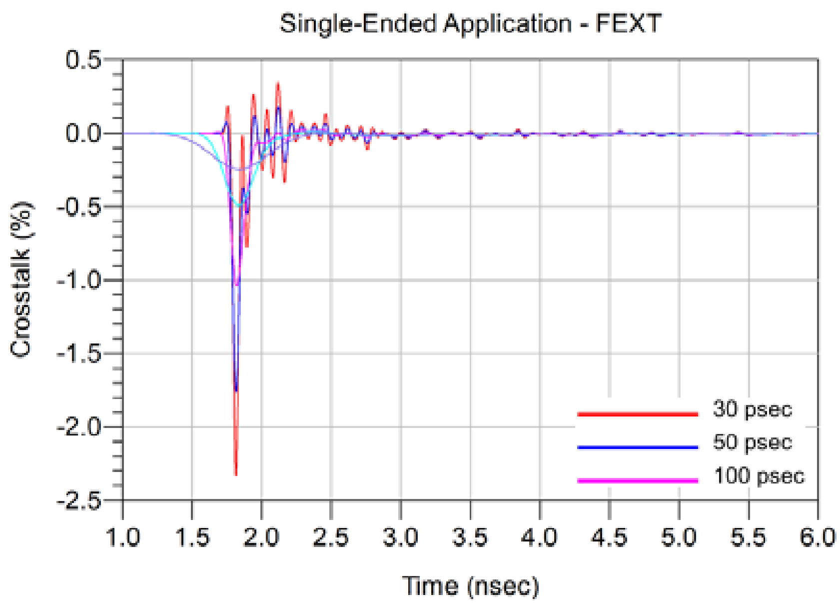


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Single-Ended 2:1 S/G Pattern Application – NEXT, AE6_AF7

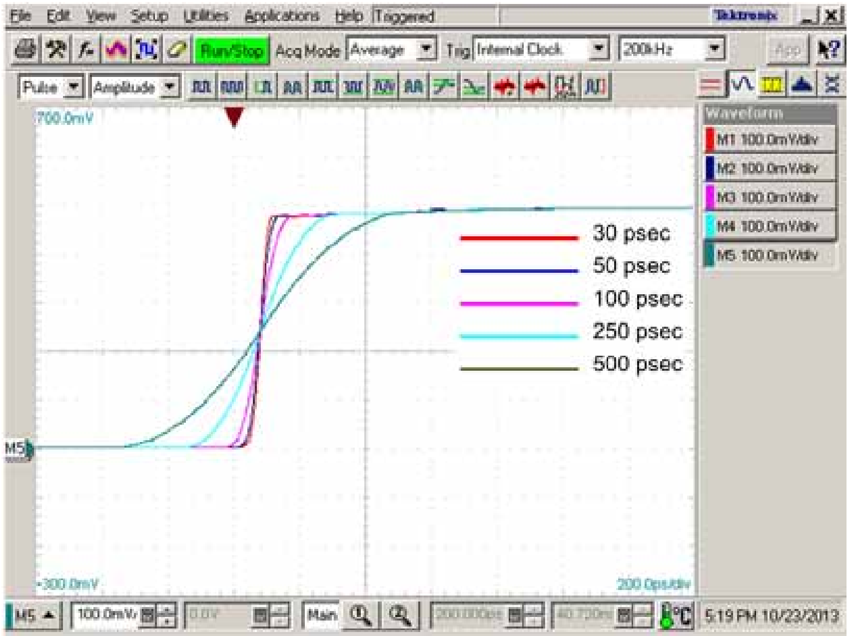


Single-Ended 2:1 S/G Pattern Application – FEXT, AE6_BF7



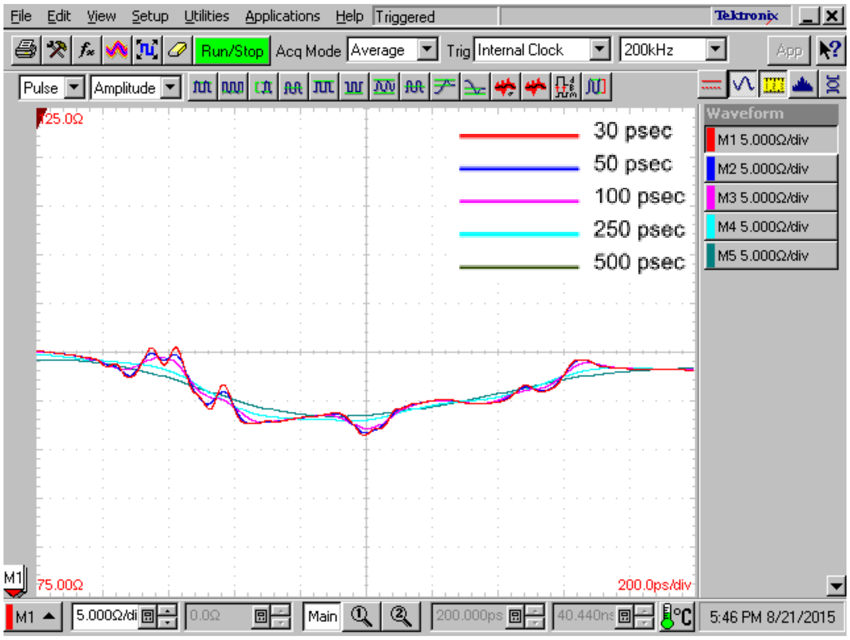
Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential Application – Input Pulse

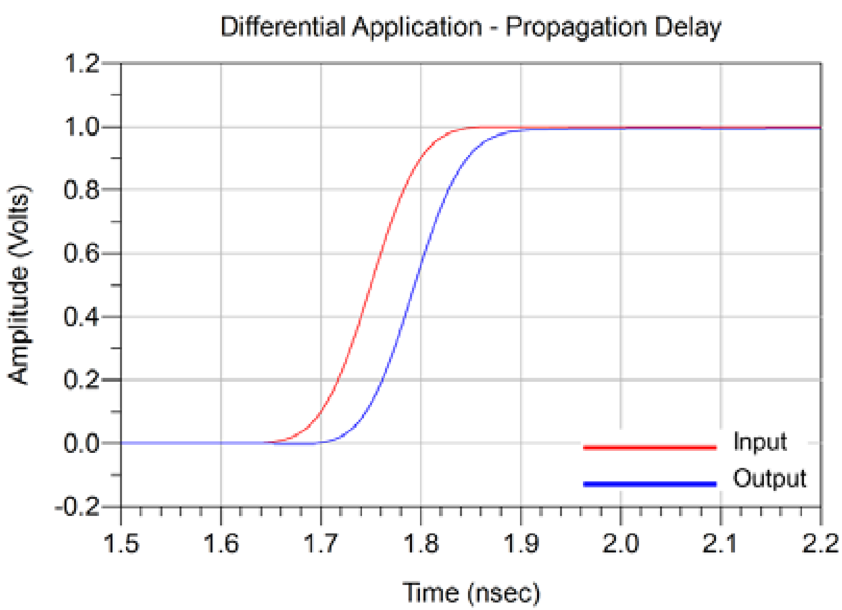


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential Optimal Horizontal Application – Impedance

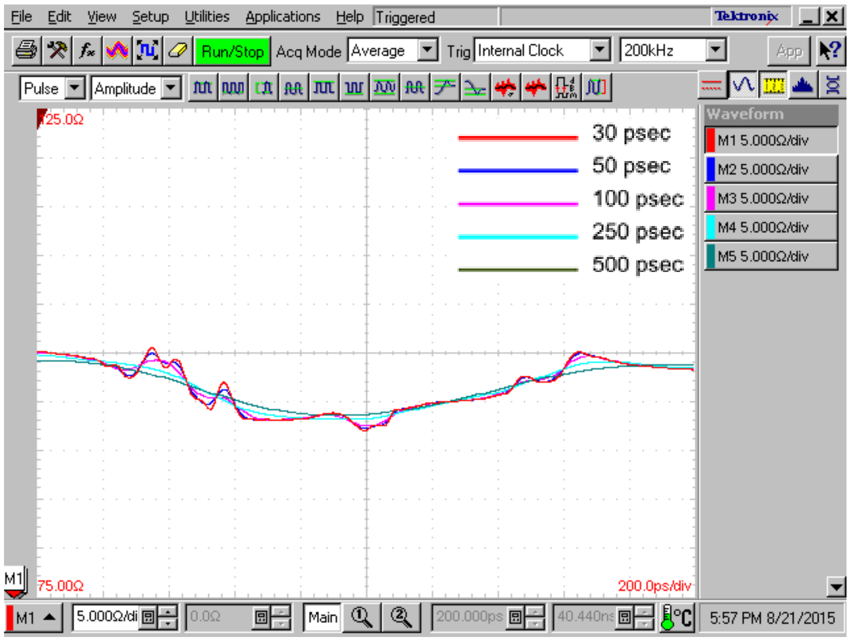


Differential Optimal Horizontal Application – Propagation Delay

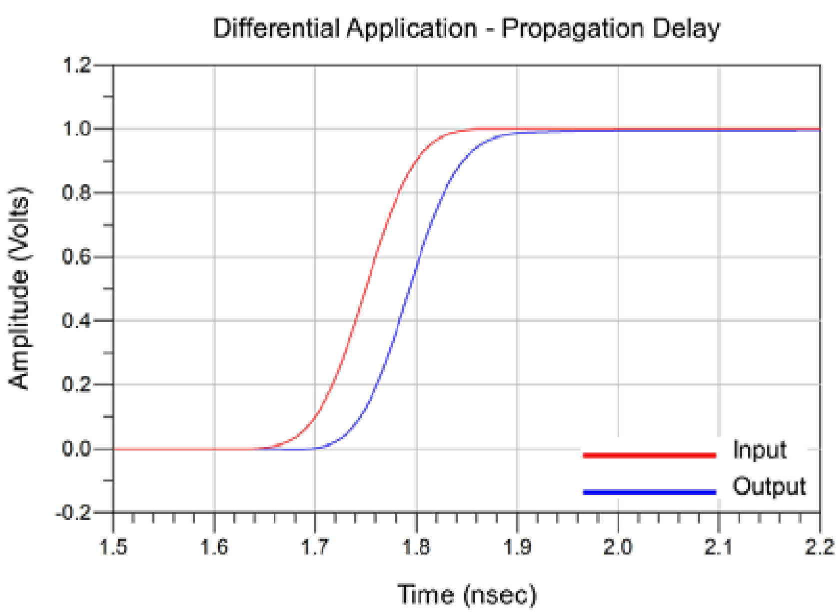


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential Optimal Vertical Application – Impedance



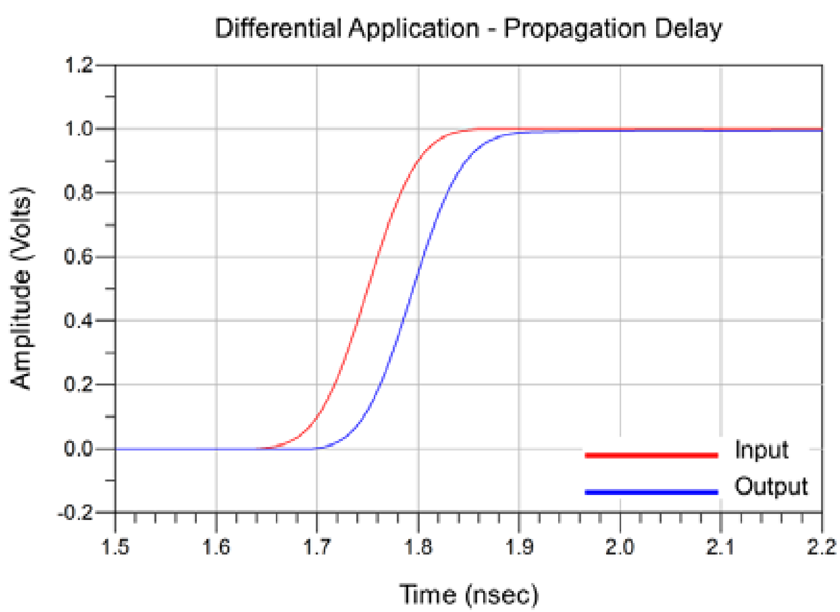
Differential Optimal Vertical Application – Propagation Delay



Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Differential High Density Vertical Application – Impedance

Differential High Density Vertical Application – Propagation Delay



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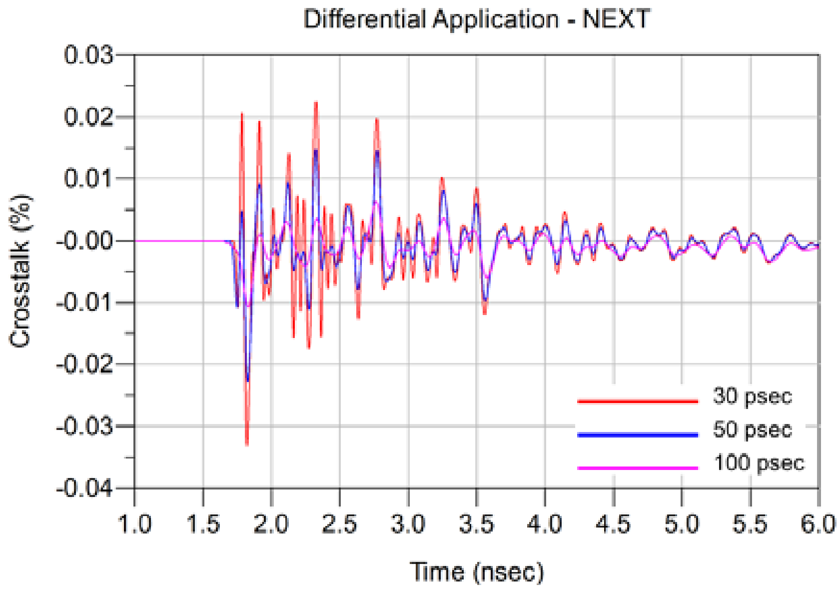
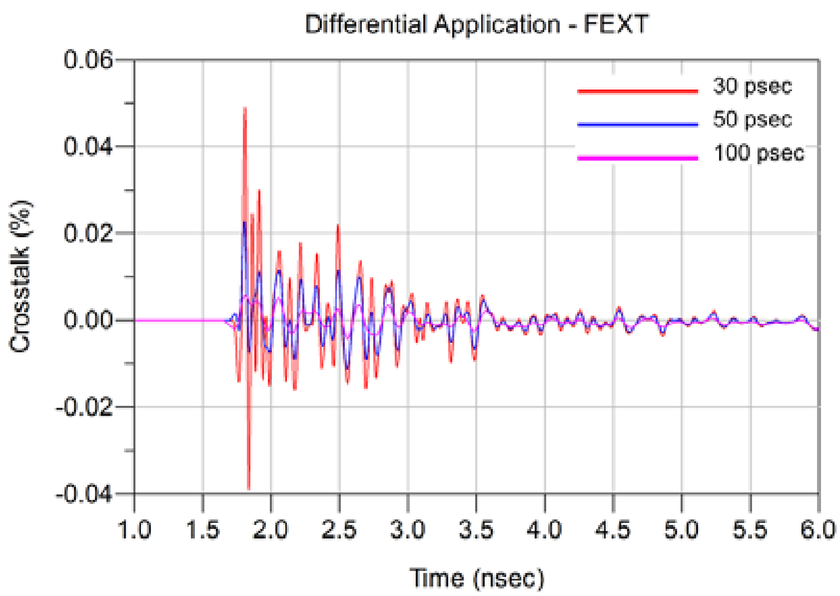
Report Revision: 9/11/2015

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff Optimal Horizontal Application – NEXT, AF7,AF8_AF3,AF4

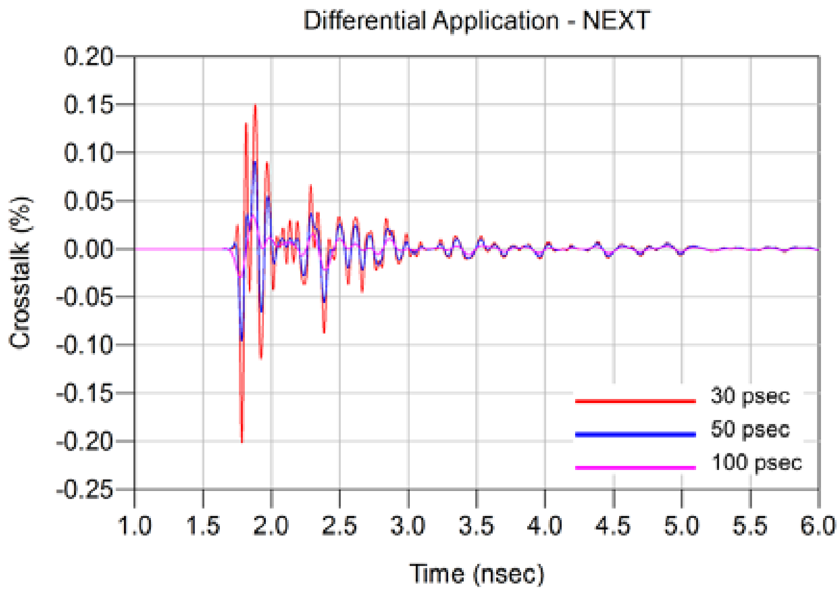


Diff Optimal Horizontal Application – FEXT, AF7,AF8_BF3,BF4

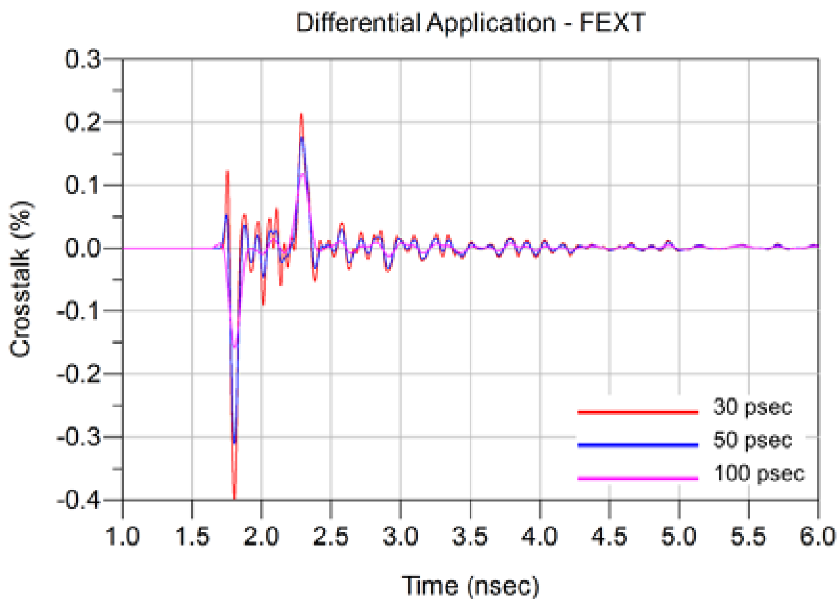


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff Optimal Horizontal Application – NEXT, AF7,AF8_AD7,AD8

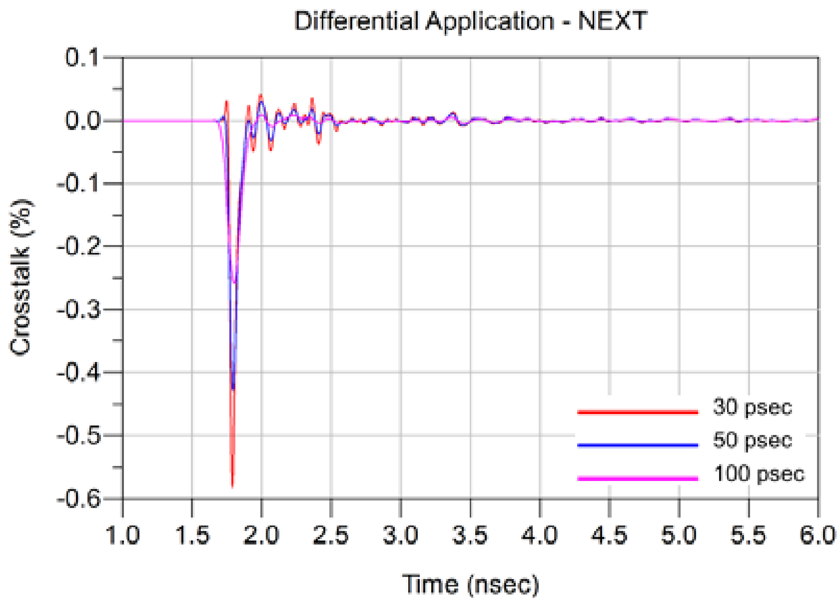


Diff Optimal Horizontal Application – FEXT, AF7,AF8_BD7,BD8

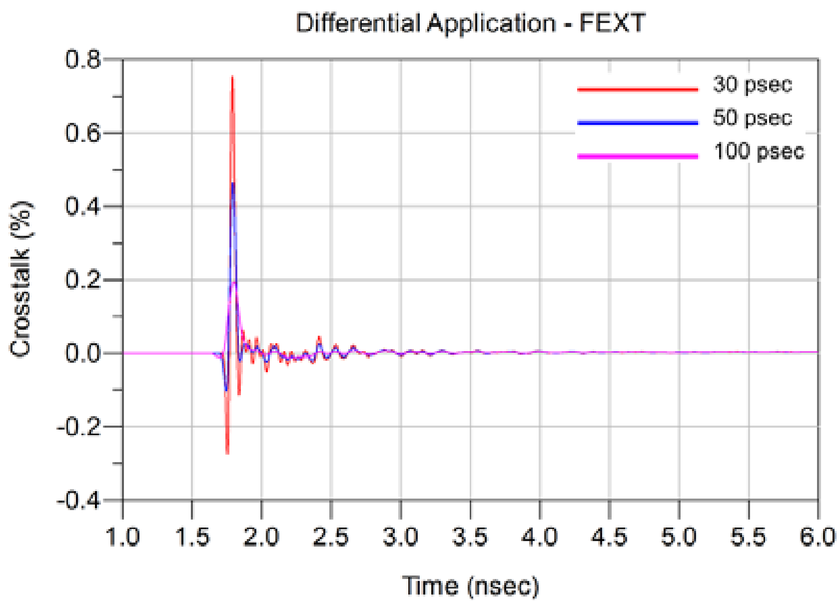


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff Optimal Horizontal Application – NEXT, AF7,AF8_AG5,AG6

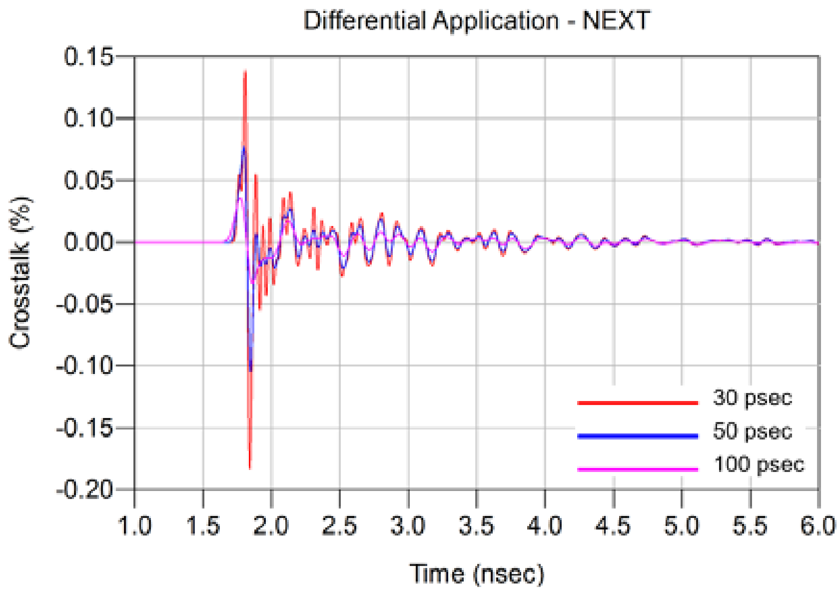


Diff Optimal Horizontal Application – FEXT, AF7,AF8_BG5,BG6

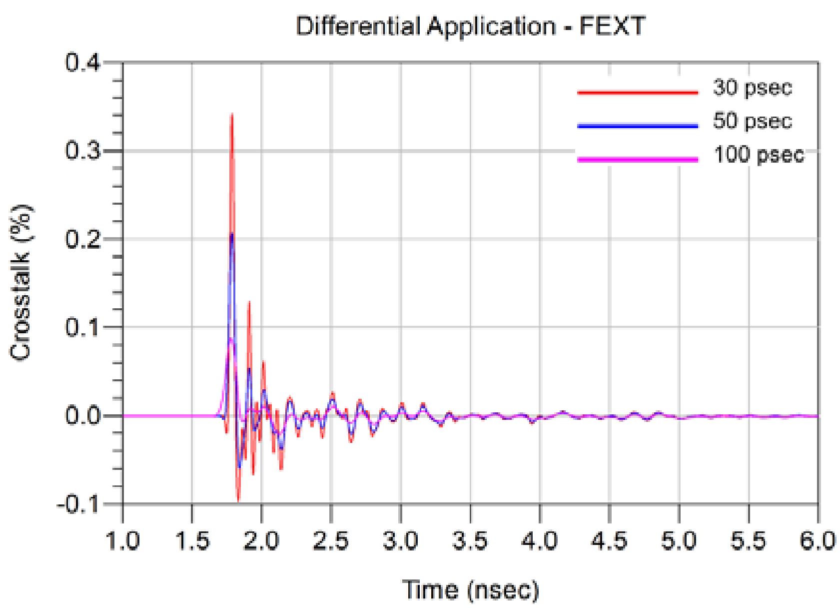


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff Optimal Vertical Application – NEXT, AG5,AH5_AG7,AH7

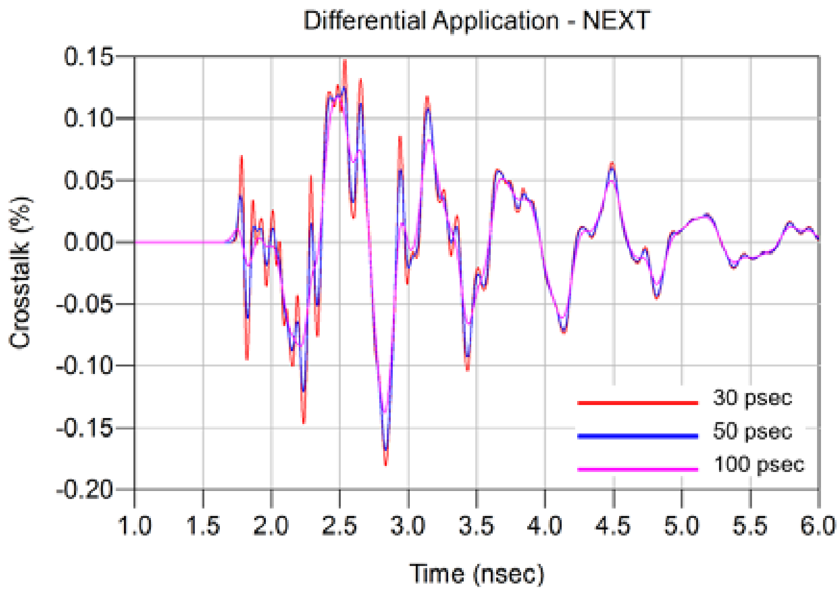


Diff Optimal Vertical Application – FEXT, AG5,AH5_BG7,BH7

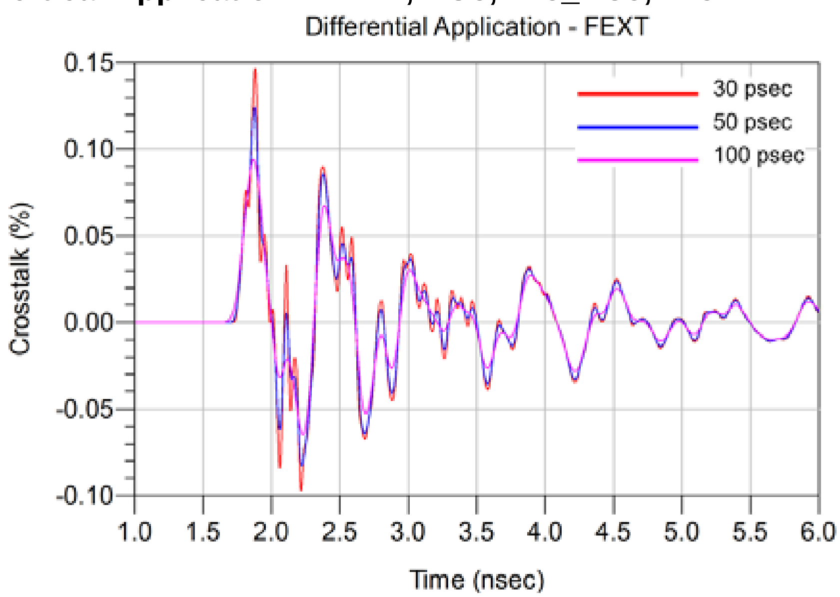


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff Optimal Vertical Application – NEXT, AG5,AH5_AC5,AD5

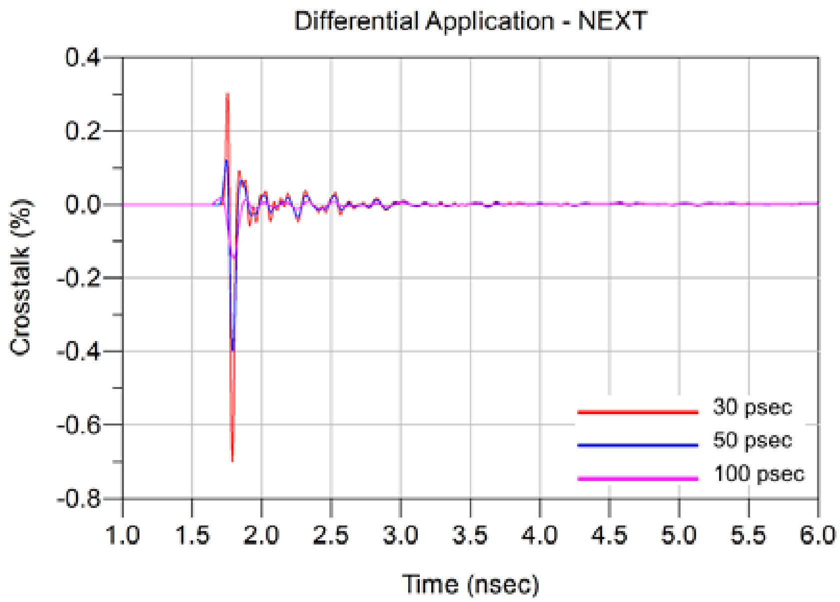


Diff Optimal Vertical Application – FEXT, AG5,AH5_BC5,BD5

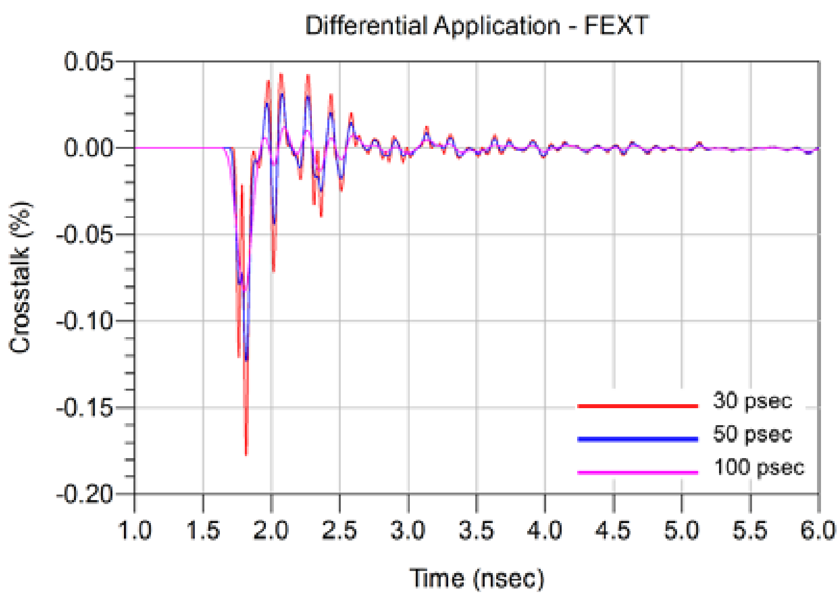


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff Optimal Vertical Application – NEXT, AG5,AH5_AE4,AF4

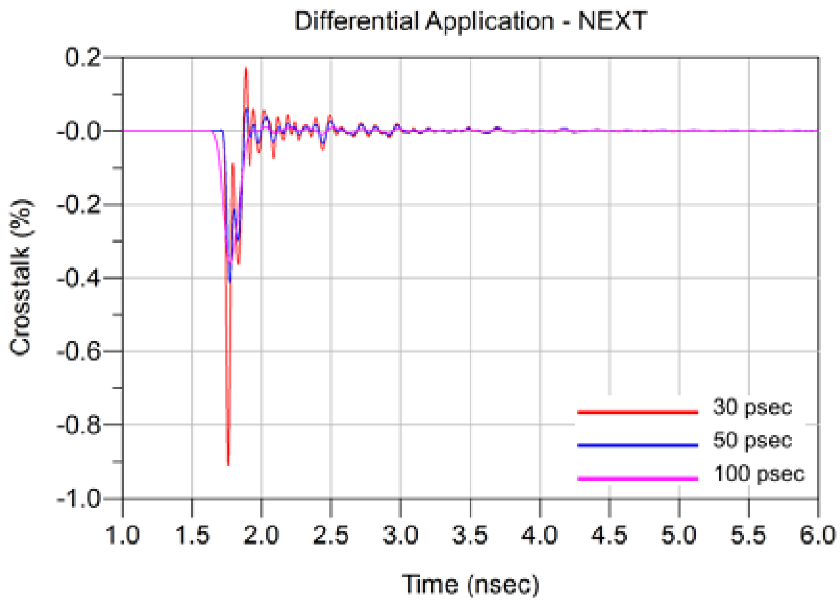


Diff Optimal Vertical Application – FEXT, AG5,AH5_BE4,BF4

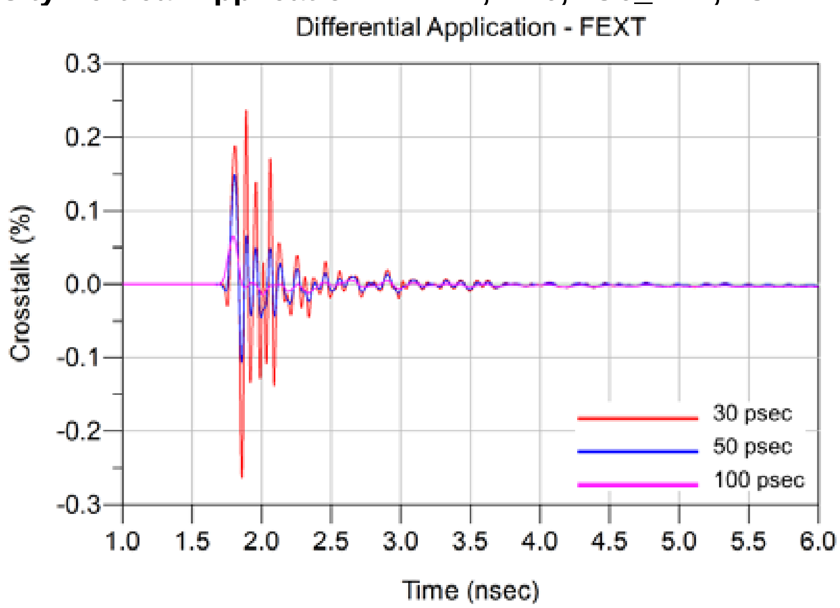


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff High Density Vertical Application – NEXT, AF6,AG6_AF4,AG4

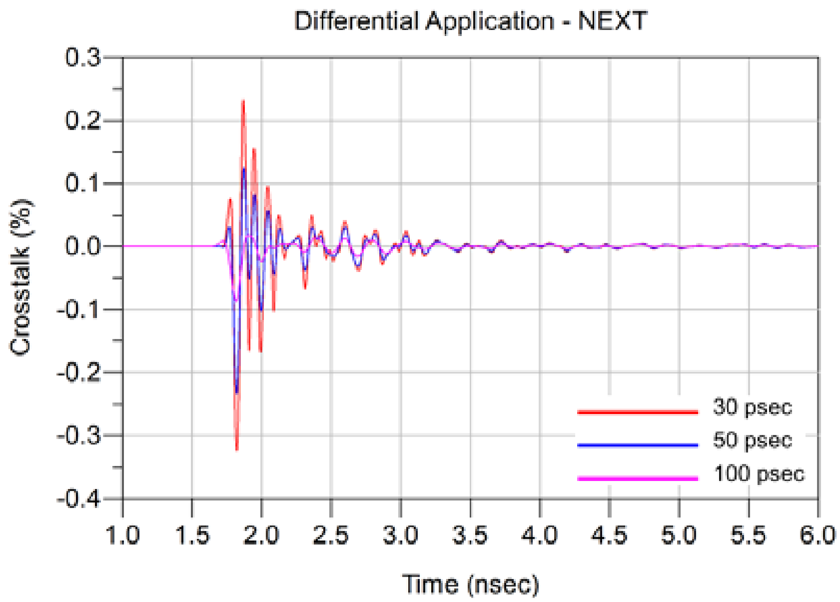


Diff High Density Vertical Application – FEXT, AF6,AG6_BF4,BG4

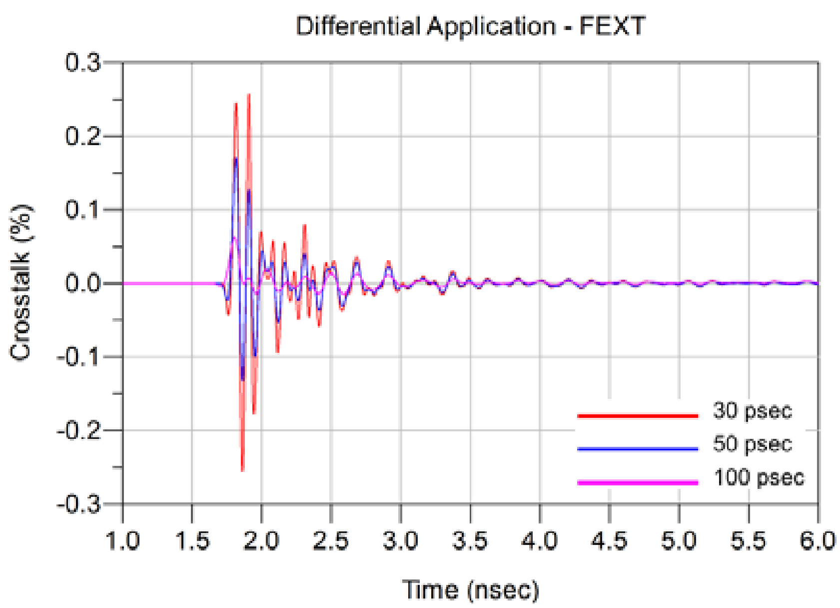


Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff High Density Vertical Application – NEXT, AF6,AG6_AC6,AD6



Diff High Density Vertical Application – FEXT, AF6,AG6_BC6,BD6



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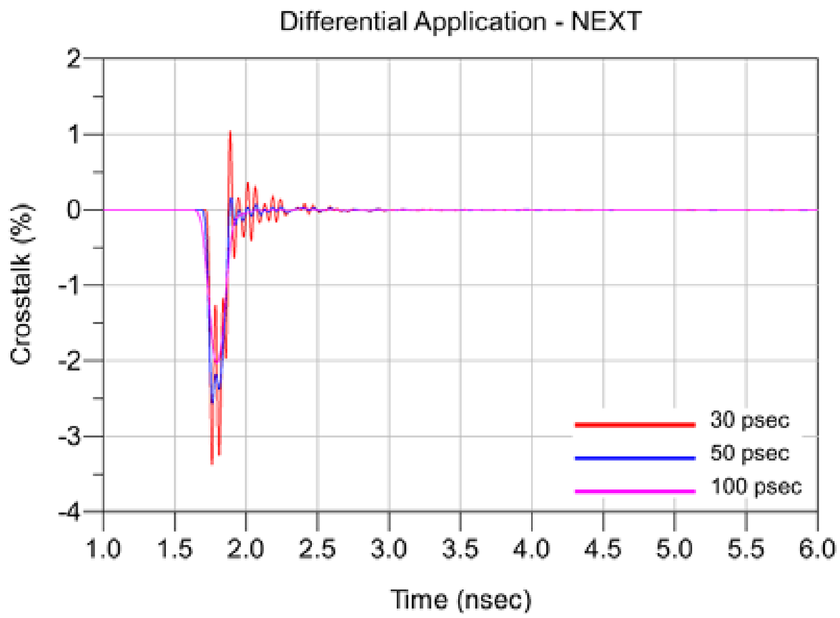
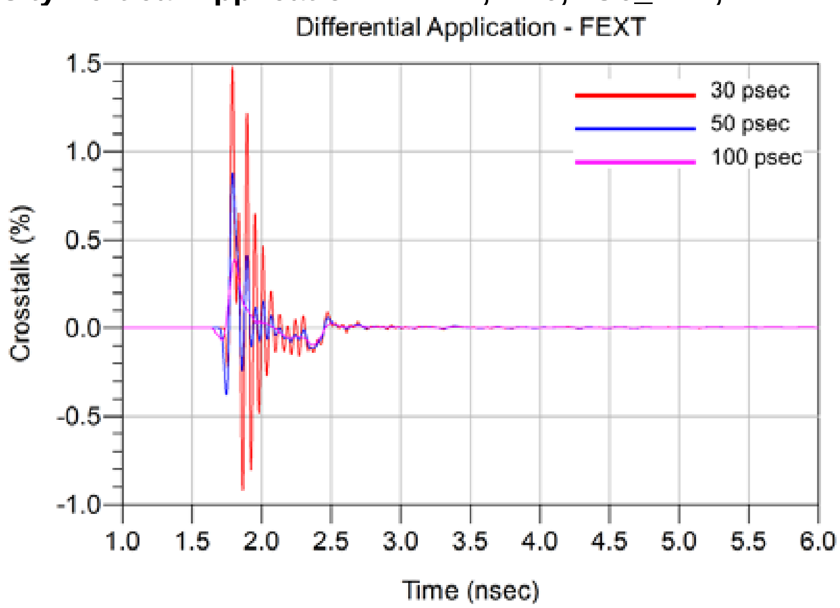
Report Revision: 9/11/2015

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Diff High Density Vertical Application – NEXT, AF6,AG6_AE7,AF7



Diff High Density Vertical Application – FEXT, AF6,AG6_BE7,BF7



Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Appendix C – Product and Test System Descriptions

Product Description

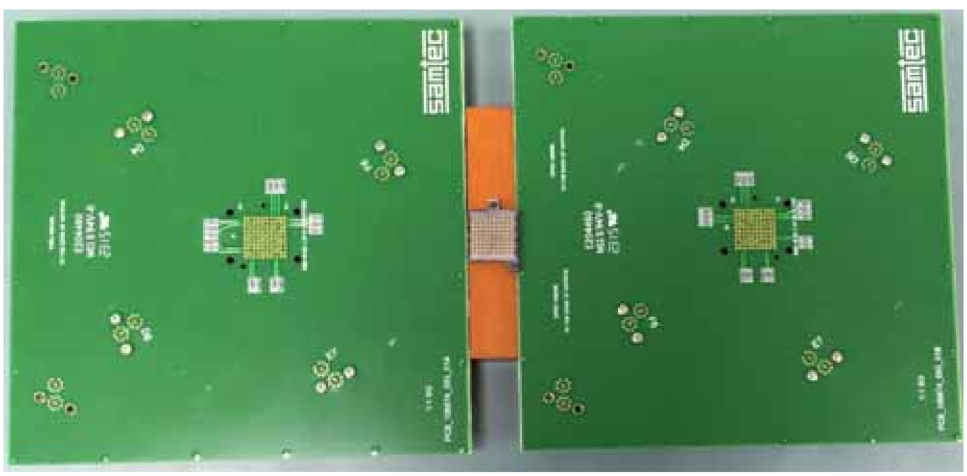
Product test samples are 1.27mm stack height GMI Series connectors. The part number is GMI-10-2-1.27-G-10. The GMI Series is a low profile one piece array connector designed for single-ended signals with various options for differential signaling configurations. The one piece array is 10 row providing 10 signal pins per row. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Ten test fixtures are specific to the GMI Series connector set and identified by part numbers PCB-106874-SIG-01A and B to PCB-106874-SIG-05A and B. Calibration standards specific to the GMI Series are located on the test boards. To keep trace lengths short, five different test board sets were required to access the necessary signal pins.

PCB-106874-SIG-XX Test Fixtures

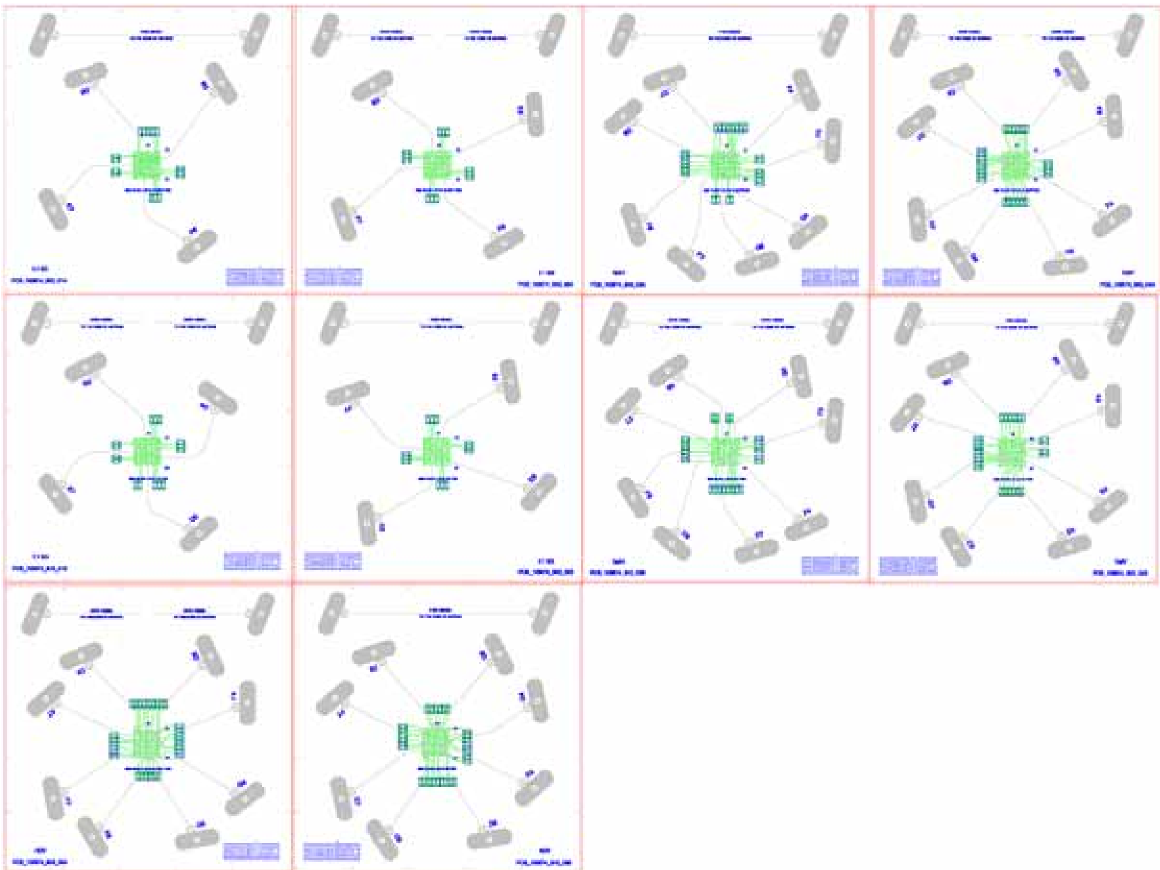
Shown below is a photograph of one of the five test board sets together with the GMI connector. The calibration standards were combined on the test boards.



Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

PCB-106874-SIG-XX PCB Layout Panel

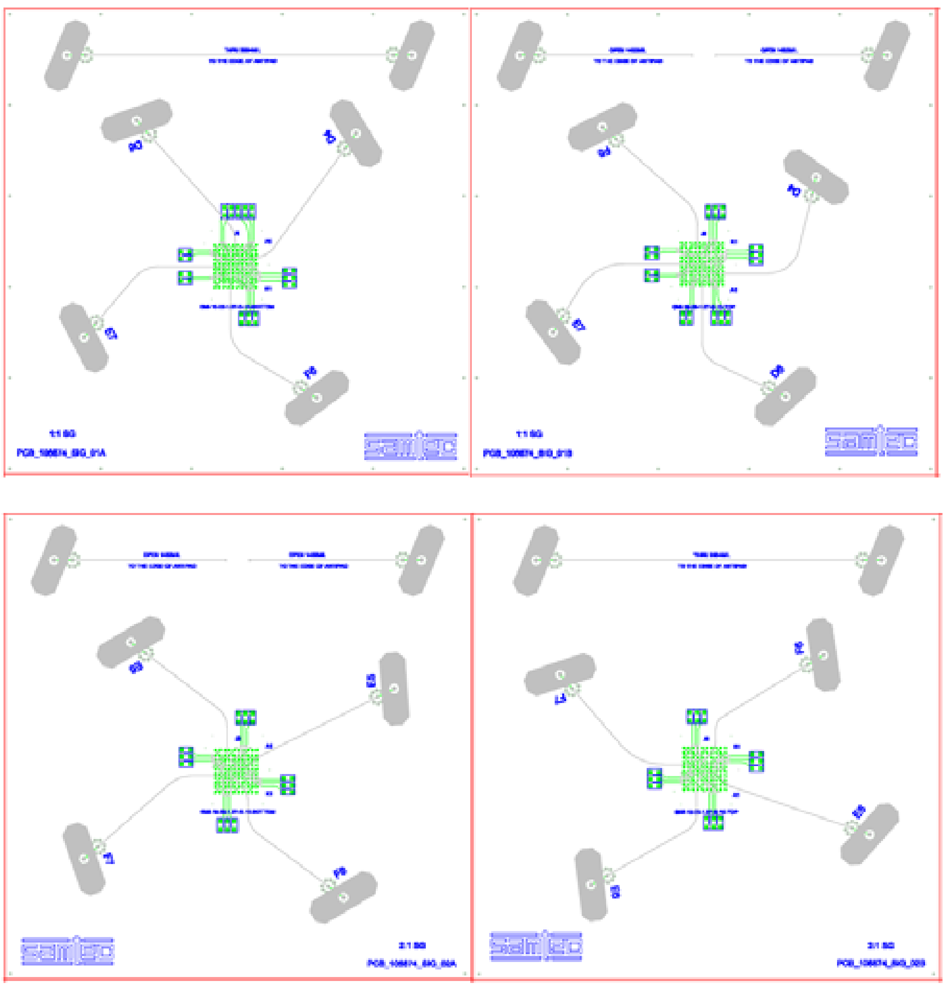
Artwork of the PCB design is shown below.



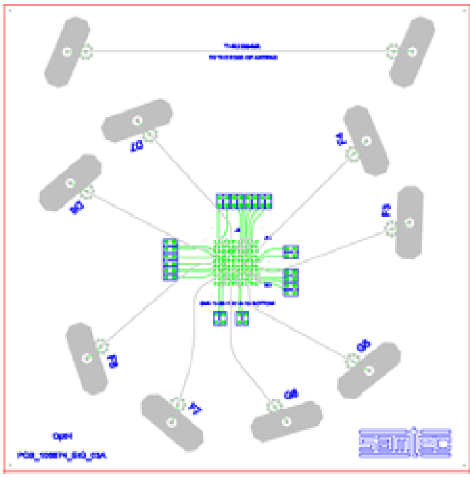
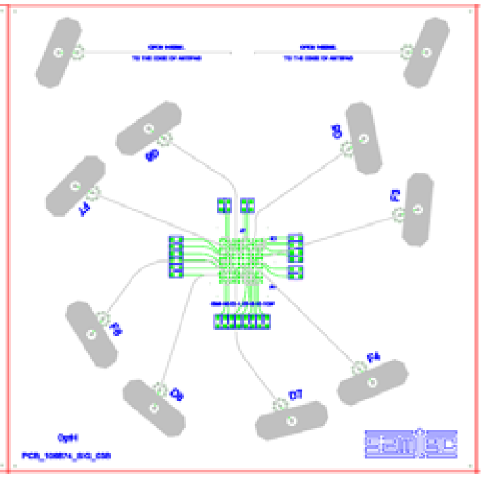
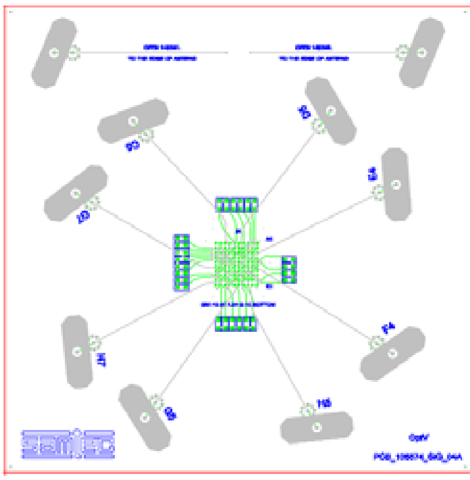
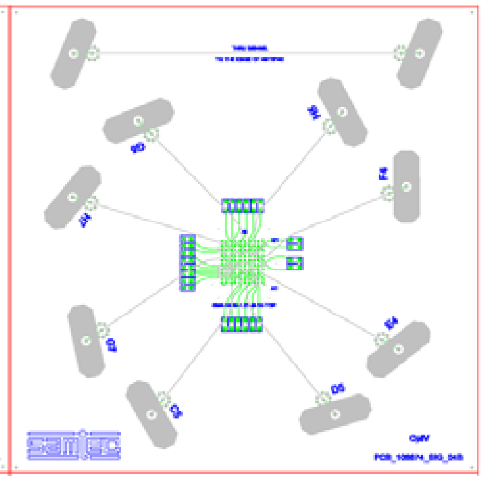
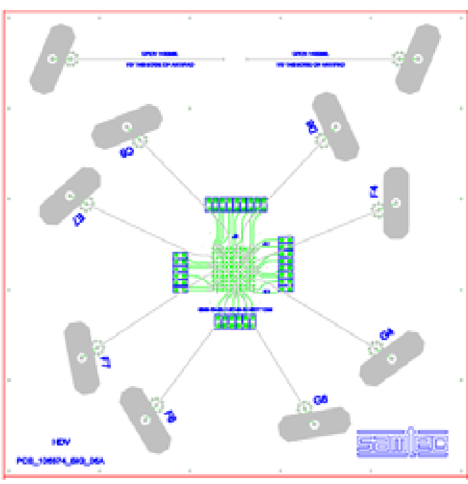
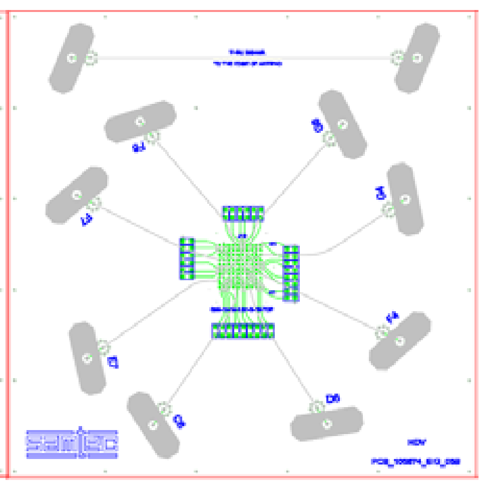
PCB Fixtures

The test fixtures used are as follows:

PCB-106874-SIG-01A – GMI Series Test Board for SE 1:1 S/G Pattern
PCB-106874-SIG-01B – GMI Series Test Board for SE 1:1 S/G Pattern
PCB-106874-SIG-02A – GMI Series Test Board for SE 2:1 S/G Pattern
PCB-106874-SIG-02B – GMI Series Test Board for SE 2:1 S/G Pattern
PCB-106874-SIG-03A – GMI Series Test Board for Differential Optimal Horizontal
PCB-106874-SIG-03B – GMI Series Test Board for Differential Optimal Horizontal
PCB-106874-SIG-04A – GMI Series Test Board for Differential Optimal Vertical
PCB-106874-SIG-04B – GMI Series Test Board for Differential Optimal Vertical
PCB-106874-SIG-05A – GMI Series Test Board for Differential High Density Vertical
PCB-106874-SIG-05B – GMI Series Test Board for Differential High Density Vertical



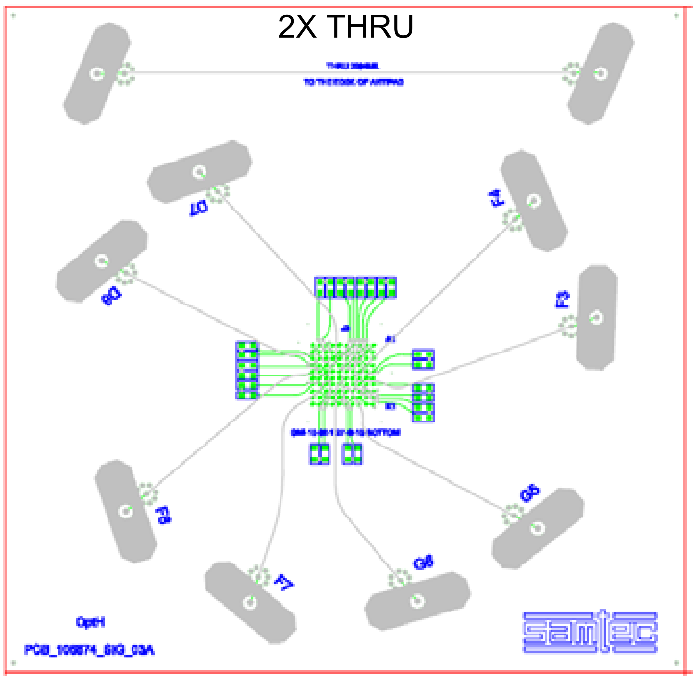
Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Calibration Board

Test fixture losses and test point reflections were removed from the data by use of Automatic Fixture Removal (AFR) application. The calibration board is shown below. It locates on the test boards. The measurements were performed under SOLT calibration and the test board effects were included in the measurements. AFR application extracts fixture S-parameters from 2X THRU measurement and performs de-embedding on the DUT+Fixture measurement to characterize only the DUT.



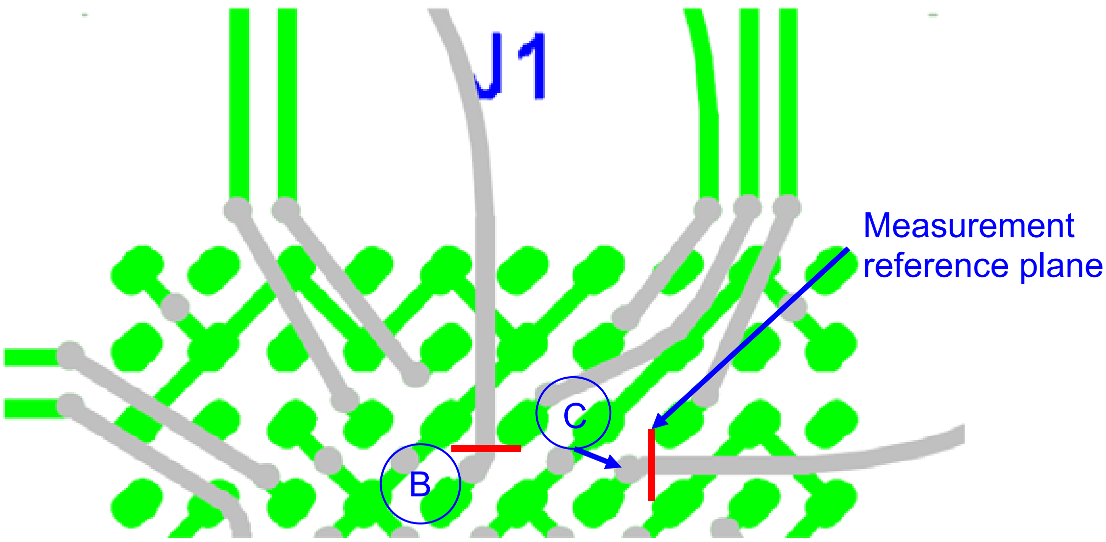
Thru line – 2964 mils

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

All traces on the test boards are length matched to 1.5" measured from the edge of the pad to the SMA. The AFR application effectively removes 1.482" of test board trace effects. This means that 18 mils of test board trace length effects are included in the measurement. The S-Parameter measurement includes:

A- The GMI Series connector
B- Test board vias and pads (footprint effects)
C- 18 mils of 9.5mil wide microstrip trace

The figure below shows the location of the measurement reference plane.



Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

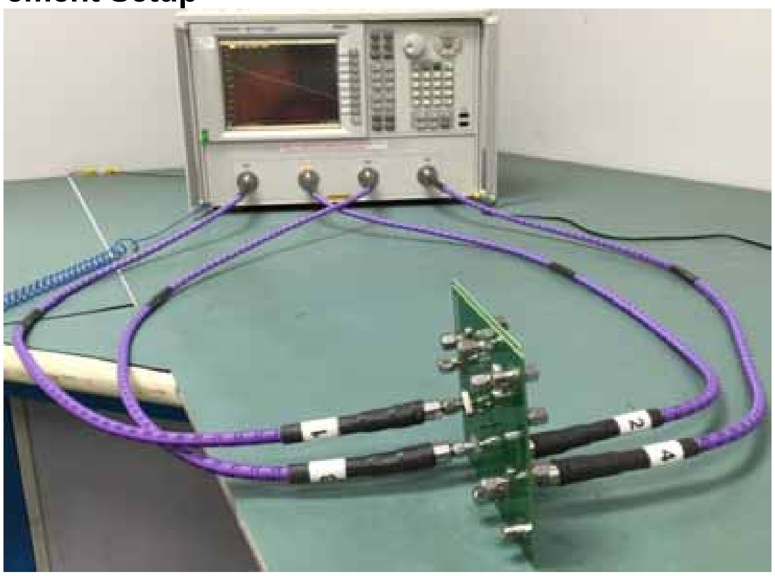
Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are extracted from the instrument by AFR application. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz
Stop Frequency – 20 GHz
Number of points -1601
IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ECAL Module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

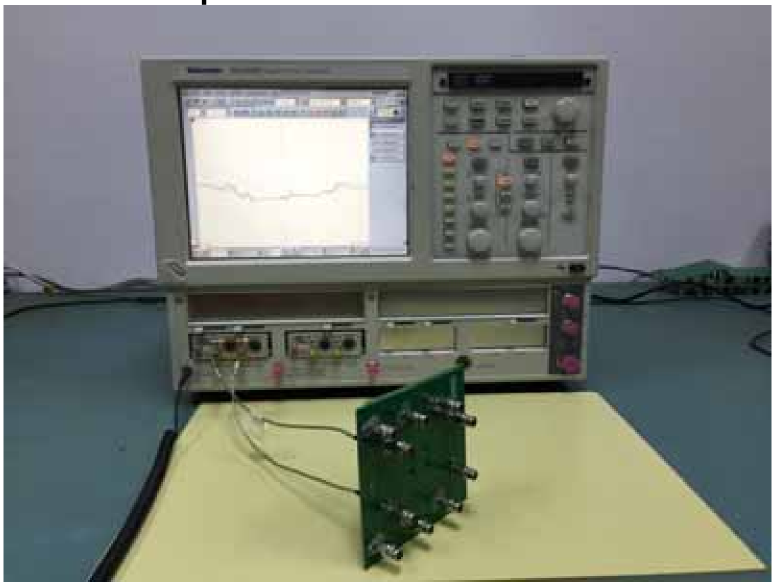
Phone: 812-944-6733
Fax: 812-948-5047

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

	Single-Ended Signal	Differential Signal
Vertical Scale:	5 ohm / Div:	5 ohm / Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	200ps/ Div	200ps/ Div
Record Length:	4000	4000
Averages:	≥ 16	≥ 16

DSA8200 Measurement Setup



Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the through calibration standards, the SI test boards, and the selection of the PCB vendor.

A coaxial SOLT calibration is performed using a N4433A ECAL module. Then DUT measurements are performed under SOLT calibration. The measurements include the effect of test fixture. The measurements of the 2X THRU line standards are required in order to remove the test fixture effect.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2009 update 1. This tool has a transient convolution simulator, which can generate a Time Domain response directly from the measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Near-End Crosstalk (TDT) & Far End Crosstalk (TDT)
A step pulse is applied to the touchstone model of the connector and the coupled voltage is monitored. The amplitude of the peak-coupled voltage is recorded and reported as a percentage of the input pulse.

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Impedance (TDR)

Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

Series: GMI
Description: Low Profile One Piece Array, 1.0mm x 1.0mm Grid, 1.27mm Stack Height

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
AFR – Automatic Fixture Removal
BC – Best Case crosstalk configuration
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
Z – Impedance (expressed in ohms)