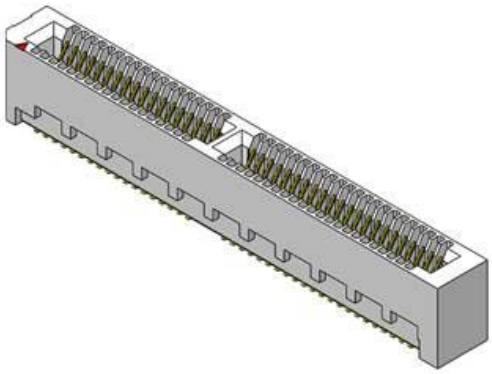
High Speed Characterization Report

HSEC1-XXX-01-X-DV-XX



Description:
Edge Rate® High-Speed Edge Card Connector, 1.0mm (.0394") Pitch, Accepts 1.60mm (.062") thick cards

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Report Revision: 6/19/2017
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Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

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Connector Overview

The HSEC1 series is a double row, edge-card connector on a 1.0mm (.0394") pitch and accepts .062" (1.60 mm) thick cards. At the time of testing, the HSEC1-DV maximum position count is 70 positions per row (140 pins). The data in this report is applicable to HSEC1-DV connector mated to 1.6mm thick card.

Frequency Domain Data Summary

Table 1 - Differential Connector System Performance (85 Ohm)			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	Edge-Card_53,55	HSEC1_53,55	3dB@ 18.6 GHz
Return Loss	Edge-Card_53,55	Edge-Card_53,55	>10dB to 12.9 GHz
Near-End Crosstalk	Edge-Card_53,55	Edge-Card_45,47	<-20dB to 20 GHz
	Edge-Card_53,55	Edge-Card_61,63	<-20dB to 20 GHz
	Edge-Card_53,55	Edge-Card_50.52	<-20dB to 20 GHz
	Edge-Card_53,55	Edge-Card_58,60	<-20dB to 20 GHz
Far-End Crosstalk	Edge-Card_53,55	HSEC1_45,47	<-20dB to 20 GHz
	Edge-Card_53,55	HSEC1_61,63	<-20dB to 20 GHz
	Edge-Card_53,55	HSEC1_50,52	<-20dB to 20 GHz
	Edge-Card_53,55	HSEC1_58,60	<-20dB to 20 GHz

PCIE (85 ohm) Pin Map:

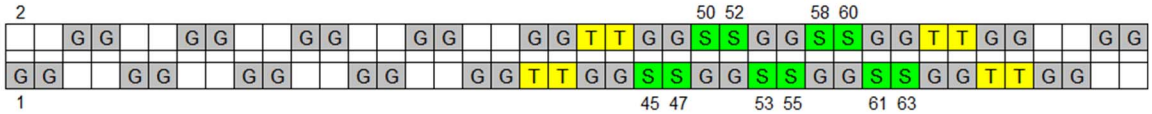

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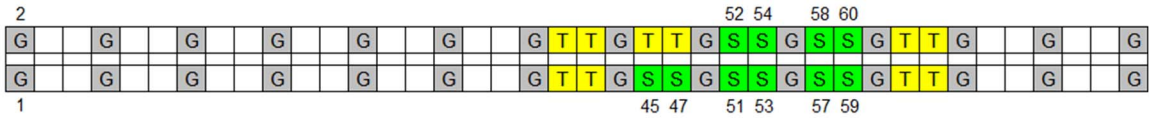
Table 2 - Differential Connector System Performance (100 Ohm)			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	Edge-Card_51,53	HSEC1_51,53	3dB@ 17.1 GHz
Return Loss	Edge-Card_51,53	Edge-Card_51,53	>10dB to 13.0 GHz
Near-End Crosstalk	Edge-Card_51,53	Edge-Card_45,47	<-20dB to 20 GHz
	Edge-Card_51,53	Edge-Card_57,59	<-20dB to 20 GHz
	Edge-Card_51,53	Edge-Card_52,54	<-20dB to 20 GHz
	Edge-Card_51,53	Edge-Card_58.60	<-20dB to 20 GHz
Far-End Crosstalk	Edge-Card_51,53	HSEC1_45,47	<-20dB to 20 GHz
	Edge-Card_51,53	HSEC1_57,59	<-20dB to 20 GHz
	Edge-Card_51,53	HSEC1_52,54	<-20dB to 20 GHz
	Edge-Card_51,53	HSEC1_58,60	<-20dB to 20 GHz

SAS (100 ohm) Pin Map:



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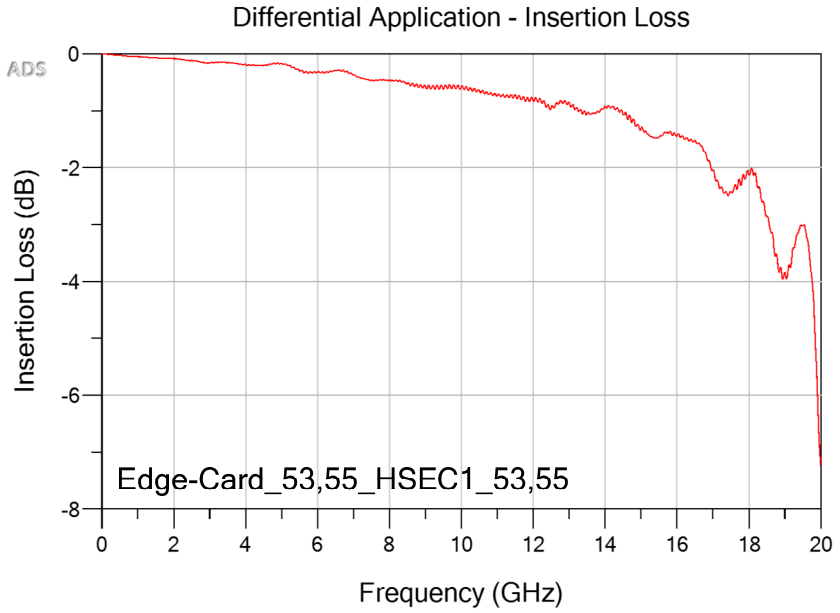
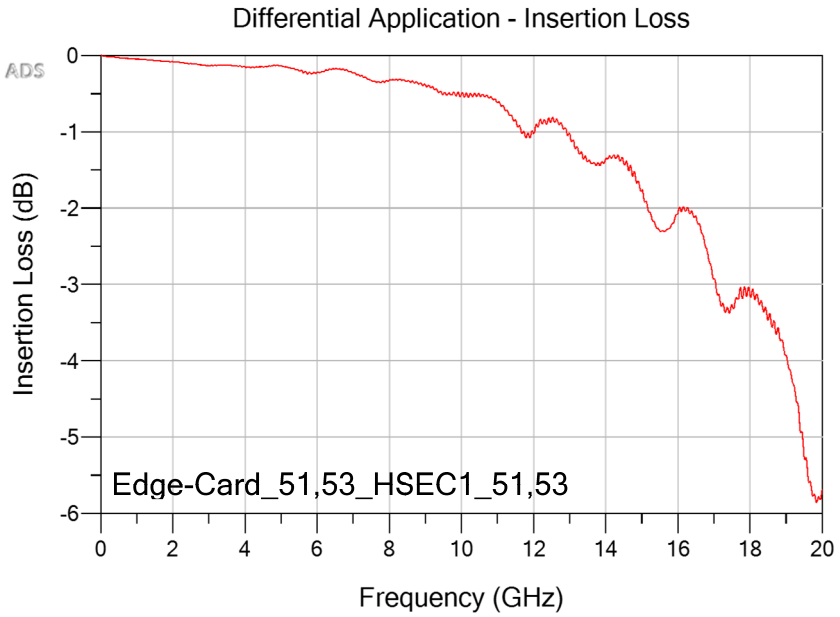
Bandwidth Chart – Differential Insertion Loss

HSEC1 Connector Series
85Ohm



100Ohm



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Time Domain Data Summary

Table 3 - Differential Impedance (Ω)-85 Ohm					
Signal Rise-time	**30ps**	**50ps**	**100ps**	**250ps**	**500ps**
Maximum Impedance	94.3	92.2	88.0	83.3	82.5
Minimum Impedance	78.5	78.5	78.5	78.7	80.5

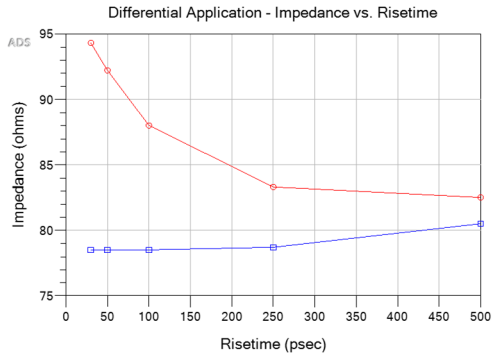

Table 4 - Differential Impedance (Ω)-100 Ohm					
Signal Rise-time	**30ps**	**50ps**	**100ps**	**250ps**	**500ps**
Maximum Impedance	97.7	96.1	94.0	92.8	93.7
Minimum Impedance	90.2	91.0	91.5	91.6	92.1

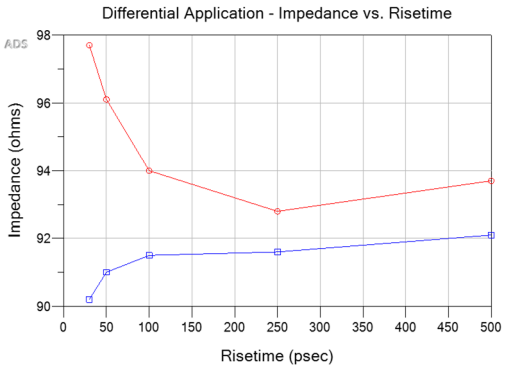

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	Table 5 - Differential Crosstalk (%) - 85 Ohm					
Input(t_r)	**Driver**	**Receiver**	**30ps**	**50ps**	**100ps**	**250ps**
NEXT	Edge-Card_53,55	Edge-Card_45,47	0.18	0.10	<0.1	<0.1
	Edge-Card_53,55	Edge-Card_61,63	0.17	0.10	<0.1	<0.1
	Edge-Card_53,55	Edge-Card_50.52	0.60	0.44	0.24	0.10
	Edge-Card_53,55	Edge-Card_58,60	0.58	0.43	0.24	0.10
FEXT	Edge-Card_53,55	Edge-Card_45,47	0.37	0.25	0.12	<0.1
	Edge-Card_53,55	Edge-Card_61,63	0.36	0.25	0.12	<0.1
	Edge-Card_53,55	Edge-Card_50.52	0.14	<0.1	<0.1	<0.1
	Edge-Card_53,55	Edge-Card_58,60	0.11	<0.1	<0.1	<0.1

	Table 6 - Differential Crosstalk (%) - 100 Ohm					
Input(t_r)	**Driver**	**Receiver**	**30ps**	**50ps**	**100ps**	**250ps**
NEXT	Edge-Card_51,53	Edge-Card_45,47	0.48	0.36	0.25	0.12
	Edge-Card_51,53	Edge-Card_57,59	0.48	0.35	0.25	0.12
	Edge-Card_51,53	Edge-Card_52,54	1.46	1.15	0.64	0.27
	Edge-Card_51,53	Edge-Card_58.60	0.19	0.14	<0.1	<0.1
FEXT	Edge-Card_51,53	HSEC1_45,47	0.60	0.42	0.20	<0.1
	Edge-Card_51,53	HSEC1_57,59	0.58	0.41	0.19	0.11
	Edge-Card_51,53	HSEC1_52,54	0.37	0.25	<0.1	<0.1
	Edge-Card_51,53	HSEC1_58,60	<0.1	<0.1	<0.1	<0.1

Table 7 - Propagation Delay (Mated Connector)	
Differential (85 Ohm)	49 ps
Differential (100 Ohm)	44 ps

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Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for differentially driven scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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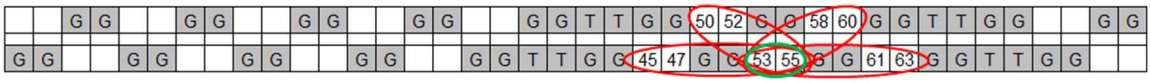
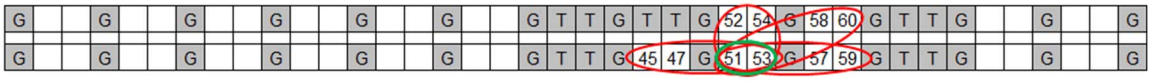
For this connector, the following array configurations were evaluated:

85 Ohm use “GGSSGGSSGG” PCIe pin configuration



100 Ohm use “GSSGSSG” pin configuration



Differential Impedance (denoted by green circles)**:**

- 85 Ohm use “GGSSGGSSGG” PCIe pin configuration
- 100 Ohm use “GSSGSSG” pin configuration

Differential Crosstalk (denoted by red circles)**:**

- 85 Ohm use “GGSSGGSSGG” PCIe pin configuration
- 100 Ohm use “GSSGSSG” pin configuration

Only one differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

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Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate the worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data
Frequency Domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data
Time Domain parameters indicate impedance mismatch versus length, signal propagation time and crosstalk in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix B of this report.

The measured S-Parameters from the network analyzer are post-processed using Keysight Advanced Design System to obtain the time domain response for signal propagation time and crosstalk. The Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 10 mils of PCB trace on the HSEC1 con-

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nector and Edge Card side each. Delay is measured at 100 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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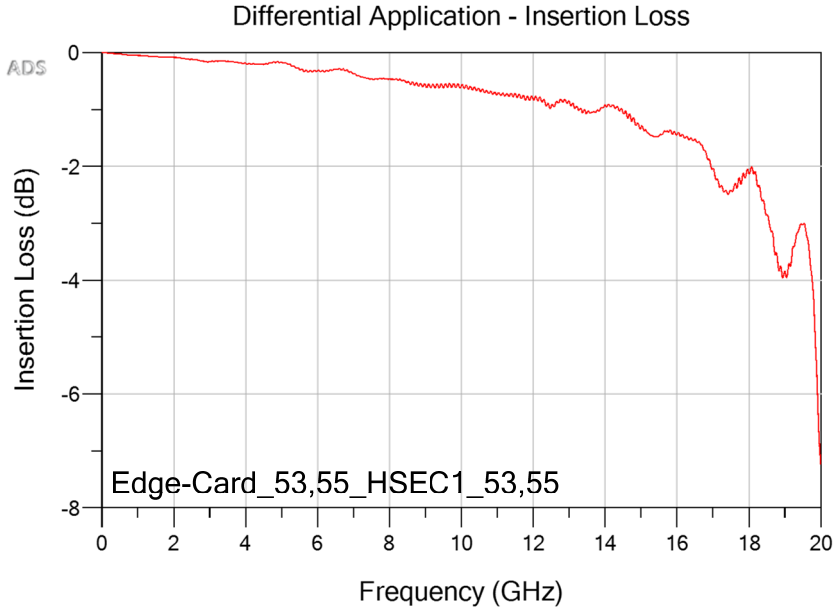
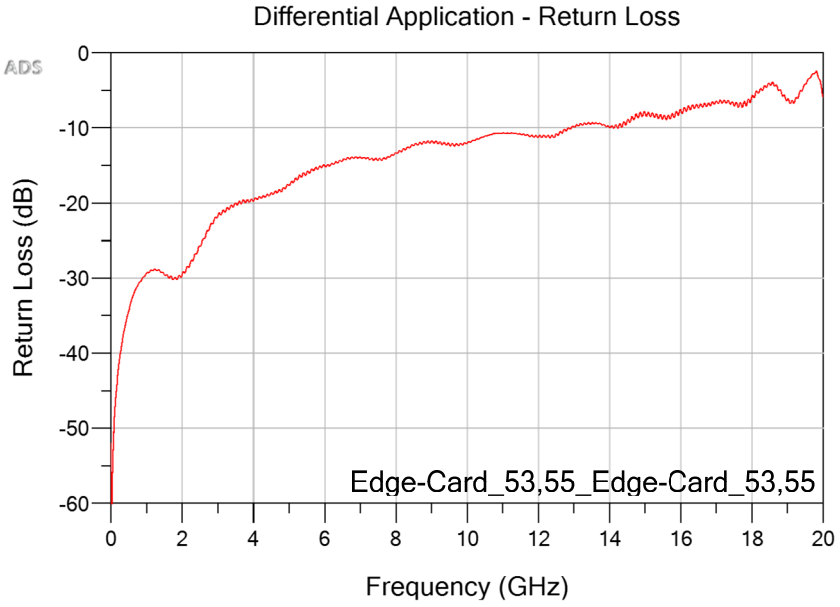
Appendix A – Frequency Domain Response Graphs

Differential Application (85 Ohm) – Insertion Loss



Differential Application (85 Ohm) – Return Loss



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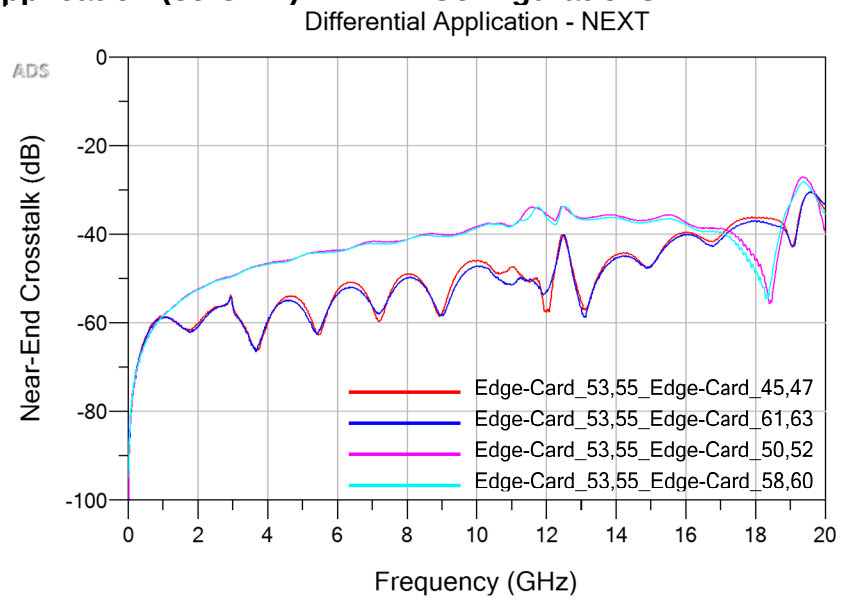
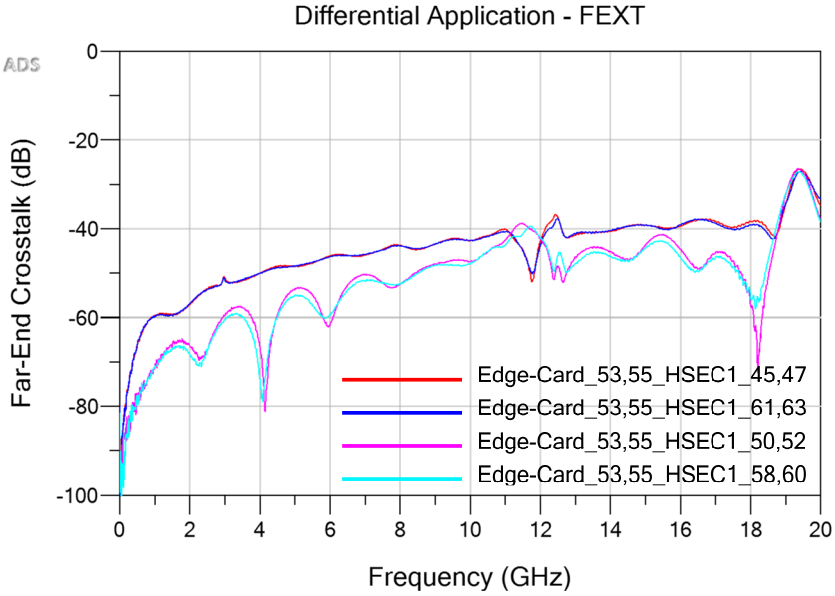
Differential Application (85 Ohm) – NEXT Configurations



Differential Application (85 Ohm) – FEXT Configurations



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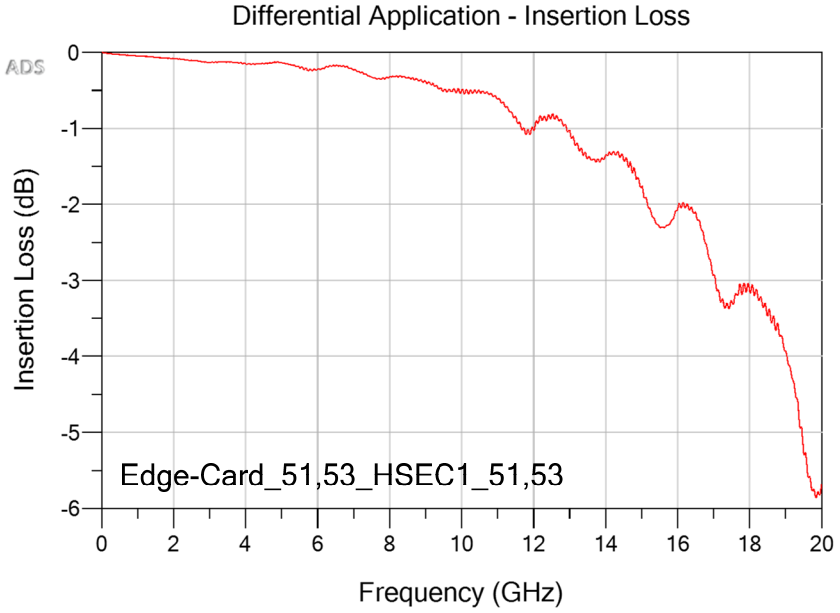
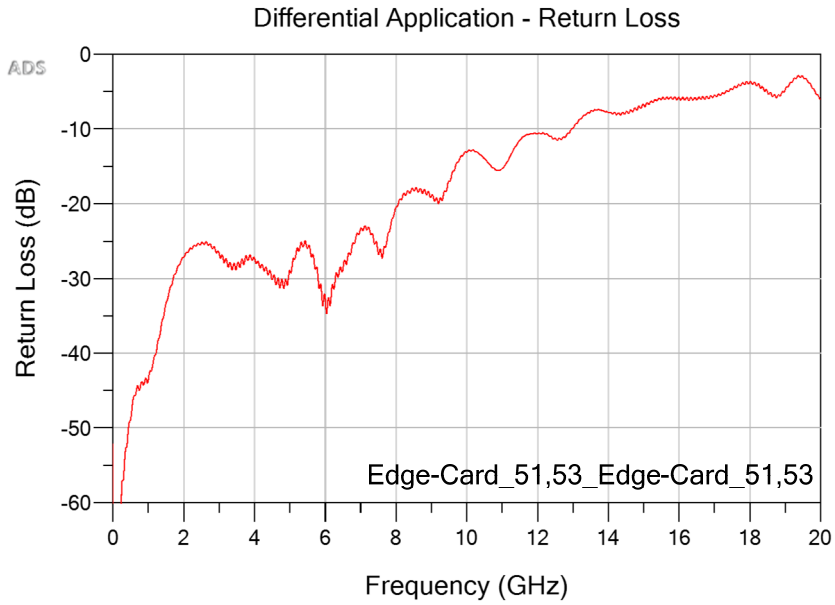
Differential Application (100 Ohm) – Insertion Loss



Differential Application (100 Ohm) – Return Loss



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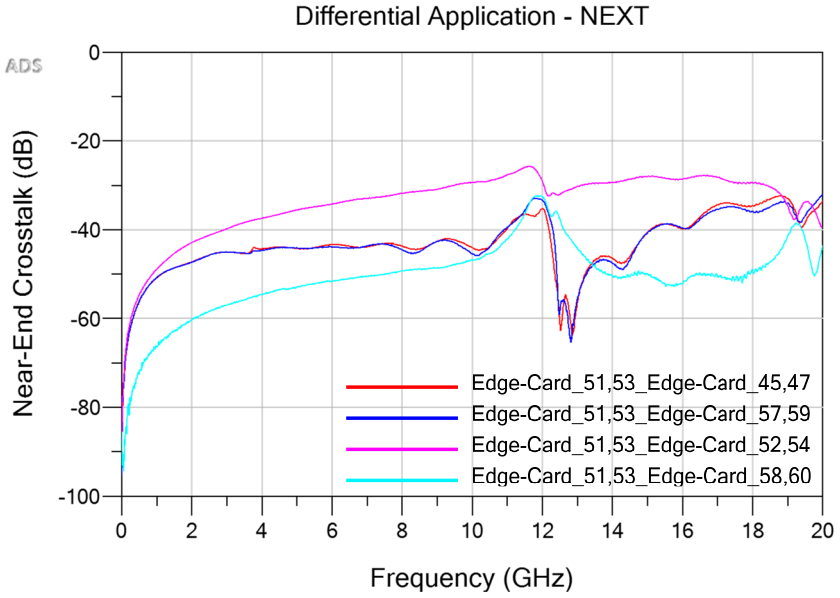
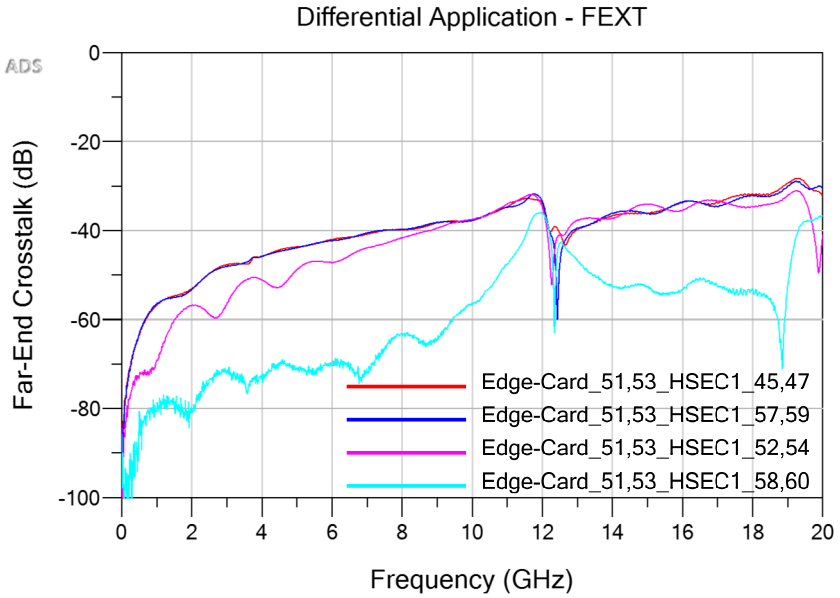
Differential Application (100 Ohm) – NEXT Configurations



Differential Application (100 Ohm) – FEXT Configurations



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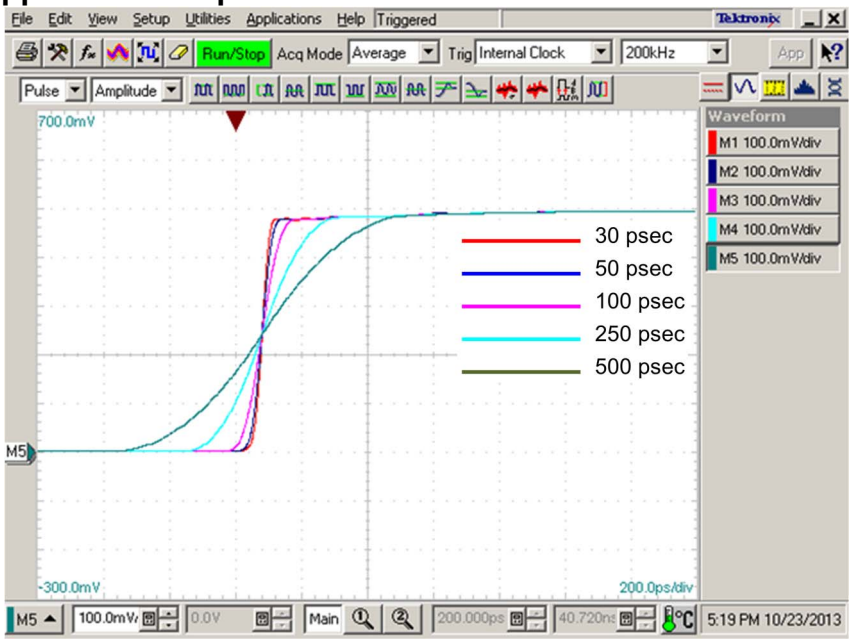
Appendix B – Time Domain Response Graphs

Differential Application – Input Pulse



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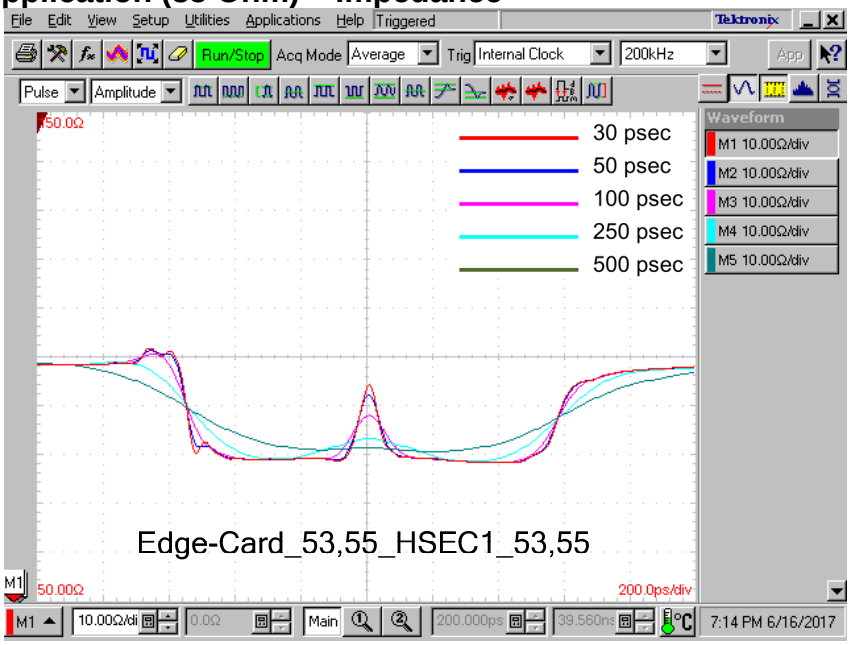
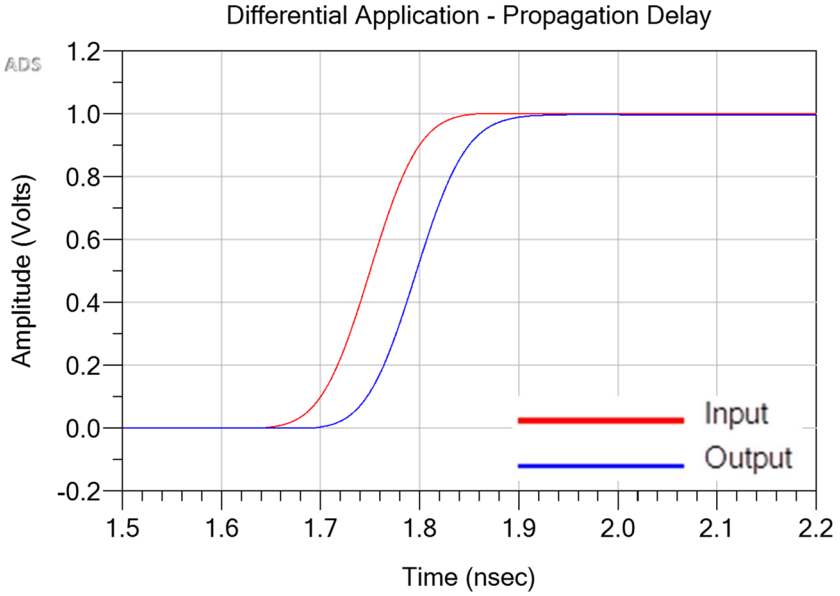
Differential Application (85 Ohm) – Impedance



Differential Application (85 Ohm) – Propagation Delay



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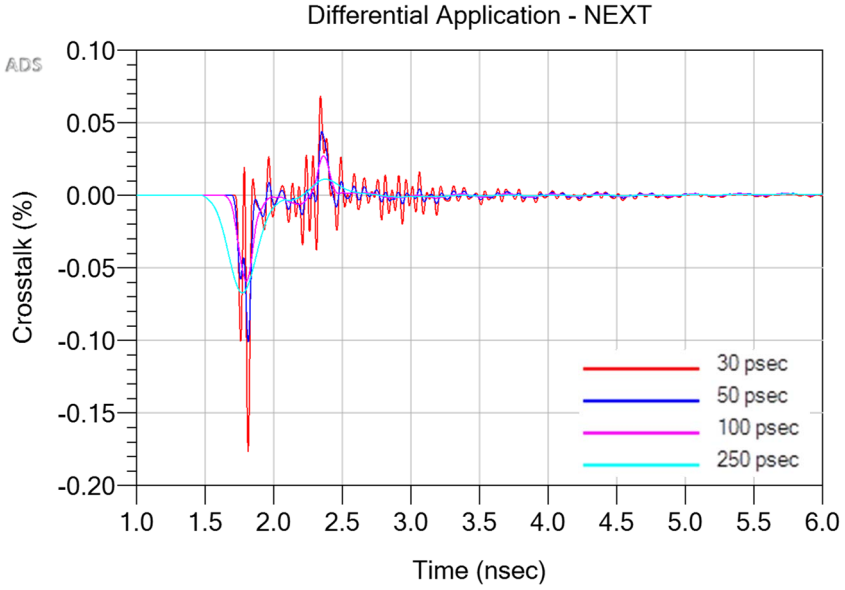
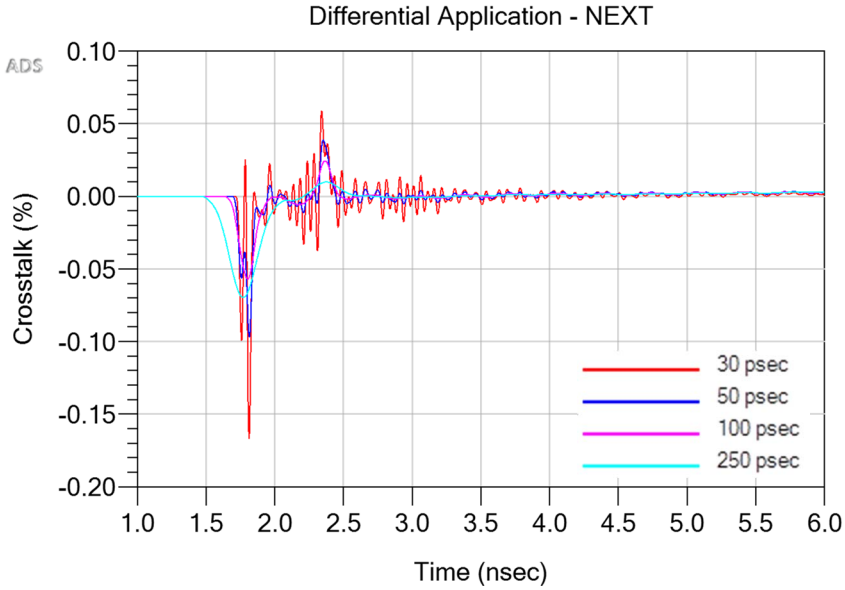
Differential Application (85 Ohm) – NEXT, Edge-Card_53,55_Edge-Card_45,47



Differential Application (85 Ohm) – NEXT, Edge-Card_53,55_Edge-Card_61,63



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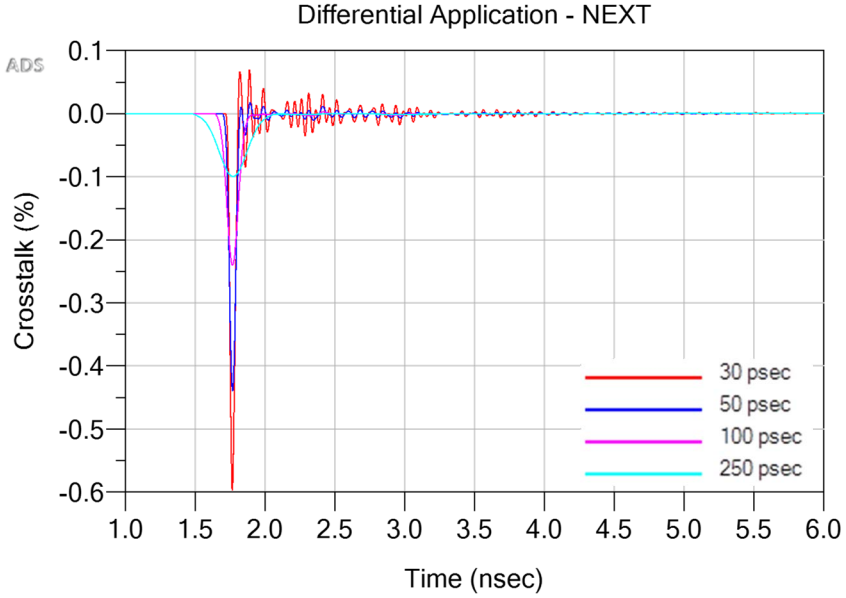
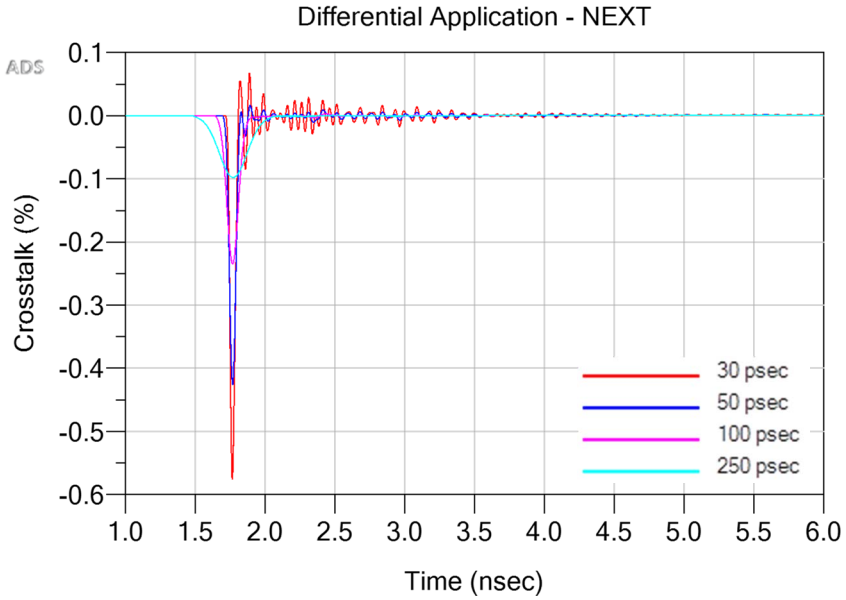
Differential Application (85 Ohm) – NEXT, Edge-Card_53,55_Edge-Card_50,52



Differential Application (85 Ohm) – NEXT, Edge-Card_53,55_Edge-Card_58,60



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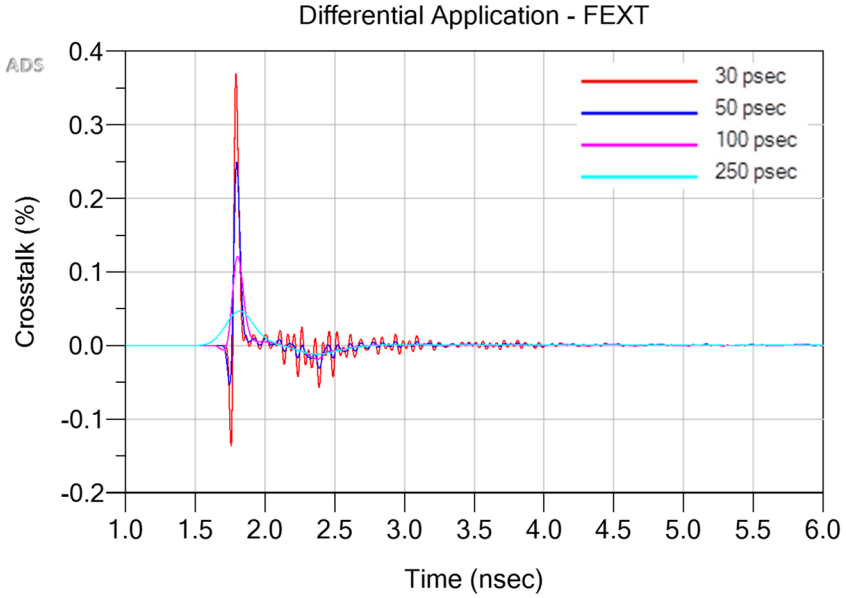
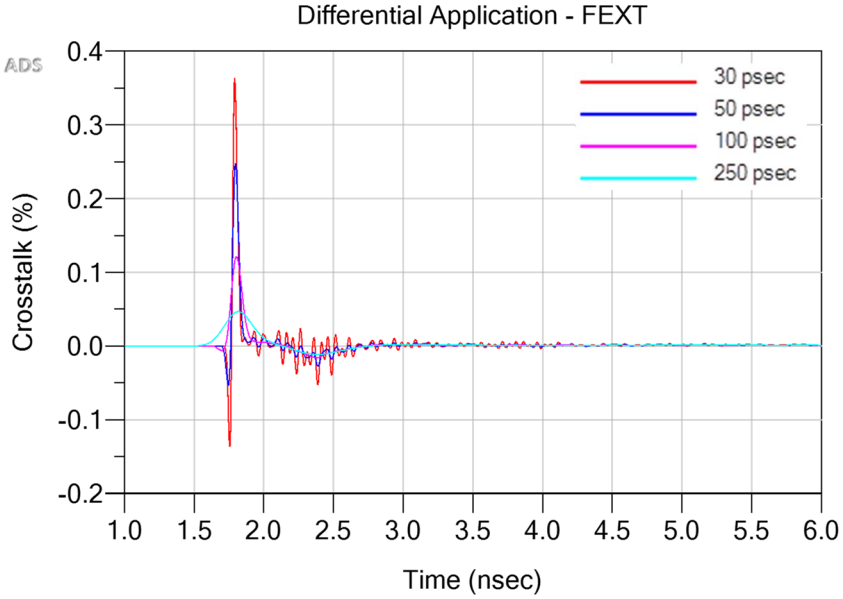
Differential Application (85 Ohm) – FEXT, Edge-Card_53,55_HSEC1_45,47



Differential Application (85 Ohm) – FEXT, Edge-Card_53,55_HSEC1_61,63



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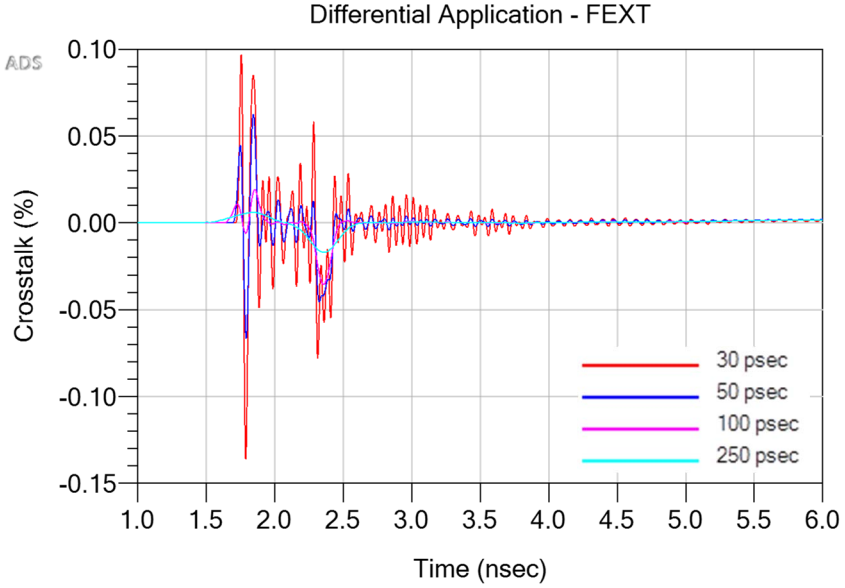
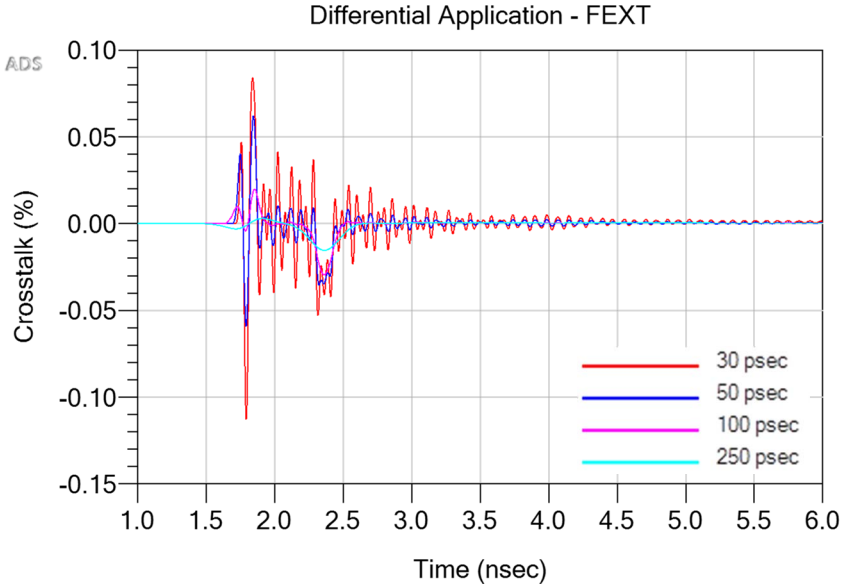
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Differential Application (85 Ohm) – FEXT, Edge-Card_53,55_HSEC1_50,52



Differential Application (85 Ohm) – FEXT, Edge-Card_53,55_HSEC1_58,60



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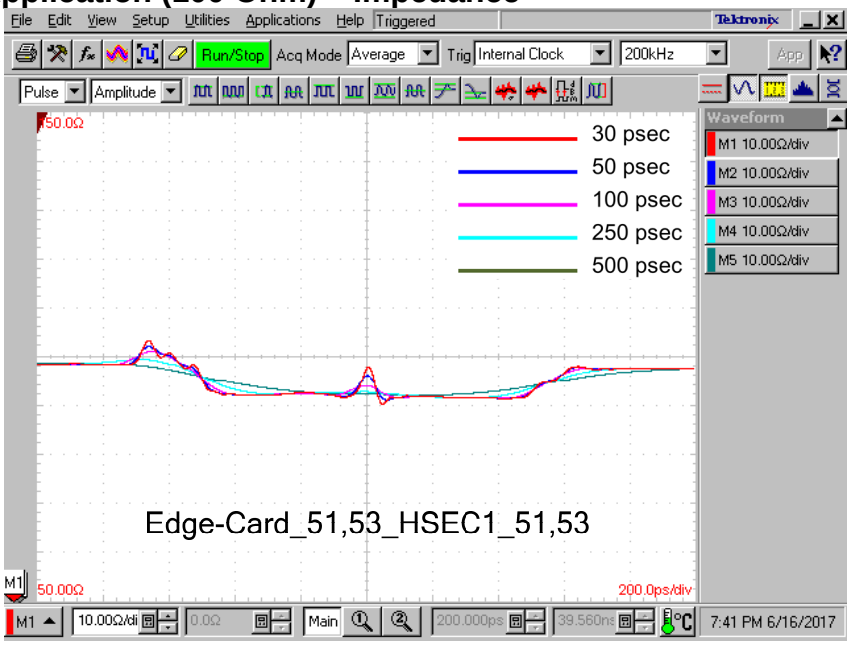
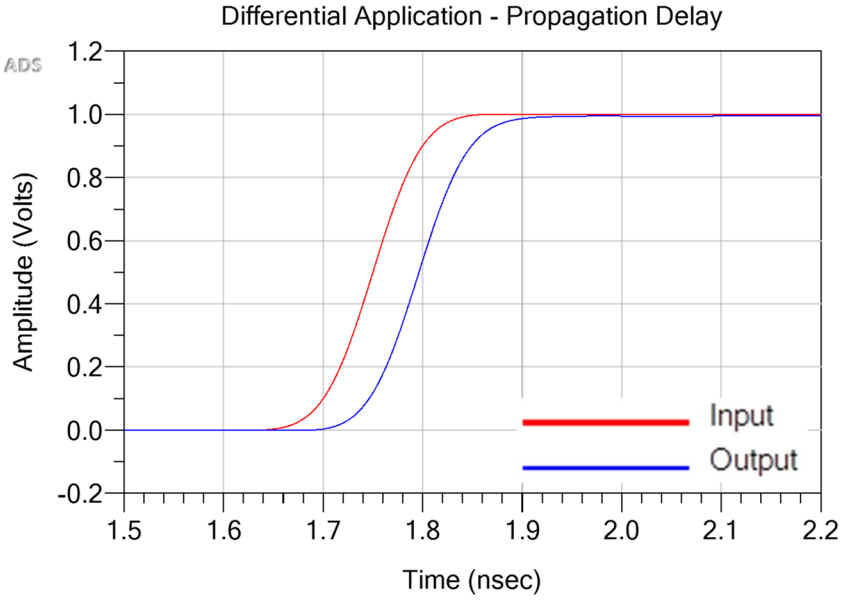
Differential Application (100 Ohm) – Impedance

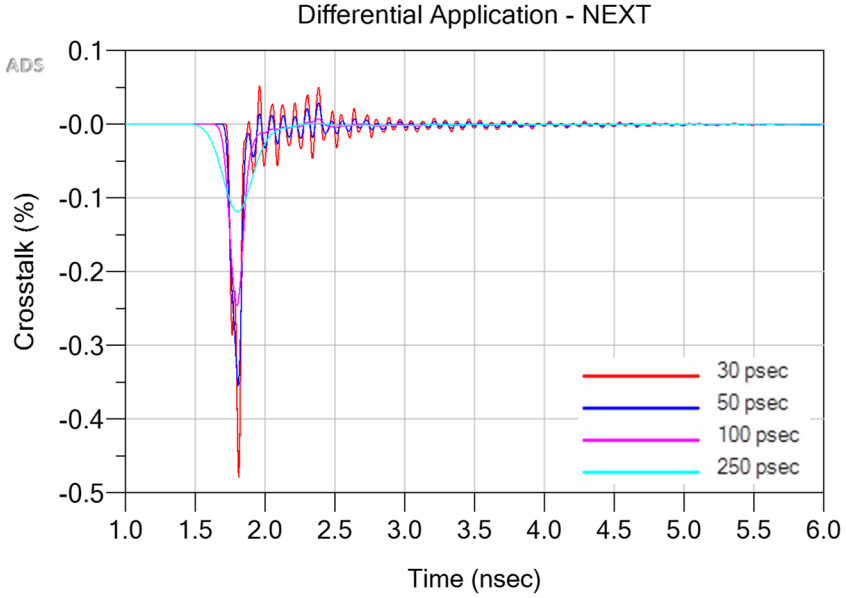


Differential Application (100 Ohm) – Propagation Delay

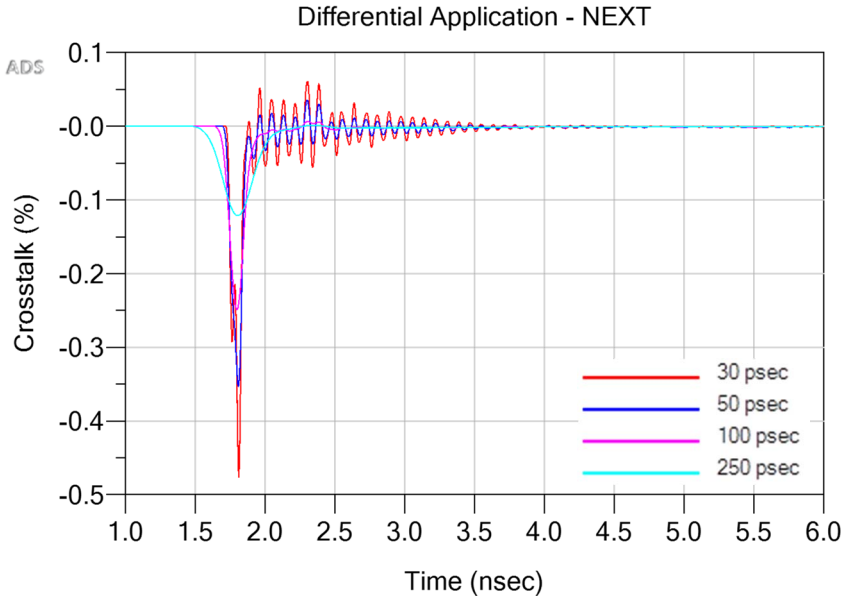


Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Differential Application (100 Ohm) – NEXT, Edge-Card_51,53_Edge-Card_45,47

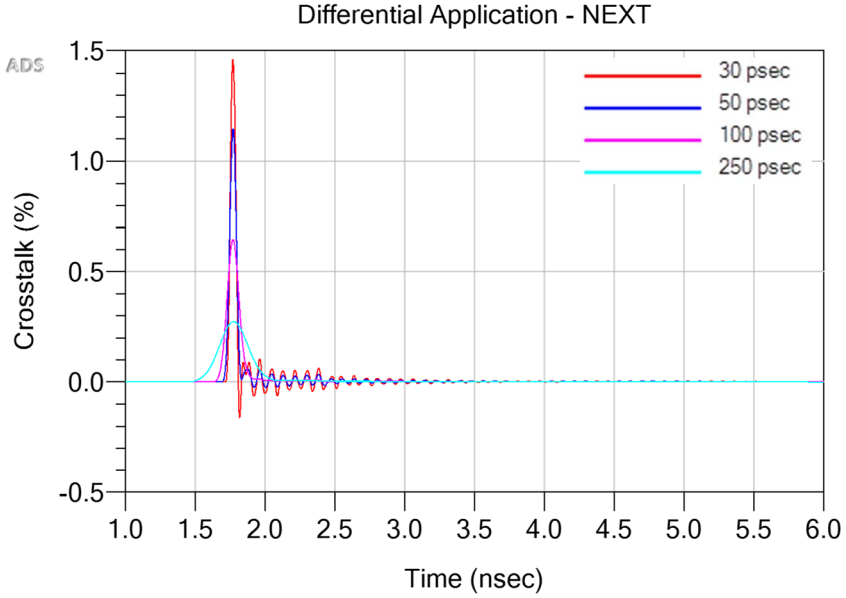


Differential Application (100 Ohm) – NEXT, Edge-Card_51,53_Edge-Card_57,59

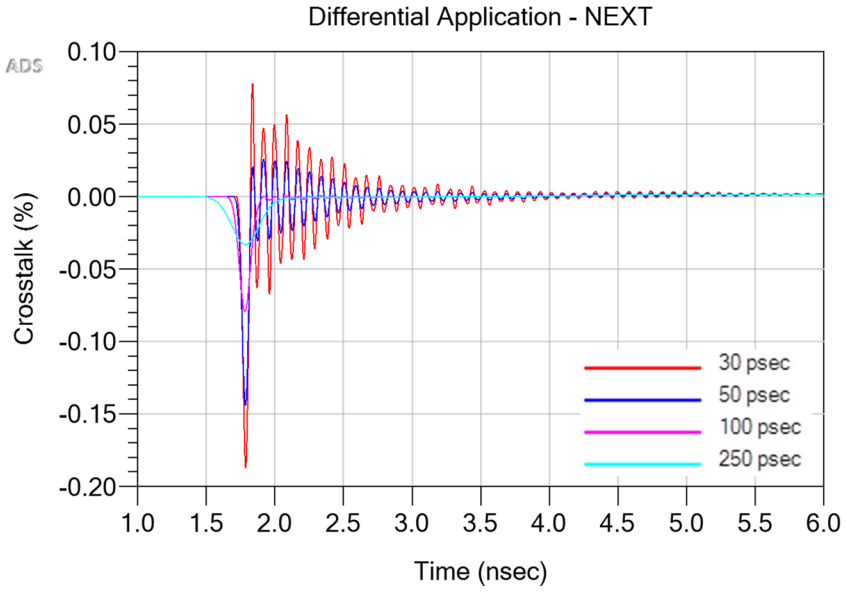


Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Differential Application (100 Ohm) – NEXT, Edge-Card_51,53_Edge-Card_52,54

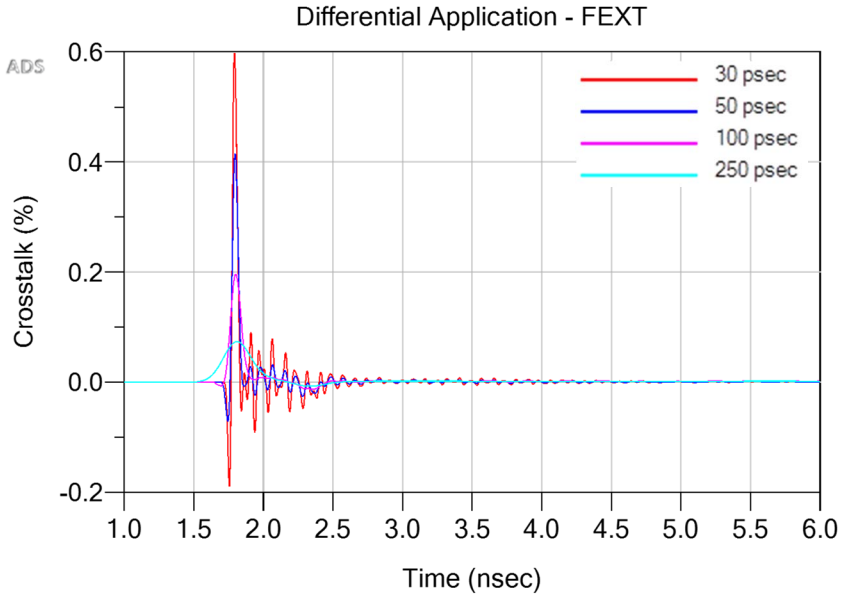


Differential Application (100 Ohm) – NEXT, Edge-Card_51,53_Edge-Card_58,60

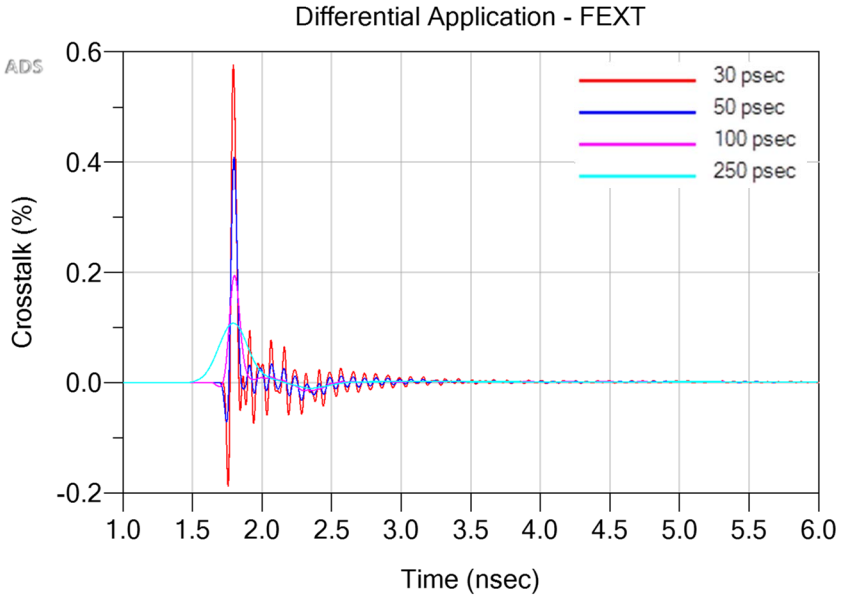


Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Differential Application (100 Ohm) – FEXT, Edge-Card_51,53_HSEC1_45,47

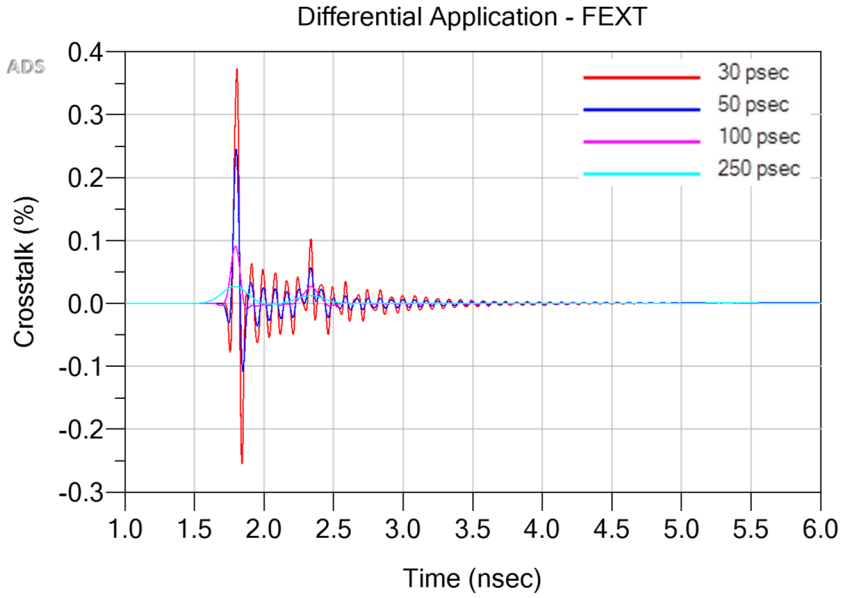


Differential Application (100 Ohm) – FEXT, Edge-Card_51,53_HSEC1_57,59

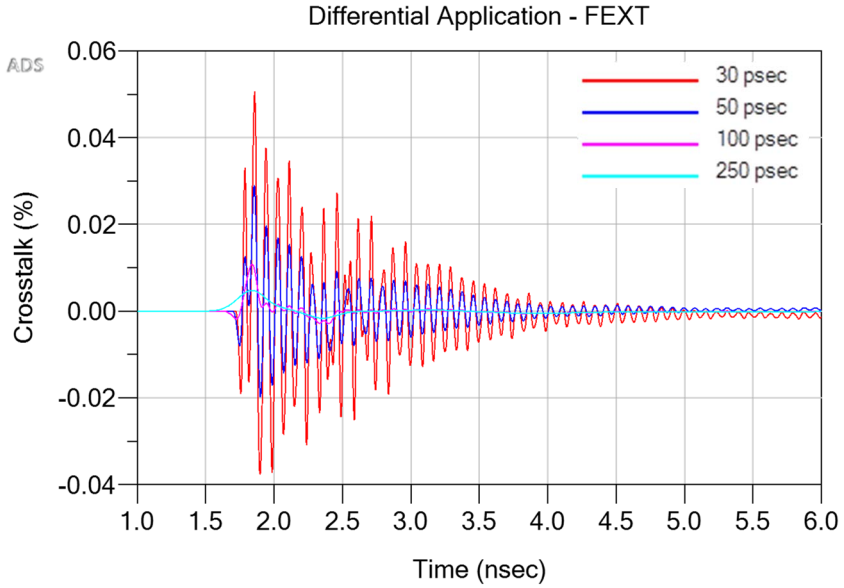


Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Differential Application (100 Ohm) – FEXT, Edge-Card_51,53_HSEC1_52,54



Differential Application (100 Ohm) – FEXT, Edge-Card_51,53_HSEC1_58,60



Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Appendix C – Product and Test System Descriptions

Product Description

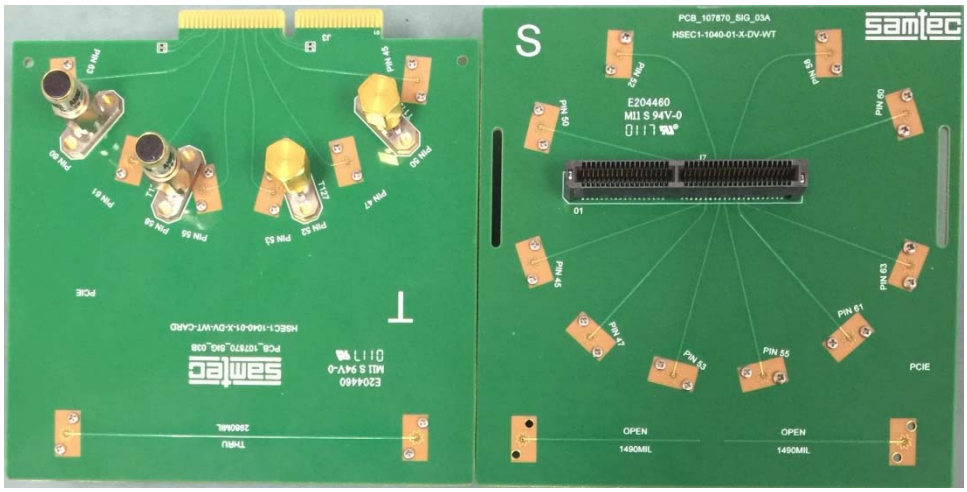
Product test samples are vertical surface mount HSEC1 Series connectors. The part number is HSEC1-040-01-L-DV-WT. The HSEC1 Series connectors use an edge-card contact system. Each connector has two rows of contacts evenly spaced on a 1.0mm (.0394") pitch. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Four test fixtures are specific to the HSEC1 series connector set and identified by part numbers PCB-107870-SIG-03-A and B, PCB-107870-SIG-04-A and B. Calibration standards specific to the HSEC1 series are located on the same boards.

PCB-107870-SIG-XX Test Fixtures

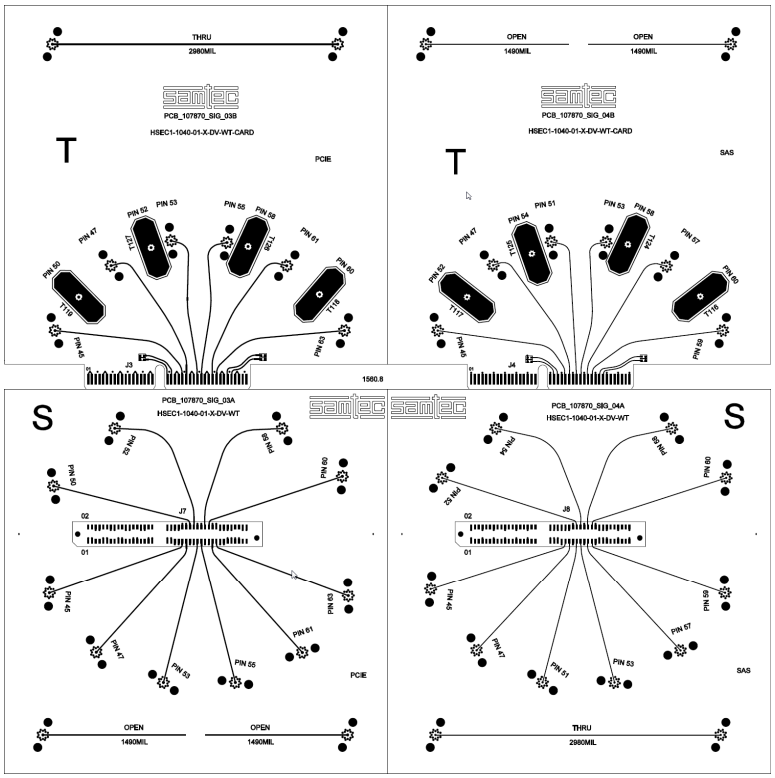
Shown below is a photograph of the one of the two test board sets.



Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

PCB-107870-SIG-XX PCB Layout Panel

Artwork of the PCB design is shown below.

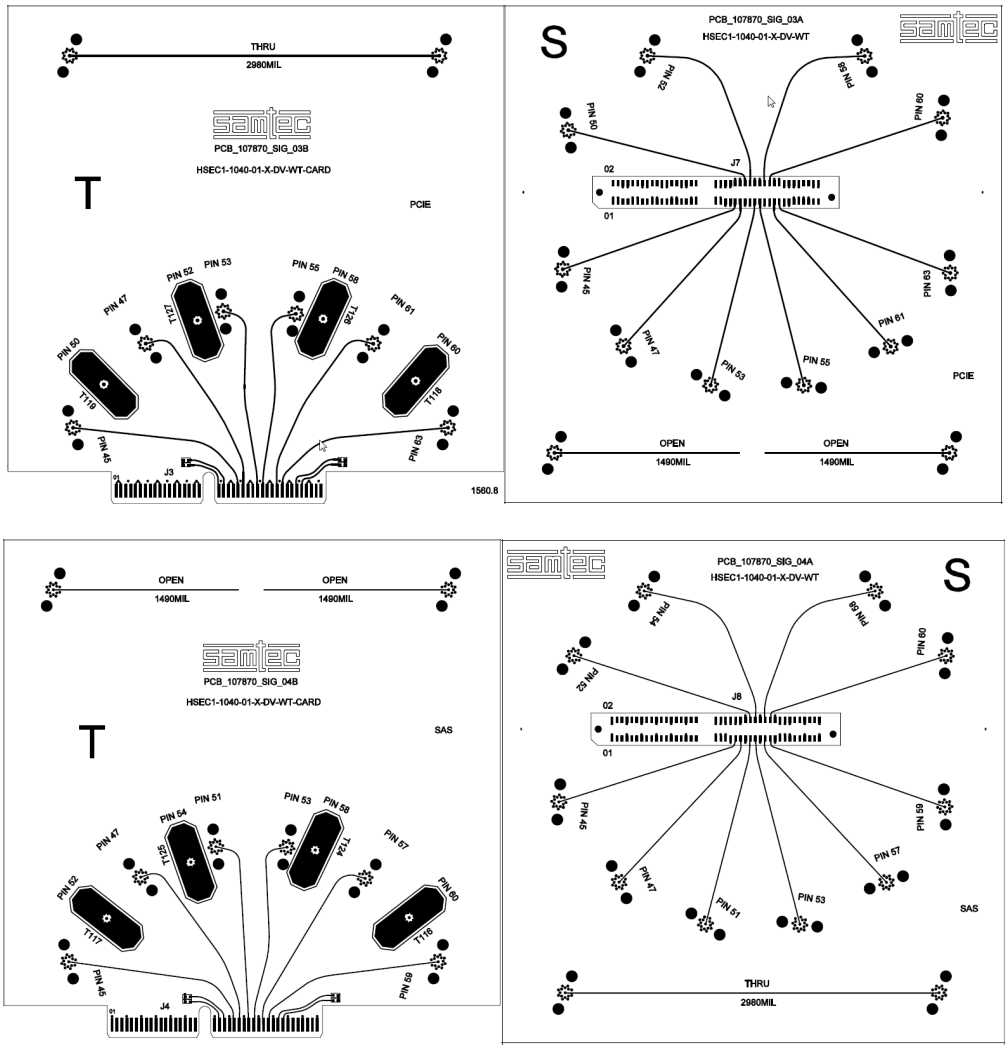


Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

PCB Fixtures

The test fixtures used are as follows:

PCB-107870-SIG-03-A – HSEC1 Series Test Board for 85 Ohm
PCB-107870-SIG-03-B – HSEC1 Series Edge Card for 85 Ohm
PCB-107870-SIG-04-A – HSEC1 Series Test Board for 100 Ohm
PCB-107870-SIG-04-B – HSEC1 Series Edge Card for 100 Ohm



Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

All traces on the test boards are length matched to 1.5" measured from the edge of the pad to the SMA. The AFR calibration effectively removes 1.49" of test board trace effects. This means that 10 mils of test board trace length effects are included in the both sides of test boards in the measurement.

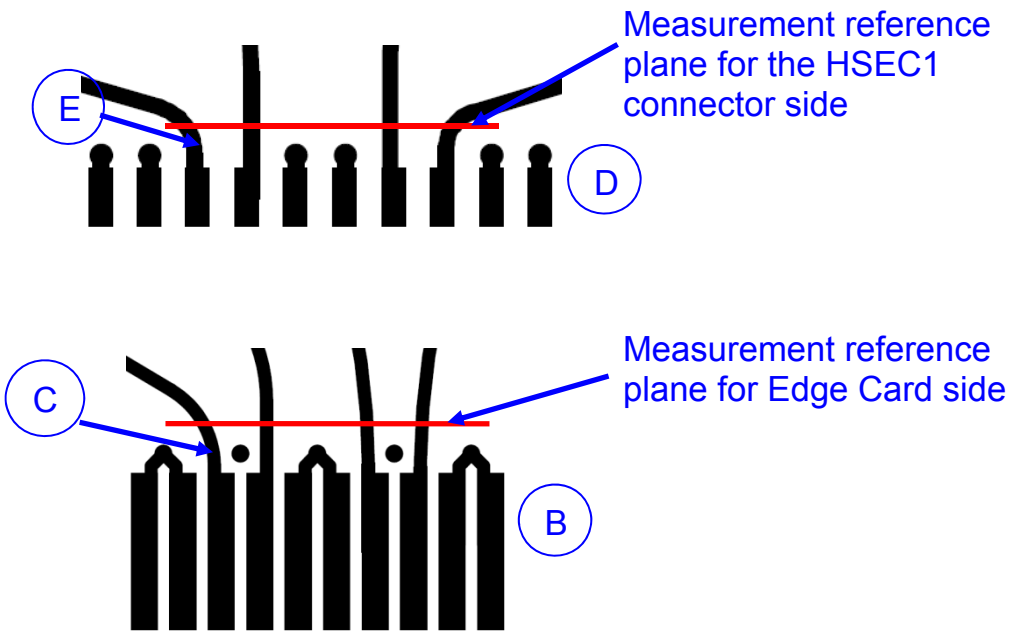
For 85 Ohm, The S-Parameter measurement includes:

A- The HSEC1 Series connector set
B- Test board vias, pads (footprint effects) for the HSEC1 connector side.
C- 10 mils of 13.5 mil wide microstrip trace.
D- Test board vias, pads (footprint effects) for the Edge Card side.
E- 10 mils of 13.5 mil wide microstrip trace.

For 100 Ohm, The S-Parameter measurement includes:

A- The HSEC1 Series connector set
B- Test board vias, pads (footprint effects) for the HSEC1 connector side.
C- 10 mils of 10 mil wide microstrip trace.
D- Test board vias, pads (footprint effects) for the Edge Card side.
E- 10 mils of 10 mil wide microstrip trace.

The figure below shows the location of the measurement reference plane.



Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

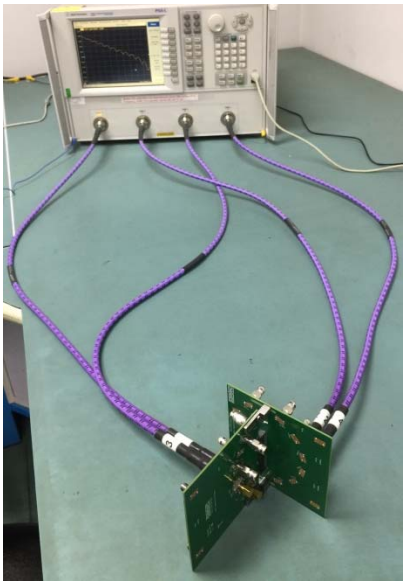
Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Keysight ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz
Stop Frequency – 20 GHz
Number of points –1601
IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ECAL module (300 KHz to 20 GHz)

Test Cables & Adapters

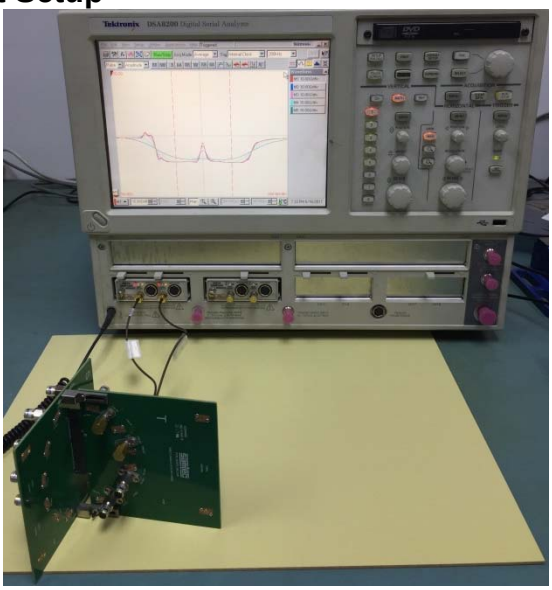
QTY	Description
4	Gore OWD01D02039-4 (DC-26.5 GHz)

Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

	Differential Signal
Vertical Scale:	10 ohm / Div:
Offset:	Default / Scroll
Horizontal Scale:	200ps/ Div
Record Length:	4000
Averages:	≥ 16

DSA8200 Measurement Setup



Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the through calibration standards, the SI test boards, and the selection of the PCB vendor.

A coaxial SOLT calibration is performed using a N4433A ECAL module. Then DUT measurements are performed under SOLT calibration. The measurements include the effect of test fixture. The measurements of the 2X THRU line standards are required to remove the test fixture effect.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Keysight ADS 2016. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Near-End Crosstalk (TDT) & Far End Crosstalk (TDT)
A step pulse is applied to the touchstone model of the connector and the coupled voltage is monitored. The amplitude of the peak-coupled voltage is recorded and reported as a percentage of the input pulse.

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Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Impedance (TDR)

Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

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Series: HSEC1-DV
Description: 1.00 mm Edge Rate® High-Speed Edge Card Connector, Vertical

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
BC – Best Case crosstalk configuration
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
Z – Impedance (expressed in ohms)