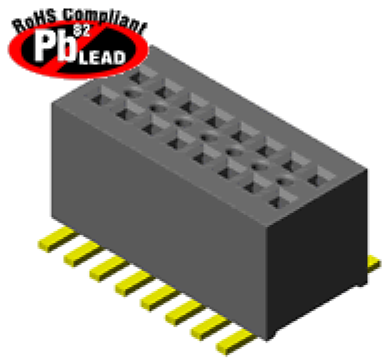
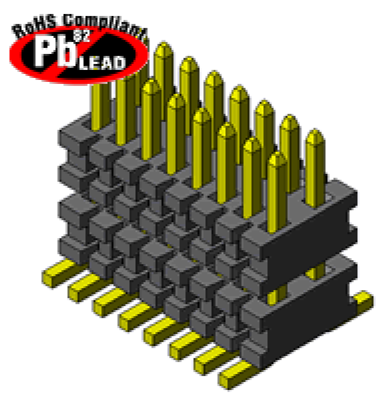
High Speed Characterization Report

CLE-150-01-G-DV-ES-A



Mates with

AW-50-03-G-D-230-075-ES-A



Description:

MICRO SOCKET & TERMINAL STRIP
SURFACE MOUNT, 0.8mm (.0315") CENTERLINE,
9.14mm (0.360") Board-to-Board Stack Height

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 10/22/2010

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Table of Contents

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Connector Overview

Micro 0.8mm (.0315") pitch, low profile socket & terminal strip connectors are available with up to 90 contacts per row. The CLE/AW series is surface mount, offers a double row option, and includes gold plating. Data presented in this report is applicable only to the 9.14mm stack height CLE/AW connector series.

Connector System Speed Rating

CLE/AW Connector Series, 0.8mm (.0315") Pitch, Surface Mount, Double Row, Gold Plating, Cost Effective, Ideal for pass through applications

Signaling	Speed Rating
Single-Ended:	**8.0GHz / 16Gbps**
Differential:	**7.5GHz / 15Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded-up to the nearest half-GHz level. The up rounding corrects for a portion of the test board's trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Frequency Domain Data Summary

Table 1 - Single-Ended Signaling System Performance

Test Parameter	Filename	Source	Victim	
Insertion Loss	SL_1_1	Tx, port1=AW_44, Rx, port3=CLE_44	[redacted]	-3dB @ 7.7 GHz
Return Loss	SL_1_1	Tx, port1=AW_44, Rx, port3=CLE_44	[redacted]	≤ -5dB to 7.7 GHz
Near-End Crosstalk	SN_1_1	AW_42	AW_40	≤ -7dB to 7.7 GHz
	SN_1_2	AW_40	AW_44	≤ -26dB to 7.7 GHz
	SN_1_3	AW_7	AW_8	≤ -18dB to 7.7 GHz
Far-End Crosstalk	SF_1_1	AW_40	CLE_44	≤ -12dB to 7.7 GHz
	SF_1_2	AW_42	CLE_40	≤ -23dB to 7.7 GHz
	SF_1_3	AW_7	CLE_8	≤ -21dB to 7.7 GHz

Table 2 - Differential Signaling System Performance

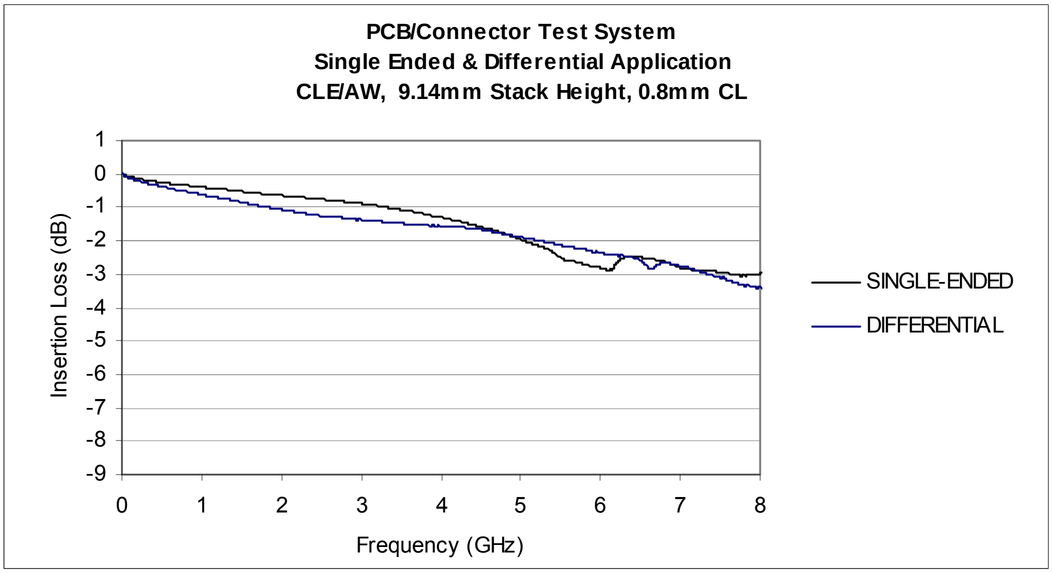
Test Parameter	Filename	Source	Victim	
Insertion Loss	DL_1_1	Tx, port12=AW_90-92, Rx, port34=CLE_90-92	[redacted]	-3dB @ 7.3 GHz
Return Loss	DL_1_1	Tx, port12=AW_90-92, Rx, port34=CLE_90-92	[redacted]	≤ -9dB to 7.3 GHz
Near-End Crosstalk	DN_1_1	AW_94-92	AW_90-88	≤ -19dB to 7.3 GHz
	DN_1_2	AW_84-86	AW_90-92	≤ -42dB to 7.3 GHz
	DN_1_3	AW_6-4	AW_3-5	≤ -29dB to 7.3 GHz
Far-End Crosstalk	DF_1_1	AW_94-92	CLE_90-88	≤ -24dB to 7.3 GHz
	DF_1_2	AW_84-86	CLE_90-92	≤ -31dB to 7.3 GHz
	DN_1_3	AW_6-4	CLE_3-5	≤ -32dB to 7.3 GHz

Pin Map (reference Appendix C for full description of test boards)

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Bandwidth Chart – Single-Ended & Differential Insertion Loss

CLE/AW Socket & Terminal Strip Series



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω)							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	61.7	56.9	53.0	51.6	51.3	51.2	51.1
Minimum Impedance	41.0	46.2	48.8	49.1	49.1	49.2	49.3

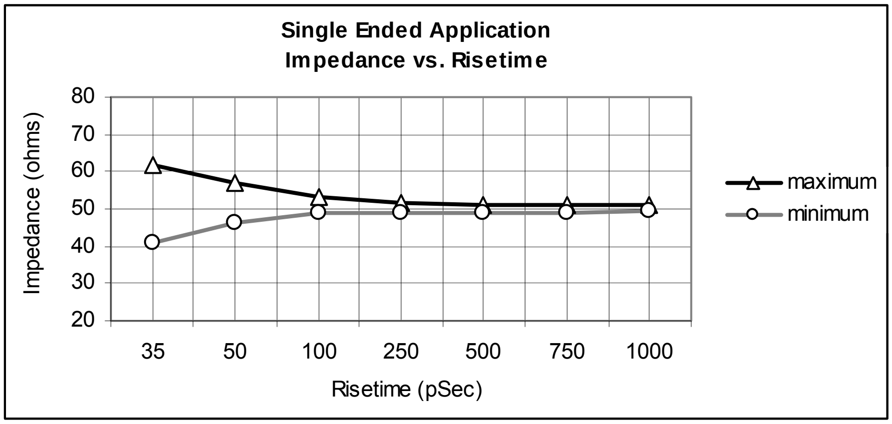
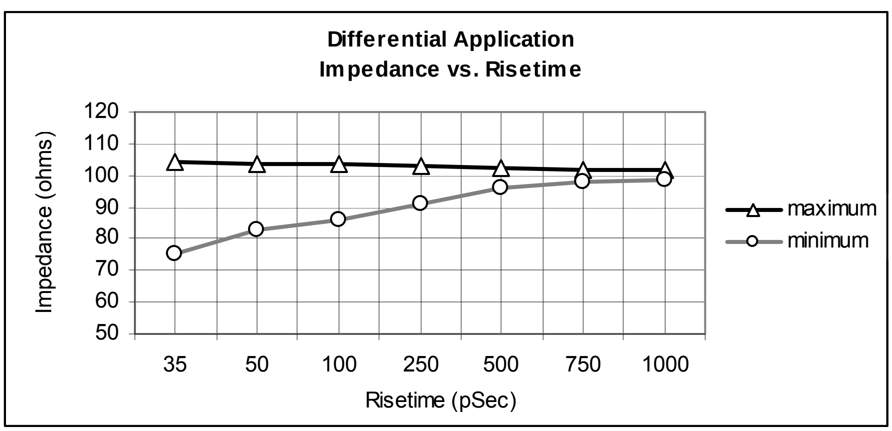


Table 4 - Differential Impedance (Ω)							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	104.1	103.7	103.5	102.8	102.3	101.9	101.8
Minimum Impedance	75.2	83.0	86.0	91.2	96.0	97.8	98.6



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Table 5 - Single-Ended Crosstalk (%)

	Input (t_r)	Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	µp1 to µp3	AW_42	AW_40	16.4	15.6	13.2	7.5	4.2	2.9	2.2
		AW_40	AW_44	2.4	1.9	1.5	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		AW_7	AW_8	4.4	3.9	3.1	1.5	< 1.0%	< 1.0%	< 1.0%
FEXT	µp1 to µp5	AW_42	CLE_40	7.8	6.4	5.2	2.6	1.4	< 1.0%	< 1.0%
		AW_40	CLE_44	3.3	2.0	1.2	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		AW_7	CLE_8	2.7	1.7	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 6 - Differential Crosstalk (%)

	Input (t_r)	Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	$\mu p1^+2^-$ to $\mu p3^+4^-$	AW_94-92	AW_90-88	5.1	4.7	3.8	2.2	1.3	< 1.0%	< 1.0%
		AW_84-86	AW_90-92	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		AW_6-4	AW_3-5	1.8	1.6	1.2	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	$\mu p1^+2^-$ to $\mu p5^+6^-$	AW_94-92	CLE_90-88	1.9	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		AW_84-86	CLE_90-92	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		AW_6-4	CLE_3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay

Configuration		Signal Path	Mated Connector Only
Single-Ended	µp1 to µp8	Tx, port1=AW_44, Rx, port3=CLE_44	54ps
Differential	µp12 to µp78	Tx, port12=AW_90-92, Rx, port34=CLE_90-92	54ps

Pin Map (reference Appendix C for full description of test boards)

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive-side probe tip to receive side probe tip. PCB effects are not removed or de-embedded from test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. However, other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high-speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others; connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. However, dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

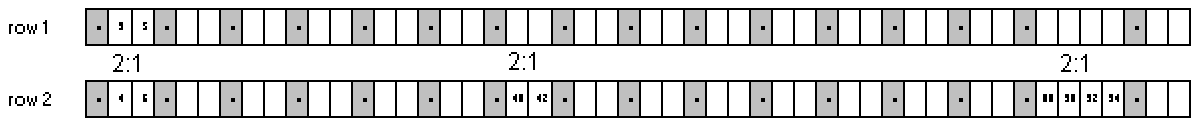
Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

For this connector, the following array configurations are evaluated:

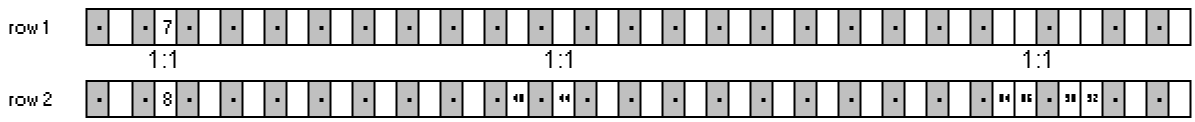
[ ] open pin field   [X] grounded pin field

[P#] signal aggressor or signal victim pins

TST-11 (board 1) & TST-12 (board



TST-21 (board 3) & TST-22 (board



<u>Single-Ended Impedance:</u>
- Well-referenced line; 1:1, S:G ratio

<u>Single-Ended Crosstalk:</u>
- Well-referenced line; mimics 1:1 S:G ratio
- 2:1 S:G ratio

Only one single-ended signal was driven for crosstalk measurements.

<u>Differential Impedance:</u>
- Well-referenced line 1:1, S:G ratio

<u>Differential Crosstalk:</u>
- Well-referenced line; mimics 1:1 S:G ratio
- Higher Signal Density, 2:1 S:G ratio
- Full-Row Differential

Only one differential pair was driven for crosstalk measurements.

*In all cases where a center ground blade is present in the connector, it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. However, in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect, can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 35 +/-5 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data
Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT's frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Time Domain Data
Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be

available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 35 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 35 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. However, modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

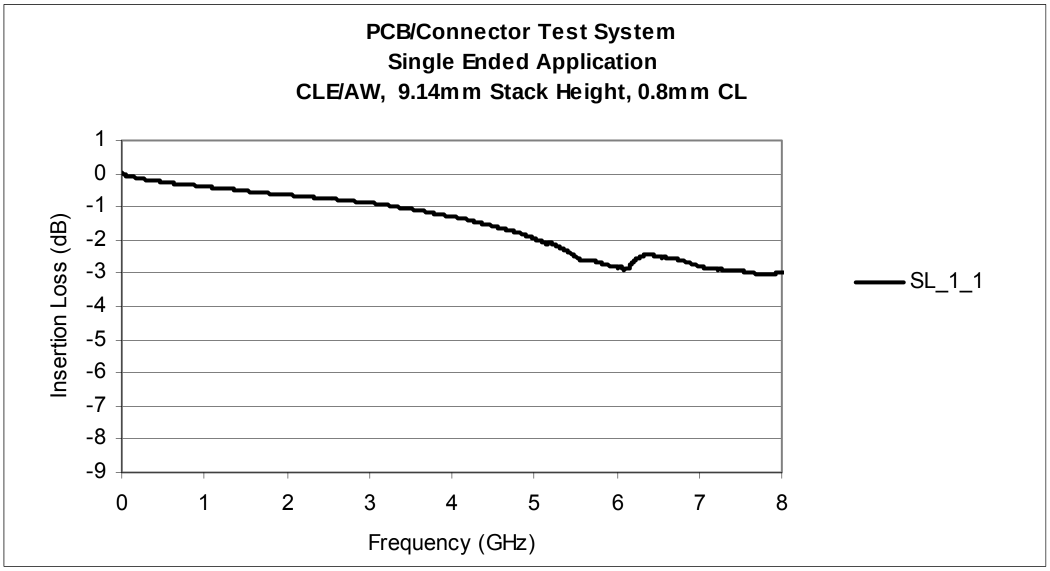
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Appendix A – Frequency Domain Response Graphs

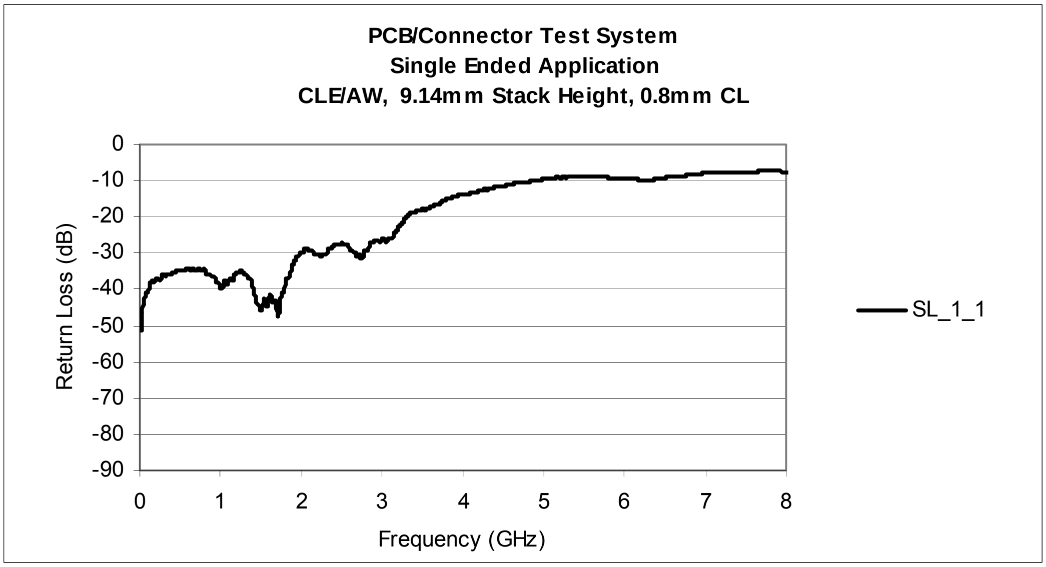
Single-Ended Application – Insertion Loss

Configuration: Tx, port1=AW_44, Rx, port3=CLE_44



Single-Ended Application – Return Loss

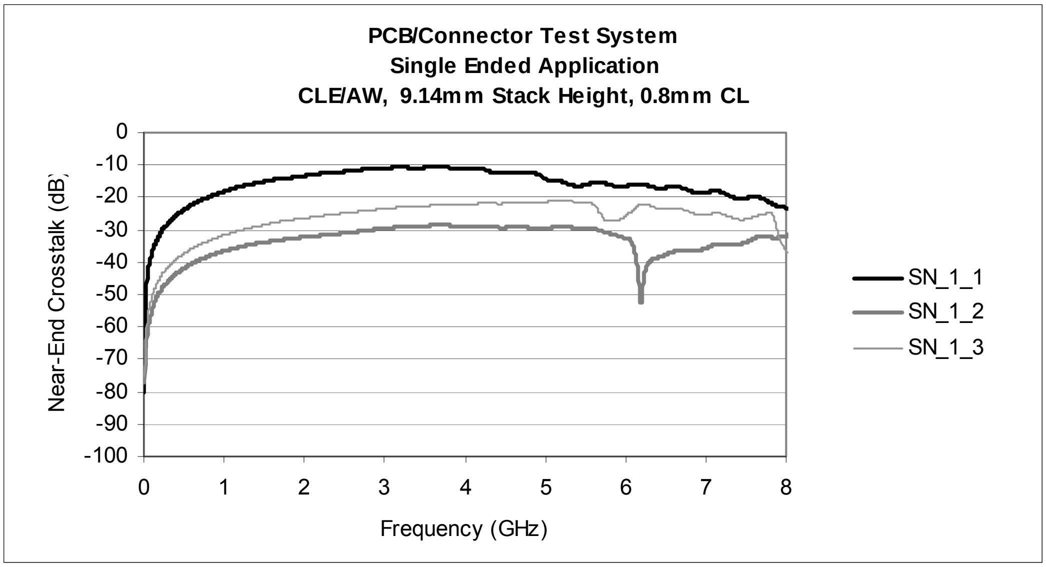
Configuration: Tx, port1=AW_44, Rx, port3=CLE_44



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

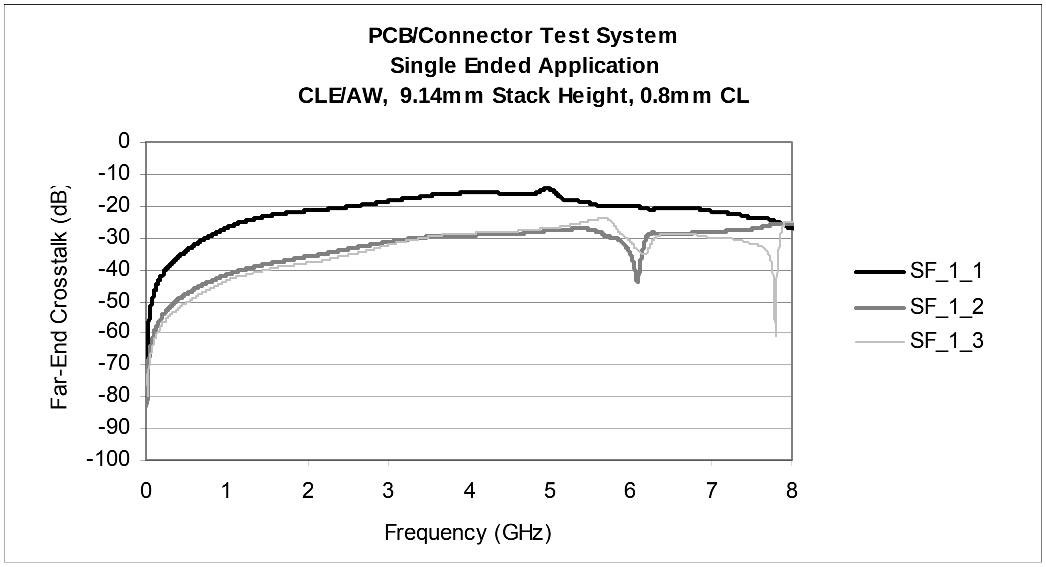
Single-Ended Application – NEXT Configurations

AW_42	AW_40
AW_40	AW_44
AW_7	AW_8



Single-Ended Application – FEXT Configurations

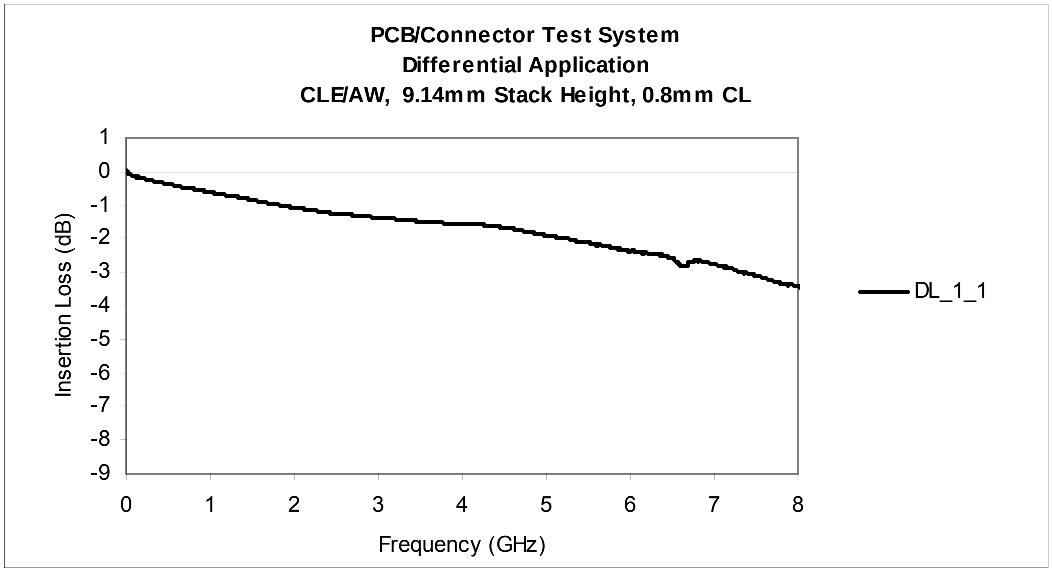
AW_42	CLE_40
AW_40	CLE_44
AW_7	CLE_8



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

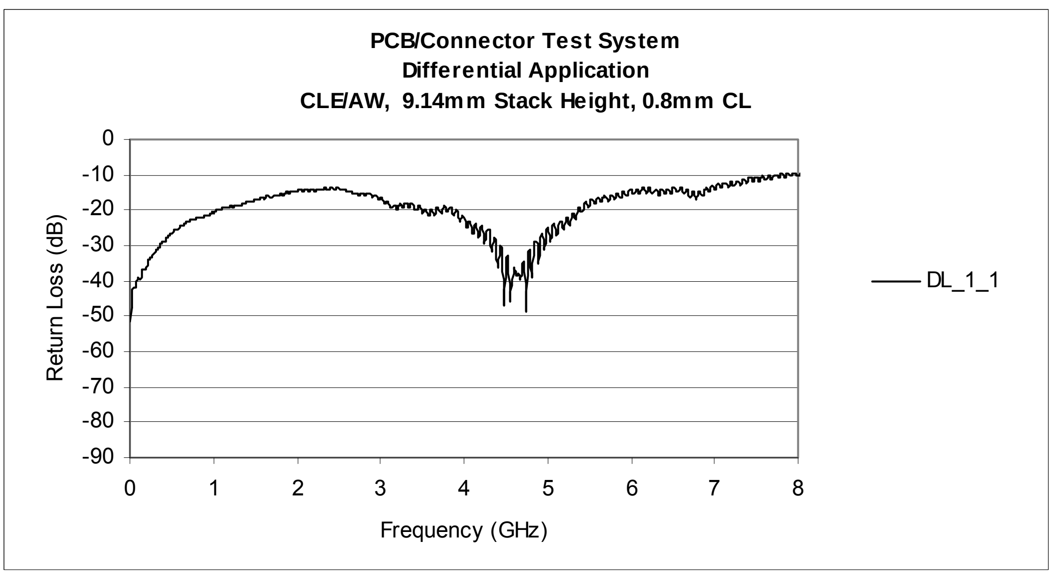
Differential Application – Insertion Loss

Configuration: Tx, port12=AW_90-92, Rx, port34=CLE_90-92



Differential Application – Return Loss

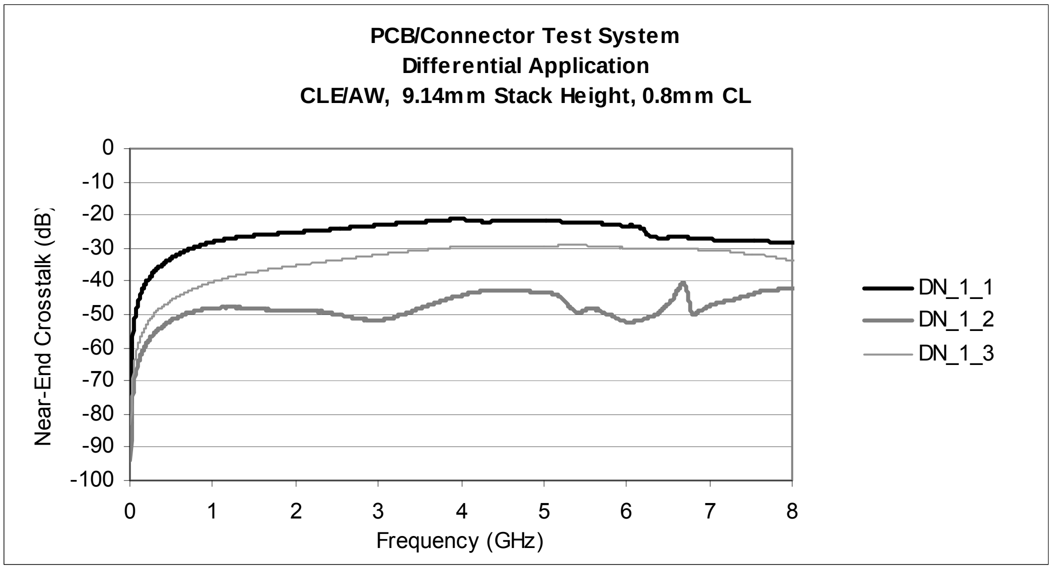
Configuration: Tx, port12=AW_90-92, Rx, port34=CLE_90-92



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

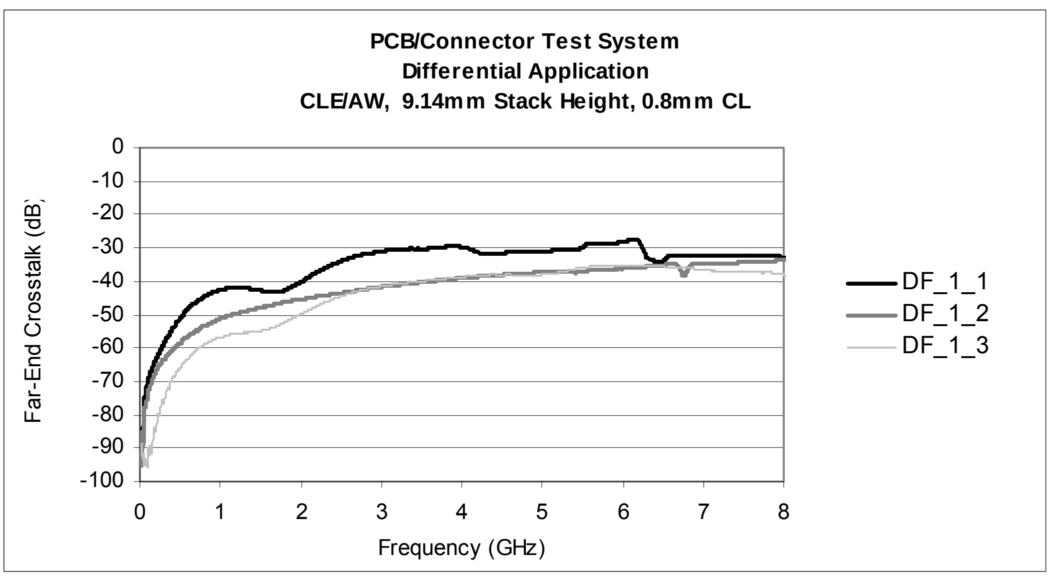
Differential Application – NEXT Configurations

AW_94-92	AW_90-88
AW_84-86	AW_90-92
AW_6-4	AW_3-5



Differential Application – FEXT Configurations

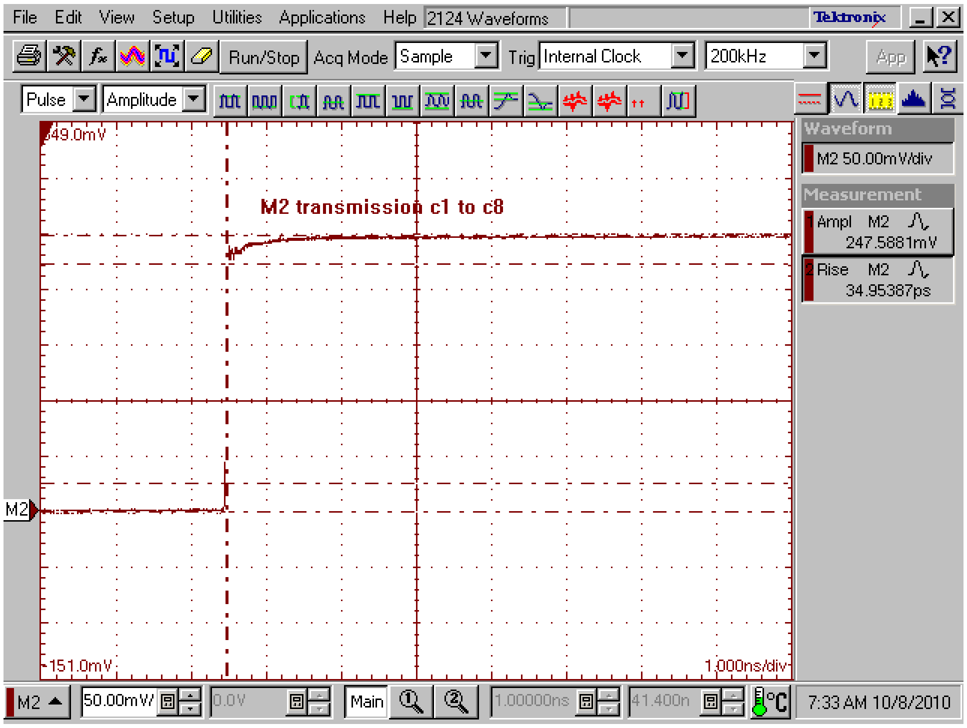
AW_94-92	CLE_90-88
AW_84-86	CLE_90-92
AW_6-4	CLE_3-5



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Appendix B – Time Domain Response Graphs

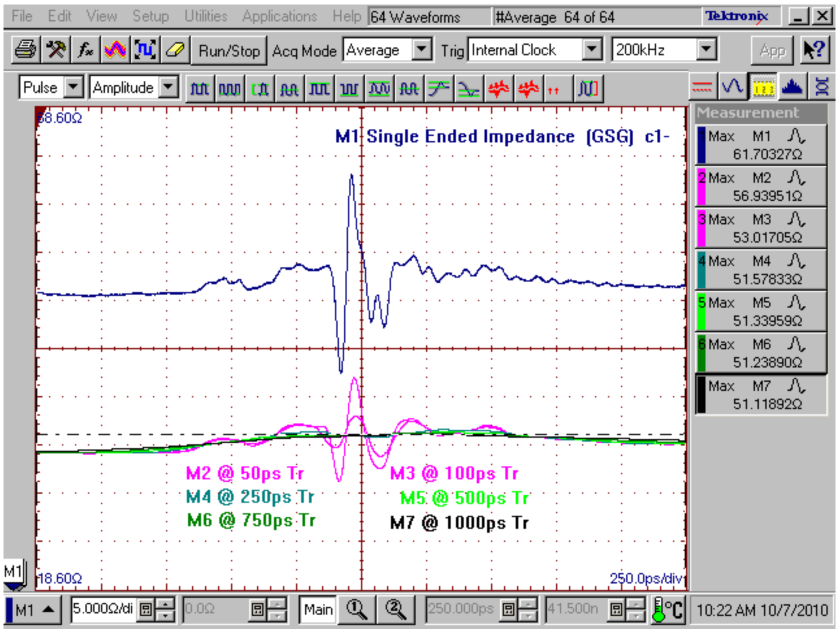
Single-Ended Application – Input Pulse,
port1=µprobe Tx1 port2= µprobe Rx1



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

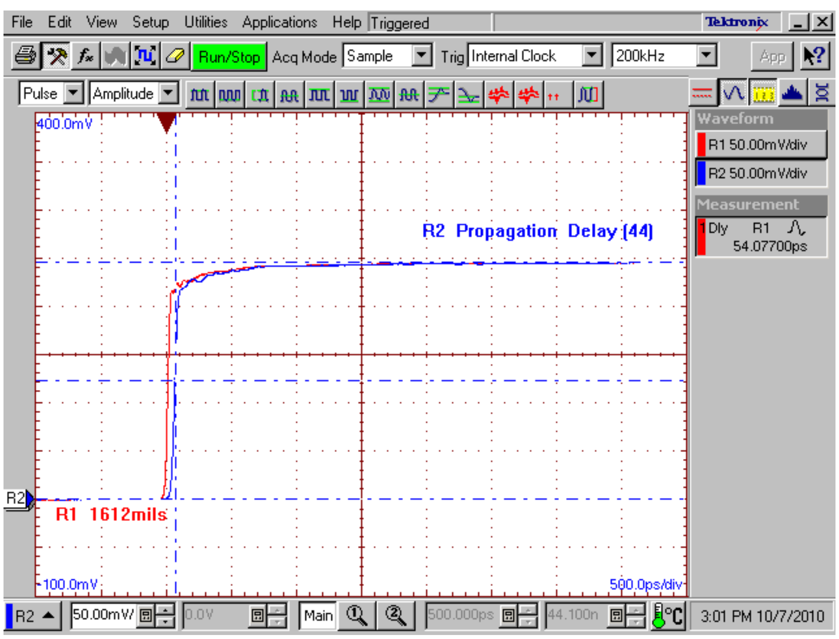
Single-Ended Application – Impedance

Configuration: Tx, port1=AW_44, Rx, port3=CLE_44



Single-Ended Application – Propagation Delay

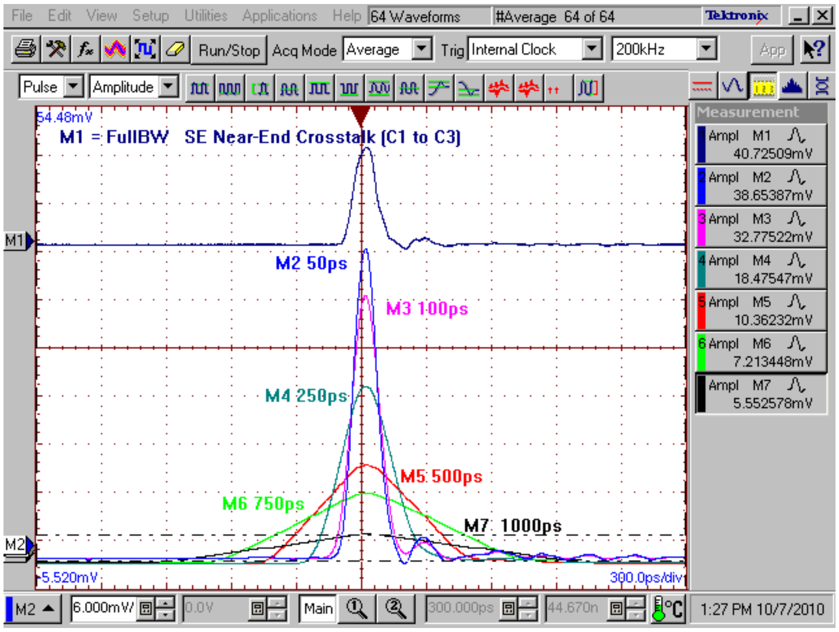
Configuration: Tx, port1=AW_44, Rx, port3=CLE_44



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

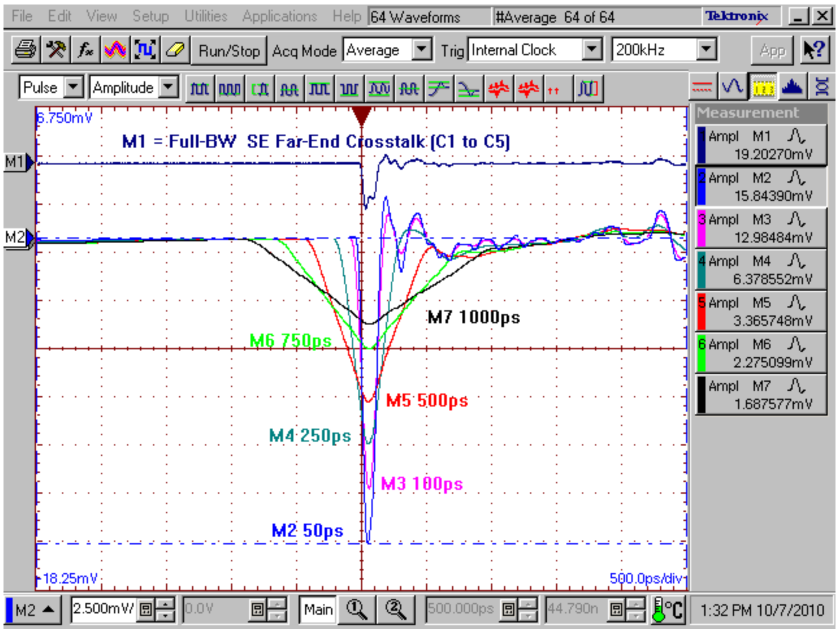
Single-Ended Application – NEXT, Worst Case Configuration

AW_40 AW_42



Single-Ended Application – FEXT, Worst Case Configuration

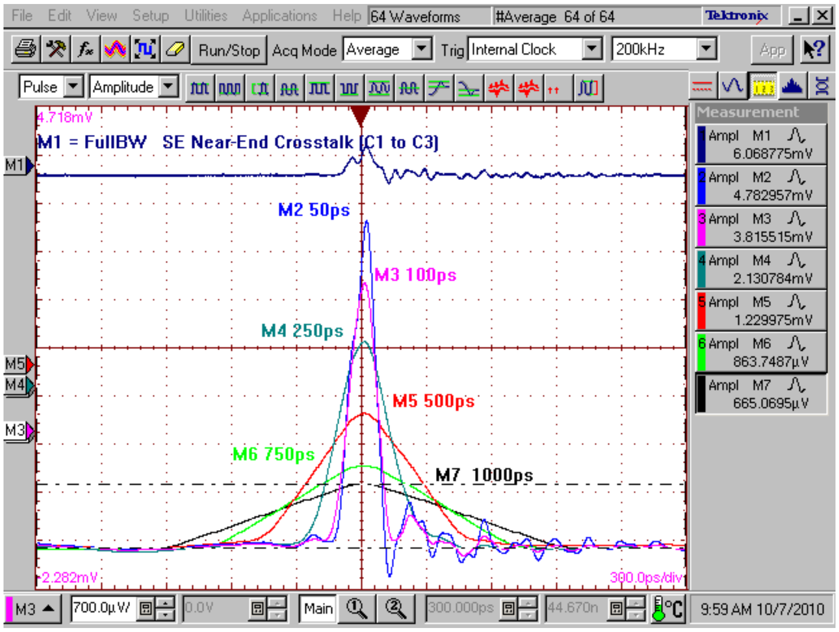
AW_40 CLE_42



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

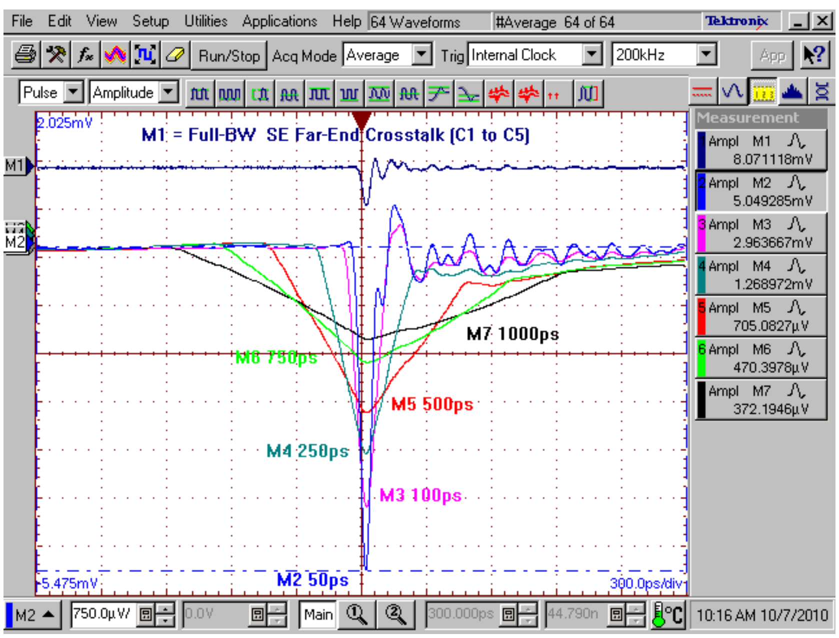
Single-Ended Application – NEXT, Best Case Configuration

AW_40 AW_44



Single-Ended Application – FEXT, Best Case Configuration

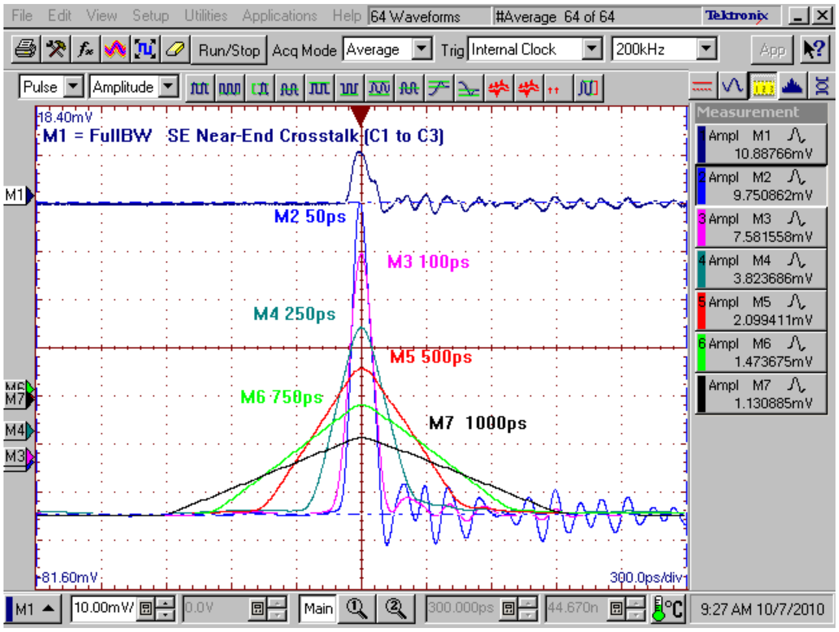
AW_40 CLE_44



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

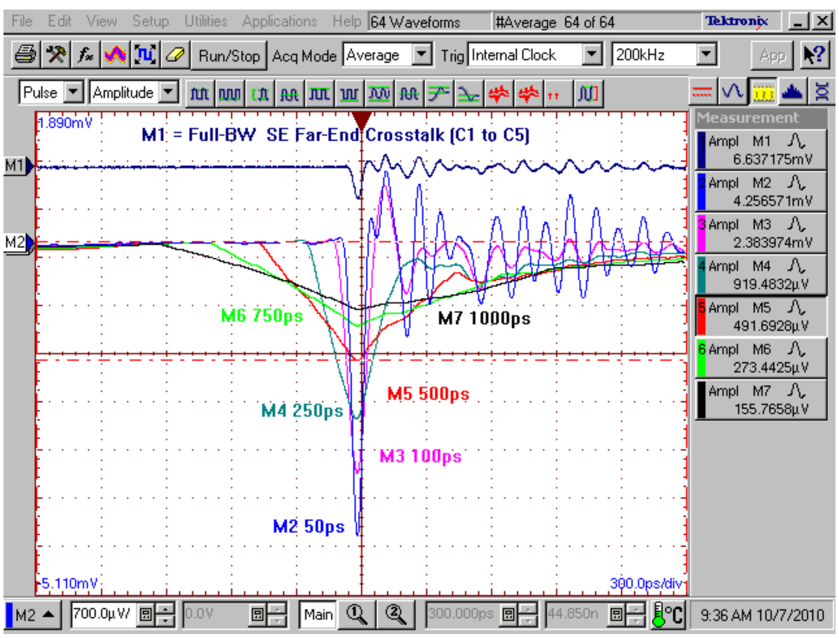
Single-Ended Application – NEXT, Across Row Configuration

AW_7 AW_8



Single-Ended Application – FEXT, Across Row Configuration

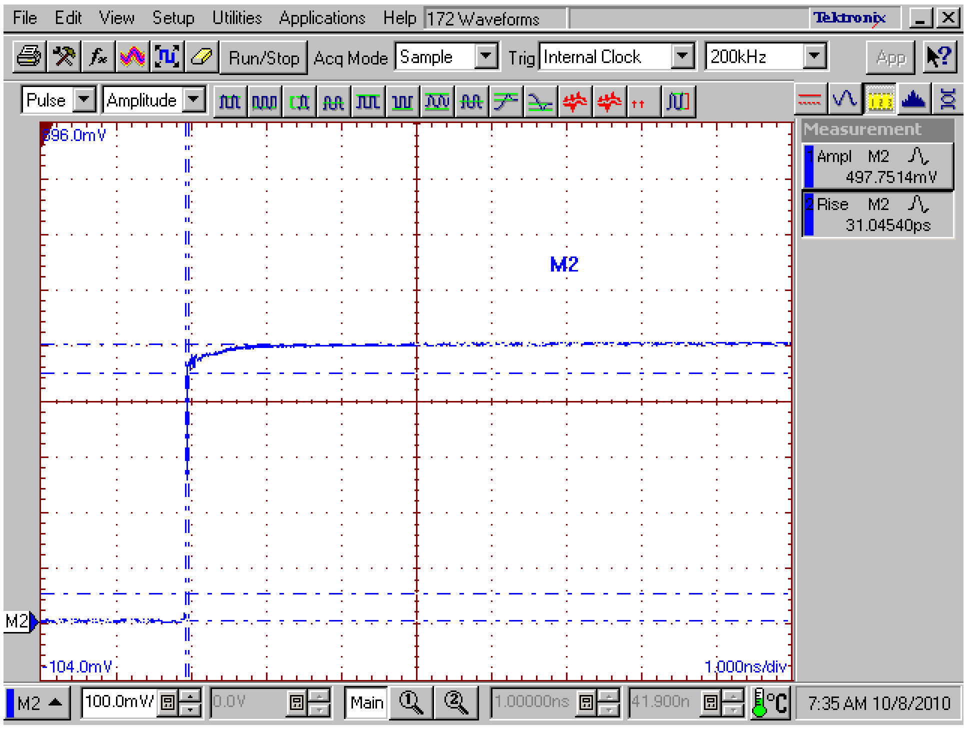
AW_7 CLE_8



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Differential Application – Input Pulse

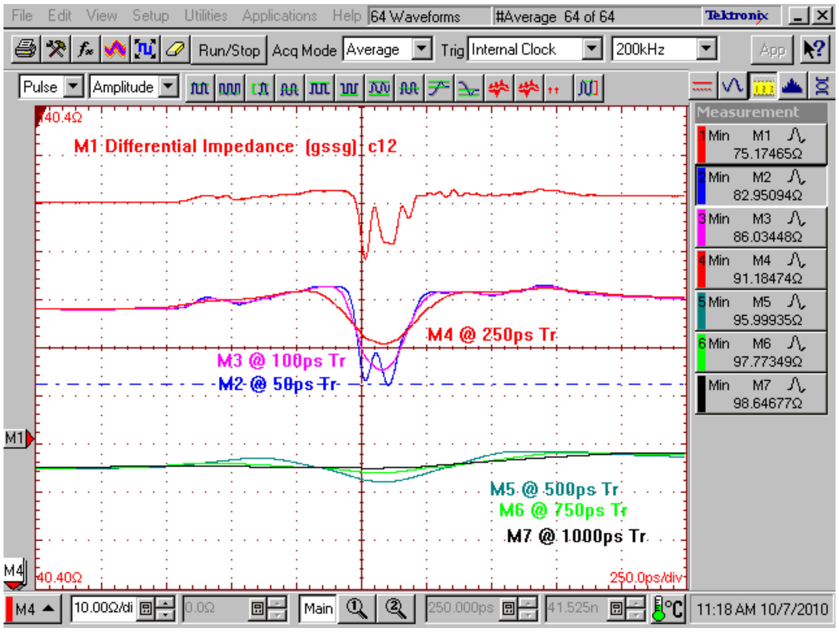
Port 12= μprobe Tx12 to Port 34= μprobe Rx78



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

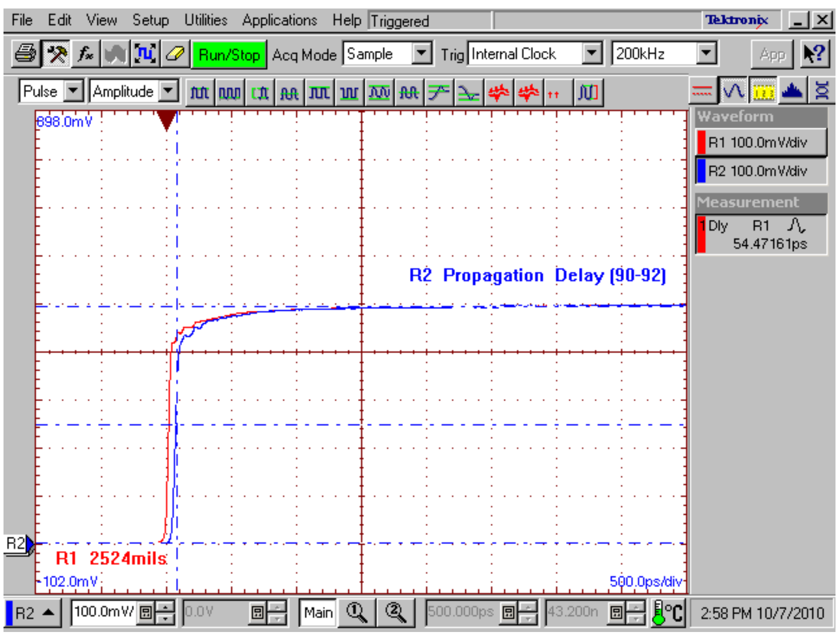
Differential Application – Impedance

Configuration: Tx, port12=AW_90-92, Rx, port34=CLE_90-92



Differential Application – Propagation Delay

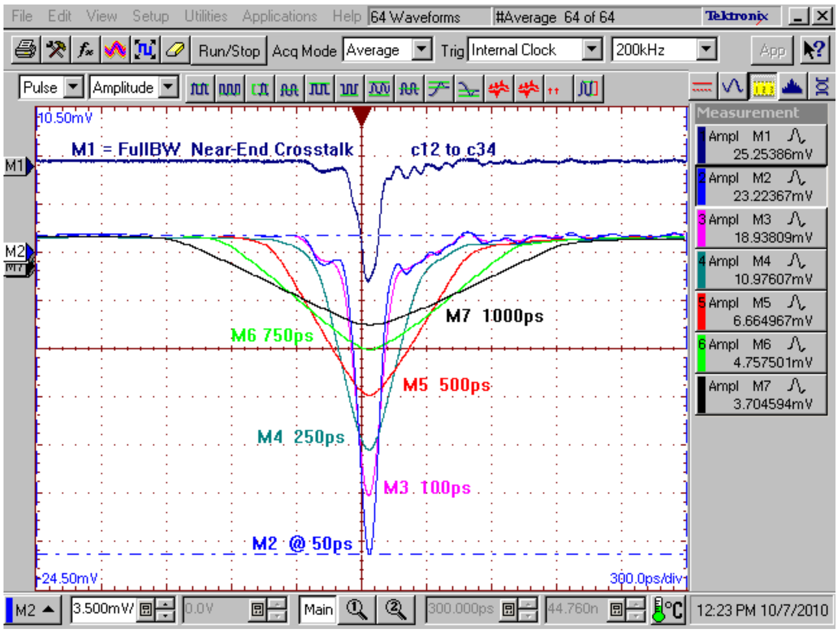
Configuration: Tx, port12=AW_90-92, Rx, port34=CLE_90-92



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

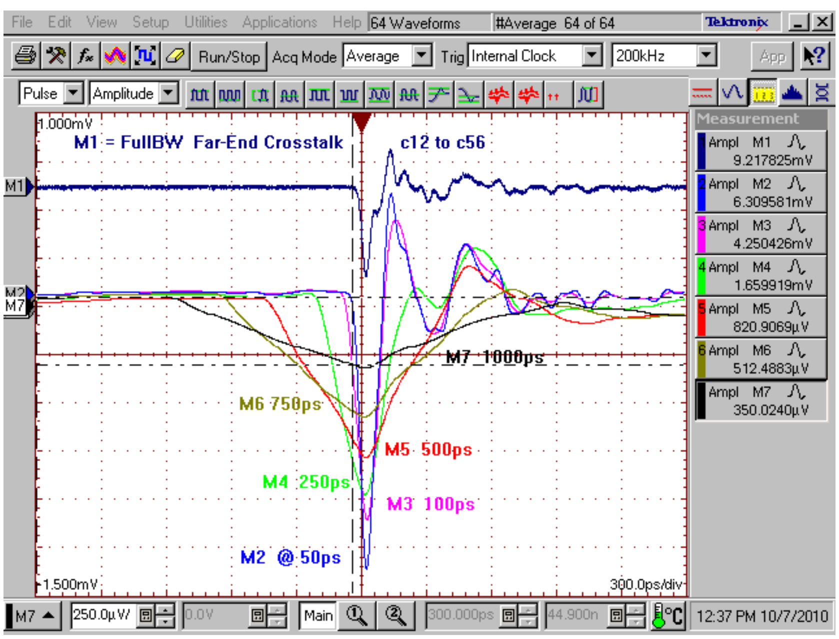
Differential Application – NEXT, Worst Case

AW_94-92 AW_90-88



Differential Application – FEXT, Worst Case

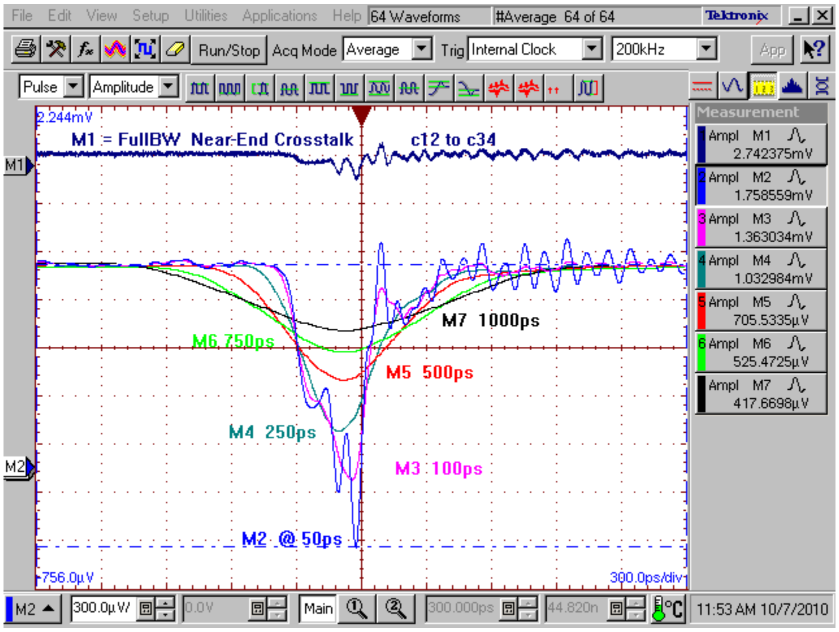
AW_94-92 CLE_90-88



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

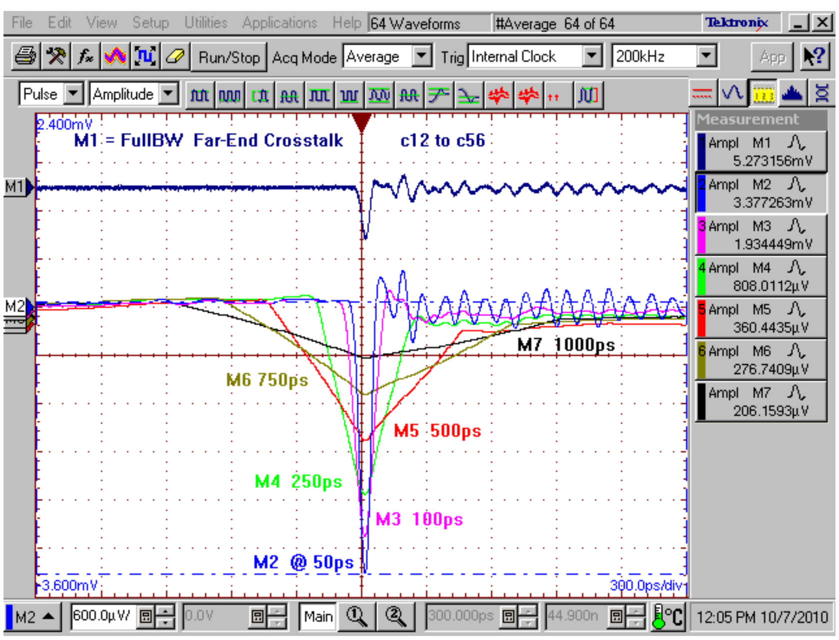
Differential Application – NEXT, Best Case

AW_84-86 AW_90-92



Differential Application – FEXT, Best Case

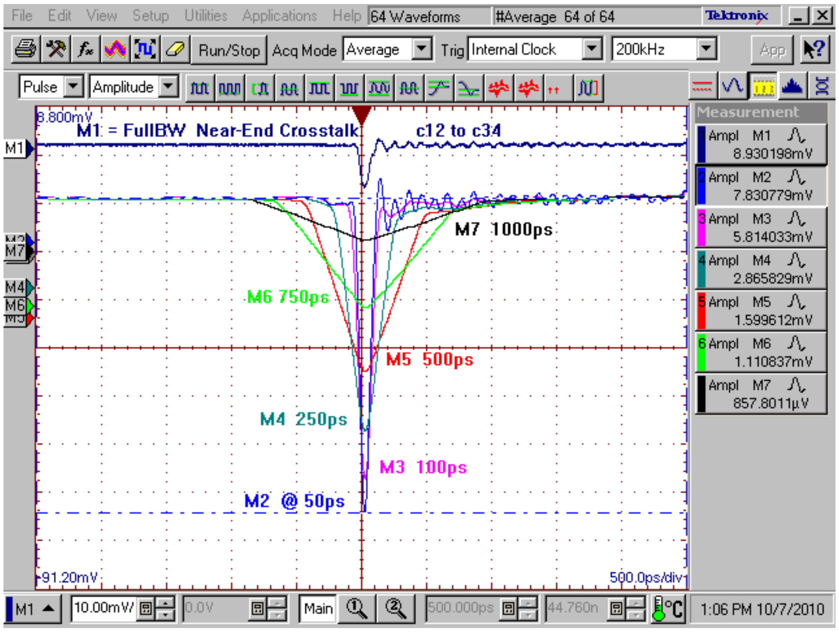
AW_84-86 CLE_90-92



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

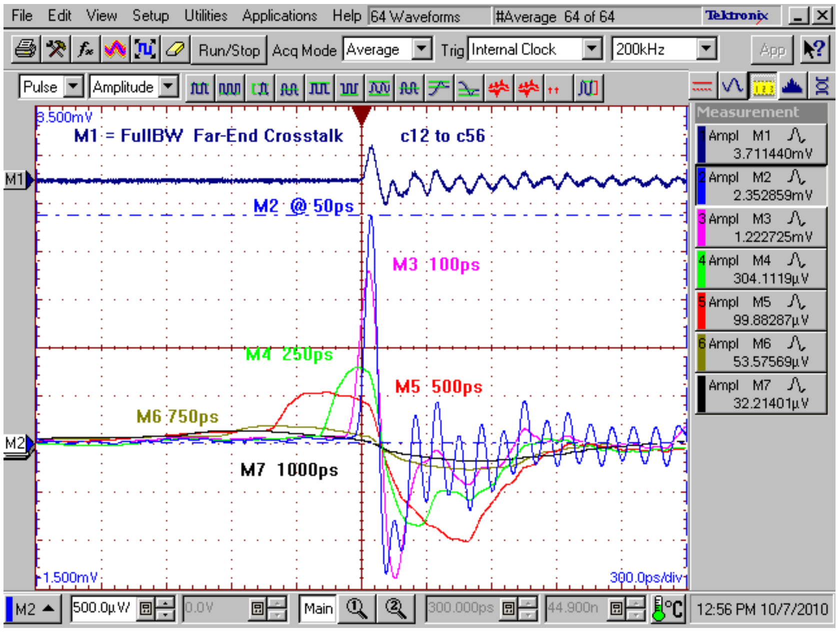
Differential Application – NEXT, Across Row Case

AW_6-4 AW_3-5



Differential Application – FEXT, Across Row Case

AW_6-4 CLE_3-5



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Appendix C – Product and Test System Descriptions

Product Description

Product test samples are surface mount socket part number CLE-150-01-G-DV-ES-A and terminal part number AW-50-03-G-D-230-075-ES-A. CLE/AW 0.8mm series is available up to 90 contacts per row. This CLE/AW hi-speed characterization reports results on a 50 contacts per row, 0.8mm (.0315") contact pitch, 9.14mm stack height board-to-board connector system.

Test System Description

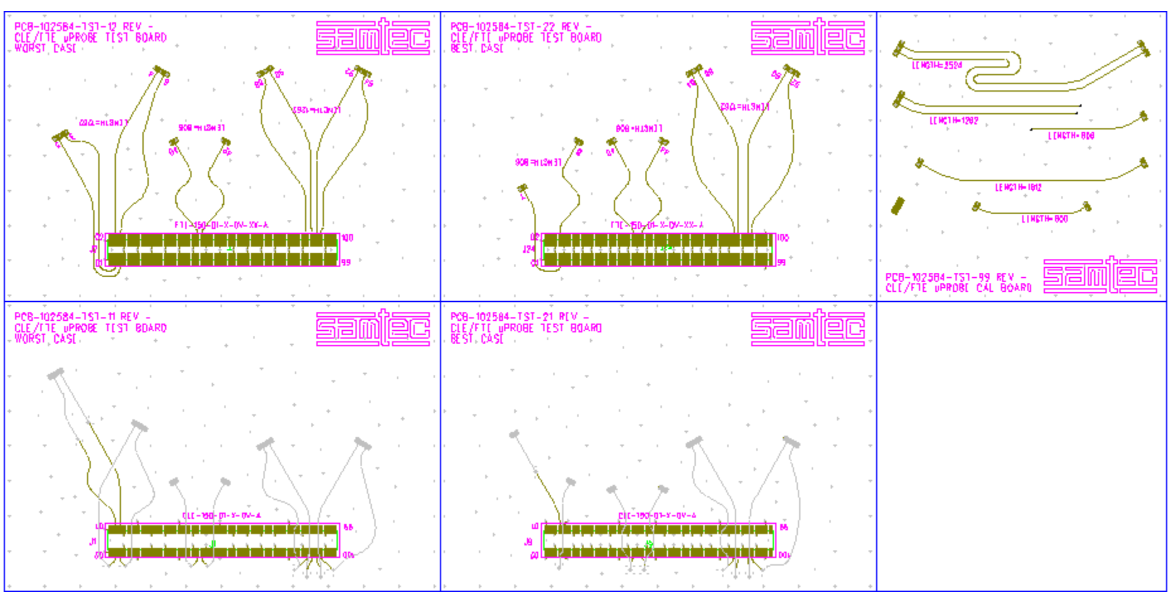
The test fixtures are composed of 4-layer FR-406 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. Edge Rate 0.8mm series test fixture labels identify PCB-102584-TST-11, PCB-102584-TST-12, PCB-102584-TST-21, and PCB-102584-TST-22. Electrical continuity exists between all the labeled test points where -11 mates to -12 and -21 mates to -22. Calibration standards specific to the CLE/AW 0.8mm series are located on test board labeled PCB-102584-TST-99 Rev, µ-PROBE CAL BOARD. All data and waveforms presented are results from an AW terminal side launch. Pictured on the next page are the mated test samples and a printed circuit board layout panel.

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

PCB-102584-TST – 9.14mm Stack Height Test Fixtures

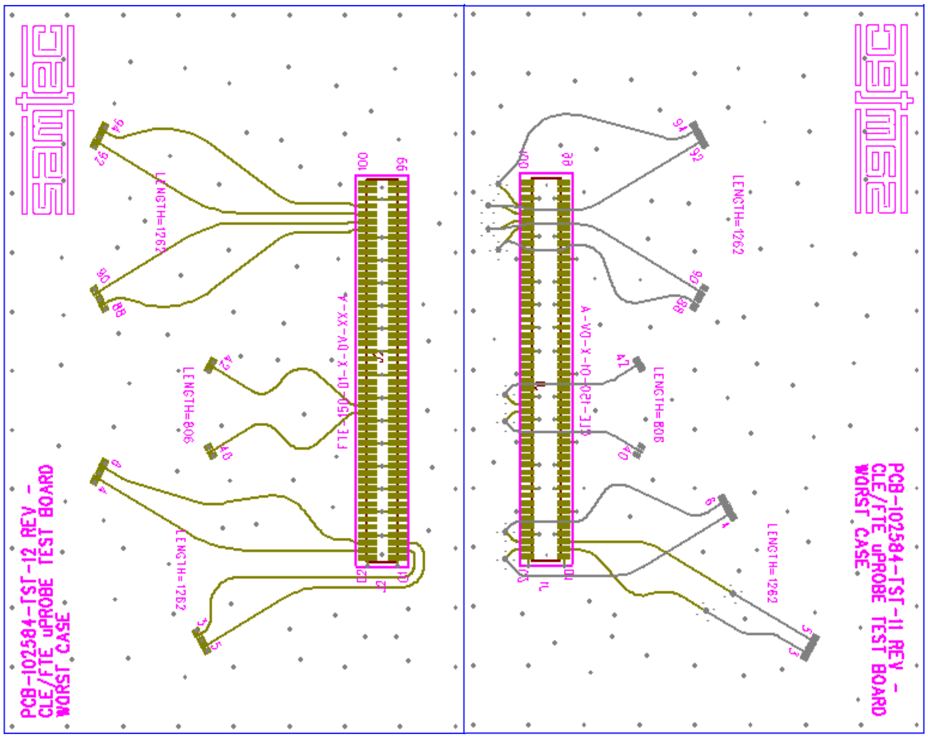
Board -11 mates with Board -12   Board -21 mates with Board -22

PCB-102584-TST PCB Array Panel



Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

PCB-102584-TST, Set 11 & 12 Mapping



Fixture Test Points – CLE/FTE µProbe Test Board, Best Case

Board No.	PCB-102584-TST-11	Socket:	CLE-150-01-G-DV-ES-A
	PCB-102584-TST-12	Terminal:	AW-50-03-G-D-230-075-ES-A

Transmission and Reflection Test Parameters:

Insertion Loss, Return Loss, Impedance, Propagation Delay

Differential:

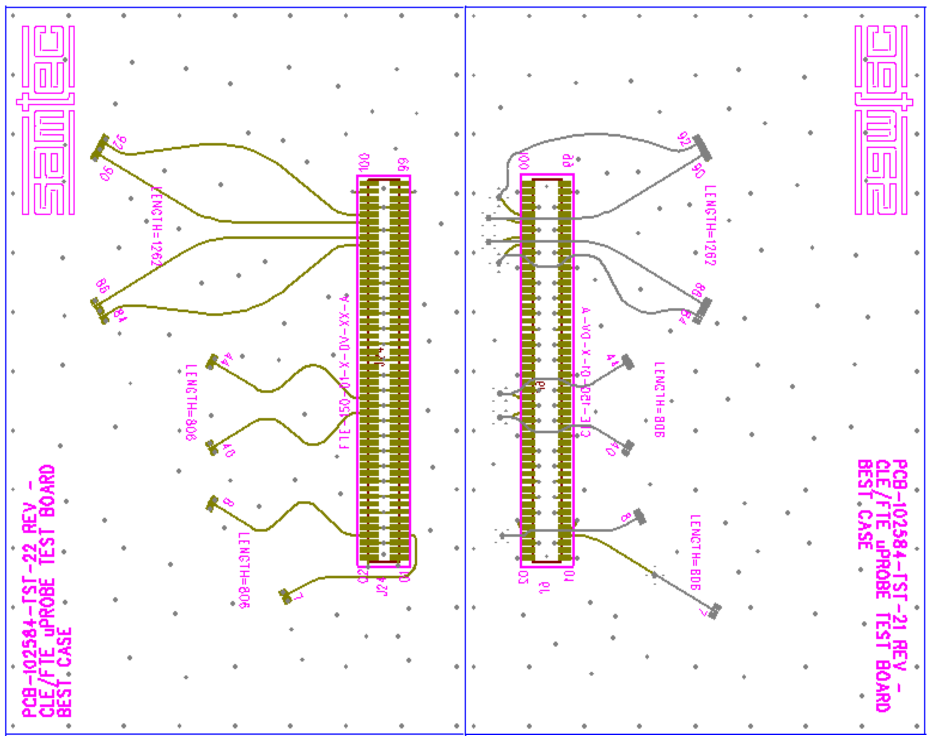
Single-Ended:

Crosstalk Frequency & Time Domain Response Parameters, NEXT, FEXT

Signal Type	Sig. to Gnd. Ratio				
Differential	Case1	Near-End Aggressor:	AW_94-92	Victim:	AW_90-88
	2:1, S:G	Far-End Aggressor:	AW_94-92	Victim:	CLE_90-88
Single-Ended	Case 2	Near-End Aggressor:	AW_40	Victim:	AW_44
	2:1, S:G	Far-End Aggressor:	AW_40	Victim:	CLE_44
Differential	Case 3	Near-End Aggressor:	AW_6-4	Victim:	AW_3-5
	2:1, S:G	Far-End Aggressor:	AW_6-4	Victim:	CLE_3-5

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

PCB-102584-TST, Set 21 & 22 Mapping



Fixture Test Points – CLE/FTE µProbe Test Board, Best Case

Board No.	PCB-102584-TST-21	Socket:	CLE-150-01-G-DV-ES-A
	PCB-102584-TST-22	Terminal:	AW-50-03-G-D-230-075-ES-A

Transmission and Reflection Test Parameters:

Insertion Loss, Return Loss, Impedance, Propagation Delay

Differential: Tx, port12=AW_90-92, Rx, port34=CLE_90-92

Single-Ended: Tx, port1=AW_44, Rx, port3=CLE_44

Crosstalk Frequency & Time Domain Response Parameters, NEXT, FEXT

Signal Type	Sig. to Gnd. Ratio				
Differential	Case1	Near-End Aggressor:	AW_84-86	Victim:	AW_90-92
	1:1, S:G	Far-End Aggressor:	AW_84-86	Victim:	CLE_90-92
Single-Ended	Case 2	Near-End Aggressor:	AW_42	Victim:	AW_40
	1:1, S:G	Far-End Aggressor:	AW_42	Victim:	CLE_40
Single-Ended	Case 3	Near-End Aggressor:	AW_7	Victim:	AW_8
	1:1, S:G	Far-End Aggressor:	AW_7	Victim:	CLE_8

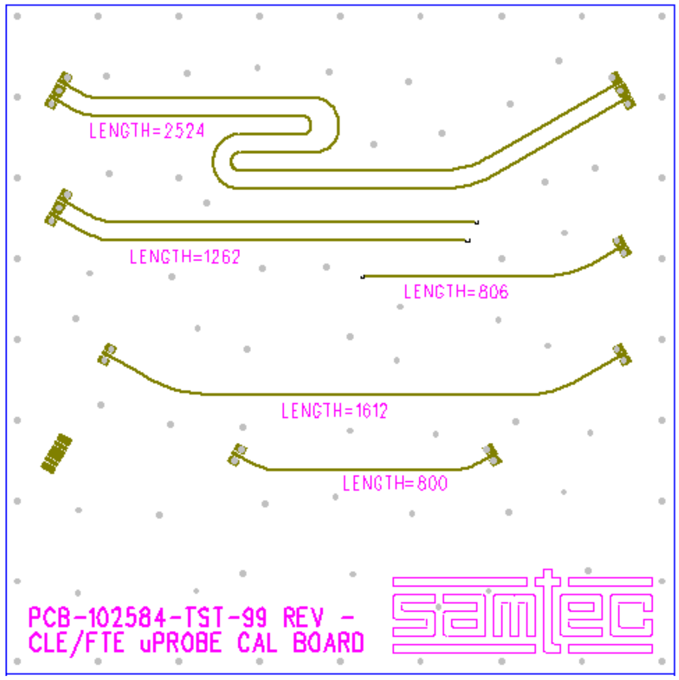
Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

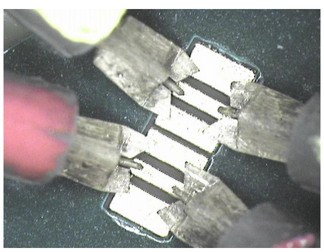
Micro-Probe TDA Calibration Board

Propagation Delay Thru Length
Differential, 2524 mils

Propagation Delay Thru Length
Single-Ended, 1262 mils

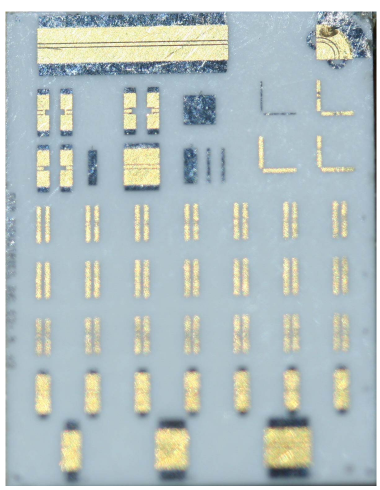
TDA Step Waveform *(Not present)*
Transmission/Reflection Standard
Reference PCB102439_TST-99 Cal
Board





CS-9 Calibration Substrate (SOLT)

OPEN
SHORT
LOAD
THRU



Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 10/22/2010

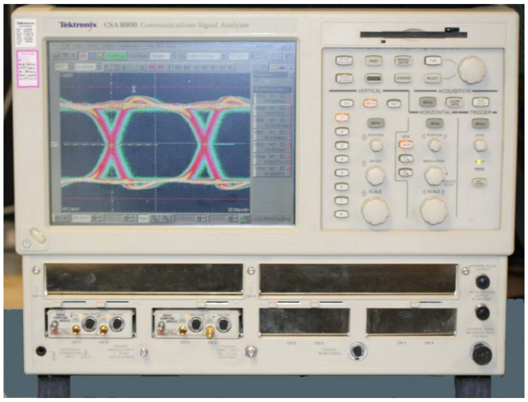
Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

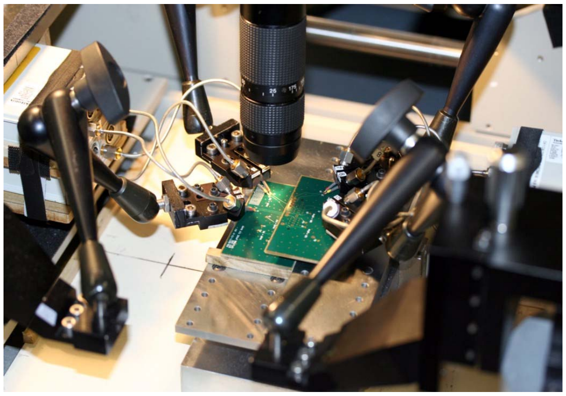
Appendix D – Test and Measurement Setup

Characterization instruments are the Agilent 5230A 4-port PNA analyzer and the Tektronix CSA8000 Communication Signal Analyzer utilizing four Tektronix 80E04 TDR/Sampling Heads. Test sample probing employs a Keyence Video Microscopy system, a Giga Test Labs probing station and Picoprobe 40GHz capable microprobes. Picoprobes’ four hundred and fifty micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available on both the probe table and articulating micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a ≥18 dB return loss, and an isolation of 38 dB providing high-bandwidth and low parasitic measurement results. Combined, the above technology provides a stable measurement environment along with the electrical accuracies for obtaining precise calibrations and signal launch capabilities.

Currently the data captured is real time (CSA8000) which is post-processed to s-parameter results employing TDA IConnect modeling software. However, either instrument capabilities allow for automated capturing, post-processing and graphical waveform representation in both domains. In a move towards full s-parameter reporting, future SI characterization reports will include PNA generated s-parameters utilizing the advantage of SOLT or TRL calibration accuracy. The end game for full s-parameter reporting will be PNA based with TRL calibration and de-embedding accuracy. All s-parameter and timing based measurements will be generated utilizing Advanced Systems Design simulation software. Appendix E will retain procedures for TDA IConnect. Procedures added to Appendix E include PNA s-parameter methods and SOLT calibration. Until full implementation of the s-parameter ADS process, impedance, propagation delay and digital crosstalk will continue to be generated by the CSA8000. Frequency based PNA s-parameter measurements will replace the IConnect processed s-parameter data. Those PNA s-parameter formats include insertion loss, return loss and RF crosstalk.

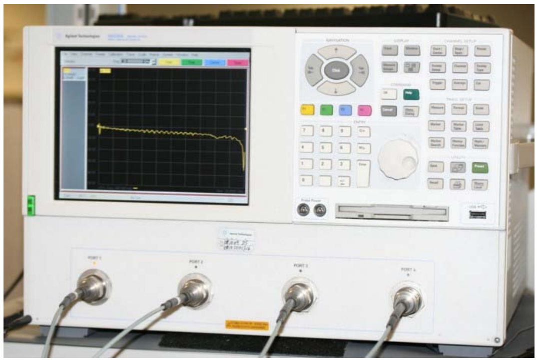
CSA8000 Time Domain Test Setup

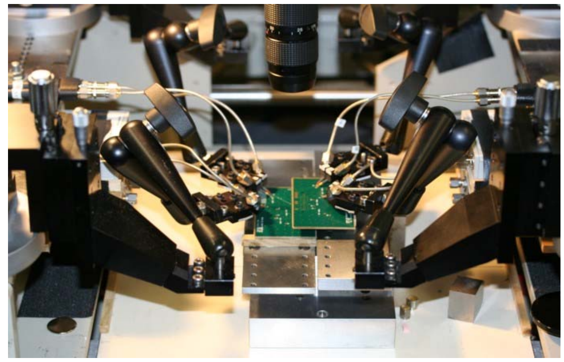




Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

N5230A Frequency Domain (S-Parameter) Test Setup





Test Instruments

QTY	Description
1	Agilent N5230A PNA 300KHz to 20 GHz
1	Tektronix CSA8000 Communication Signal Analyzer
4	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Probe Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
4	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG
1	GGB Industries CS-9 Calibration Substrate (SOLT standards)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

QTY	Description
8	Pasternack Enterprises 2.9mm Semi-Rigid (.086) 6” Cable Assemblies (4)
4	MegaPhase CM40-K1K2-48 Chip Set Cables (40GHz)
4	Tektronix 1 Meter Module Extenders

Calibration Kits

QTY	Description
1	GGB Industries, Picoprobe CS – 9 Calibration Substrate

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded.

Sample Preparation

Determine signal launch and monitoring test points by referencing the detailed pin-out maps provided in Appendix E. Pinout maps names are:

Microprobe Calibration Board, **TDA**
PCB Fixture Set **I**
PCB Fixture Set **II**

It is good practice to terminate all non-active signal lines immediately adjacent to the designated active or quiet signal lines under test.

Frequency Domain Procedures

TDA IConnect S-Parameter Extraction & Processing
Frequency data extraction involves a two-step process. The first step creates the TDR based waveform relationships utilizing a Tektronix CSA8000 time based instrument. The second step involves the conversion of these time-based waveforms into s-parameter format using the TDA Systems IConnect software tool. TDA Systems labels time related conversion waveforms as the *Step* and *DUT* waveform references. This section establishes the setup procedures for defining the *Step* and *DUT* reference for conversion to frequency s-parameters presented in this report.

CSA8000 Setup
Listed below is the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. Functional settings such as window length, number of points and averaging

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

capability determines the instruments frequency boundaries. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process. The single channel pulsed source processes s-parameters in single-ended format. A dual channel differential pulsed source processes s-parameters in differential format.

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss (TDA conversion)
STEP Waveform - determine TD waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Complete the transmission path by inserting a negligible length of transmission standard between the system test probes. Calibration or waveform referencing utilizes a six pad cal structure for each of the probe touchdowns (i.e.; se thru = 3 pads or diff thru = 6 pads). Reference the **TDA** calibration board, and use the 1mm (0.390”) length calibration reflect/transmission structure for TDA step waveform characterization.
DUT Waveform - determine TD waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the TDA reflection/transmission standard and record the measurement. Reference PCB fixture set **II** for Insertion Loss configurations.

Return Loss (TDA conversion)
STEP Waveform – determine TD waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. Calibration or waveform referencing utilizes three pads for each probe touchdown (i.e.; se reflect = 3 pads or diff reflect = 6 pads). Reference the **TDA** calibration board and use the 1mm (0.390”) length calibration reflect/transmission standard for TDA step waveform characterization.
DUT Waveform – determine waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the reflection standard. In this condition cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. Reference PCB fixture set **II** for Return Loss configurations.

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Near-End Crosstalk (TDA conversion)
STEP Waveform – Use Return Loss (RL) step waveform.
DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent near-end signal line. Reference PCB fixture sets **I** and **II** for NEXT configurations.

Far-End Crosstalk (TDA conversion)
STEP Waveform - Use Insertion Loss (IL) step waveform.
DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent far-end signal line. Reference PCB fixture sets **I** and **II** for FEXT configurations.

PNA Calibration & S-Parameter Measurements

Valid S-Parameter measurements require a frequency driven instrument with IO capabilities compatible with the many different mating interfaces of a precision type calibration kit. Requirements meet in this test with the N5230A PNA as the source instrument and the Picoprobe CS-9 substrate serving as the precision SOLT type calibration kit.

N5230A PNA Setup

Frequency Sweep: Linear, 300 KHz to 20 GHz, Date Points: 1601, RBW: 1KHz, Cal Type: (3*) Full 4-port: Defined Calibration Kit ID: 40 – Dual Microprobe, Location: Calibration/Advanced Modify Cal Kit/ ID: 40, Calibration Substrate: **CS-9**,

Calibration Filename: * **Microprobe_ dual_1p2m_3p4m_thru**
Calibrated reflective reference exists at microprobe GSG tip #’s 1, 2, 7 & 8
Calibrated Thru references exist at 1-2 to 8-7 & 1 to 8 or 2-7
Provides s-parameter information for Insertion Loss, Return Loss

Calibration Filename: * **Microprobe_ dual_1p2m_3p4m_next_2**
Calibrated reflective reference exists at microprobe GSG tip #’s 1, 2, 3 & 4
Calibrated Thru references exist at 1-2 to 3-4 & 1 to 3 or 2-4
Provides s-parameter information for RF Near-End Crosstalk

Calibration Filename: * **Microprobe_ dual_1p2m_5p6m_fext**
Calibrated reflection reference plane are at microprobe GSG tip #’s 1, 2, 5 & 6
Calibrated Through reference planes are 1-2 to 5-6 & 1 to 5 or 2-6
Provides s-parameter information for RF Far-End Crosstalk

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315”) Pitch, 9.14mm (0.360”) Stack Height

Time Domain Procedures

Utilize the Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) method for digital type pulse measurements. Impedance and propagation delay characterization utilize TDR measurement methods. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to characterize the SUT.

Impedance (TDR)

Energize the SUT’s signal line(s) with a TDR pulse. The far-end of the energized signal lines are terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω termination) or use quality cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. Reference PCB fixture set **II** for Impedance configurations.

Propagation Delay (TDT)

This test reports differential or single ended signal delay as the measured difference of propagation between a combined electrical length of the input/output signal pads and traces (35 ± 5 ps edge rate) and the device under test (DUT) plus a referenced electrical length of the signal pads and signal traces ($PD^{pads/traces}$- $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$). The recorded delay is the signal delay of the connector only. $PD^{pads/traces}$ is the nomenclature representing the electrical length of PCB signal pads & traces equal to physical lengths of PCB pads & traces entering and leaving the device under test (DUT). The PD^{DUT} + $PD^{pads/traces}$ variable is the mated DUT fixture. Measure the risetime of $PD^{pads/traces}$ waveform & $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$ waveforms. Record the 50% amplitude of each rising edge. The distance in time between the rising edges is the propagation delay of the device under test (DUT). Reference the **TDA** calibration board for trace lengths. Reference PCB fixture set **II** for Propagation Delay configurations.

Near-End Crosstalk (TDT)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the near-end for magnitudes of coupled energy. Terminate adjacent signal lines not under test in the test systems characteristic impedance. Reference both PCB fixture set **I** and fixture set **II** for crosstalk configurations.

Far-End Crosstalk (TDT)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the far-end for magnitudes of coupled energy. Terminate adjacent signal lines not under test into the test systems characteristic impedance. Reference both PCB fixture set **I** and fixture set **II** for crosstalk configurations.

Series: AW/CLE
Description: Surface Mount, 0.8mm (.0315") Pitch, 9.14mm (0.360") Stack Height

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
BC – Best Case crosstalk configuration
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
EC6 – Edge Card with a .635mm signal pad pitch
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
HDV – High Density Vertical
LEC6 – Signal Launch Edge Card with a .635 mm signal pad pitch
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
Z – Impedance (expressed in ohms)