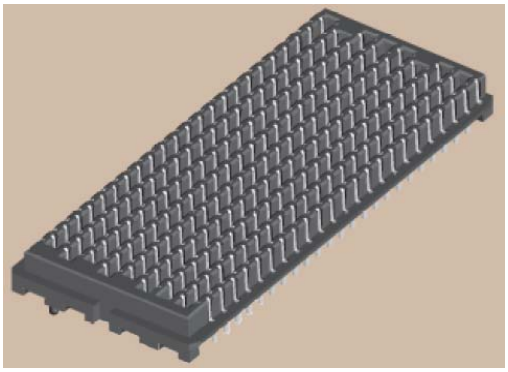
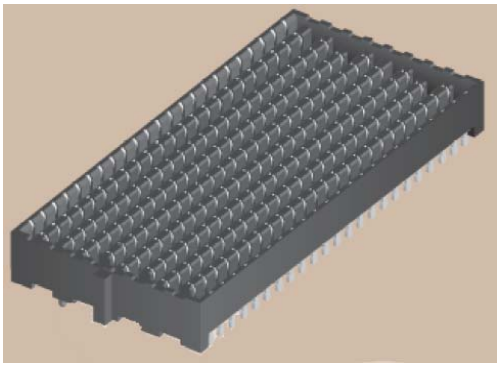
High Speed Characterization Report

DPAM-23-07.0-H-8-1-A



Mates with

DPAF-23-03.0-H-8-1-A



Description:

Differential Pair High Density Interconnect
2.16mm (.085”) x 2.54mm (.100”) Array
10mm Stack Height

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA
©Samtec, Inc. 2005

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 11/21/2007
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table of Contents

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Connector Overview

DPAM/DPAF is a high density 2.16mm x 2.54 mm pitch differential pair array system for high-speed board-to-board applications. DPAM/DPAF configured properly is capable of Rapid I/O, XAUI, PCI Express and SATA Data Rates. DPAM/DPAF High Density Series is tooled in 8, 15 or 23 differential pairs per row and available in three or eight pair rows. This report reflects both standard and optimized SI configurations for hi-speed electrical characteristics specific to a mated 10mm DPAM/DPAF stack height.

Connector System Speed Rating

DPAM/DPAF Array Series, 2.16mm x 2.54mm (.085" x .100") pitch interconnect, 10mm Stack Height

Signaling	Speed Rating
Single-Ended:	**8.0 GHz / 16 Gbps**
Differentia Pair:	
Standard High Density	**7.0 GHz / 14Gbps**
Optimal High Density	**7.0 GHz / 14Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board's trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

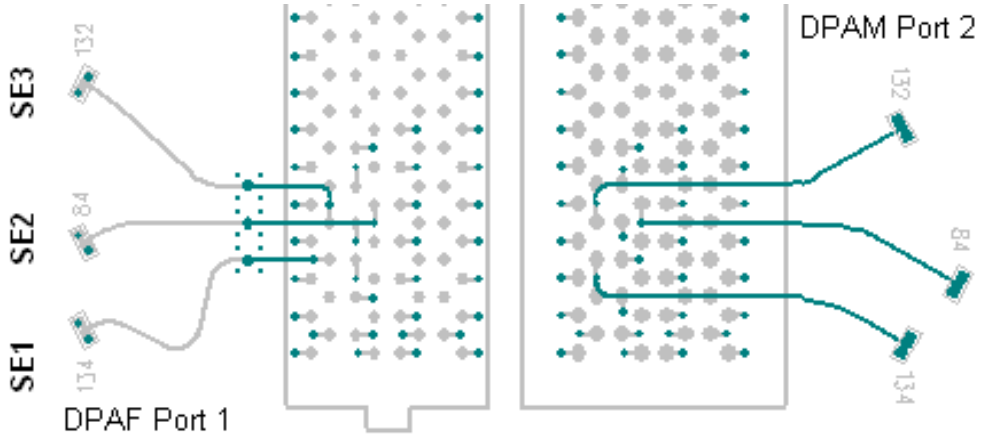
©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Frequency Domain Data Summary

Table 1 - Single-Ended Signaling Performance			
Test Parameter	**Source**	**Victim**	
Insertion Loss	port 1=DPAF_132; port 2=DPAM_132	[redacted]	-3dB @ 7.9 GHz
Return Loss	port1=DPAF_132; port2=DPAM_132	[redacted]	≤ -5dB to 7.9 GHz
Near-End Crosstalk	DPAF _134	DPAF _132	≤ - 15dB to 7.9 GHz
	DPAF _84	DPAF _132	≤ -18dB to 7.9 GHz
Far-End Crosstalk	DPAF _134	DPAM_132	≤ - 15dB to 7.9 GHz
	DPAF _84	DPAM _132	≤ - 15dB to 7.9 GHz

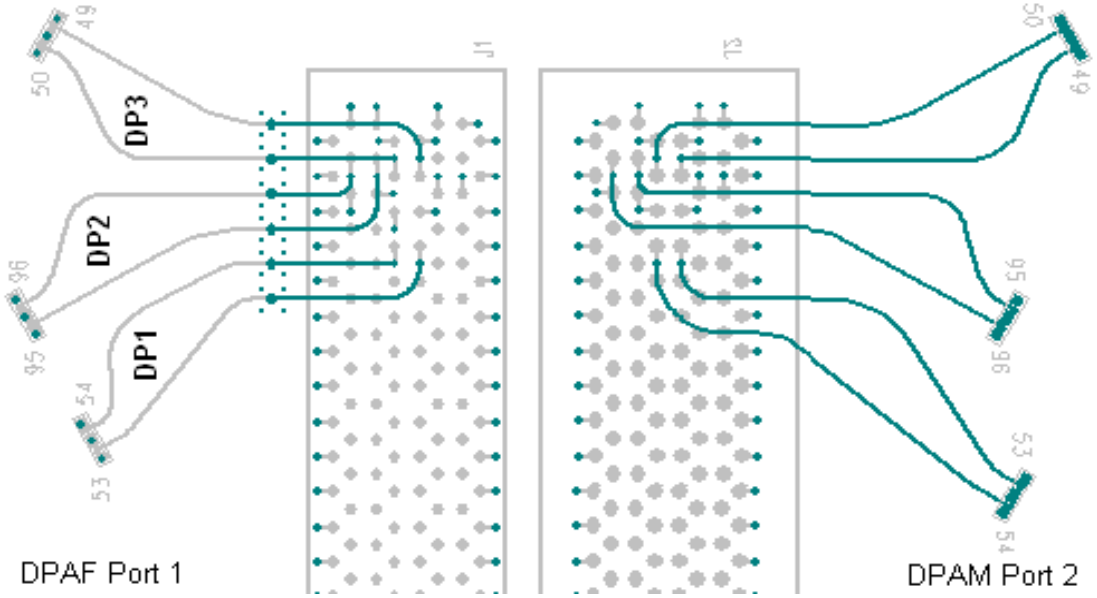
Pin Map (reference Appendix C for full description of test boards)



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table 2 – Optimal Differential Performance			
Test Parameter	**Source**	**Victim**	
Insertion Loss (path1)	port1=DPAF_95_96; port2=DPAM_95_96	[redacted]	-3dB @ 7.0 GHz
Insertion Loss (path2)	port1=DPAF_49_50; port2=DPAM_49_50		-3dB @ 6.8 GHz
Return Loss (path1)	port1=DPAF_95_96; port2=DPAM_95_96		≤ -5dB to 7.0GHz
Return Loss (path2)	port1=DPAF_49_50; port2=DPAM_49_50		≤ -5dB to 6.8 GHz
Near-End Crosstalk	DPAF_53_54	DPAF_49_50	≤ -40dB to 6.8 GHz
	DPAF_95_96	DPAF_49_50	≤ -25dB to 6.8 GHz
Far-End Crosstalk	DPAF_53_54	DPAM_49_50	≤ -38dB to 6.8 GHz
	DPAF_95_96	DPAM_49_50	≤ -30dB to 6.8 GHz

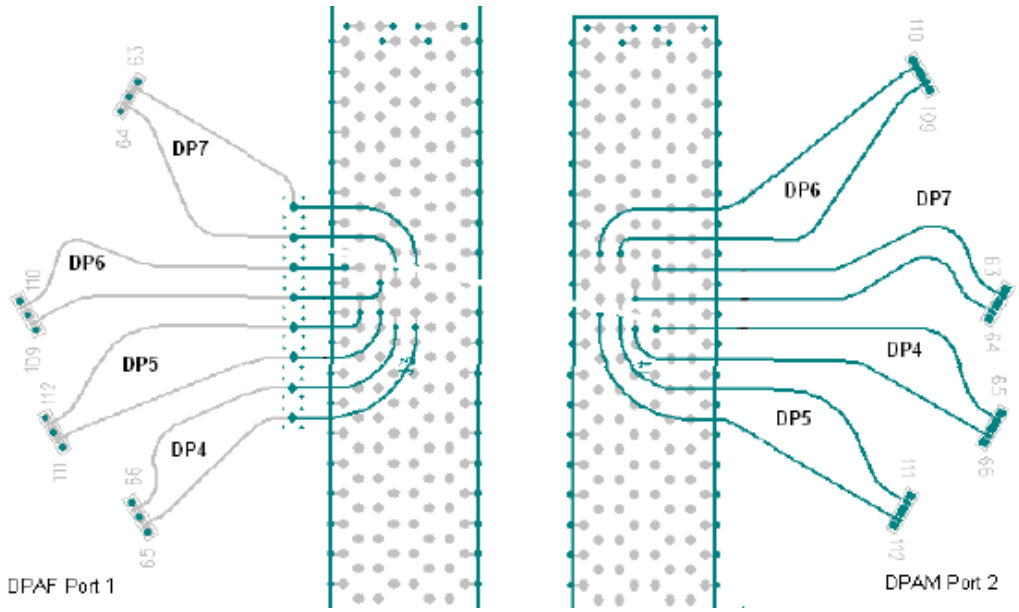
Pin Map (reference Appendix C for full description of test boards)



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table 3 – Standard Differential Performance			
Test Parameter	**Source**	**Victim**	
Insertion Loss (path1)	port1=DPAF_95_96; port2=DPAM_95_96	[redacted]	-3dB @ 6.9 GHz
Insertion Loss (path2)	port1=DPAF_49_50; port2=DPAM_49_50		-3dB @ 6.8 GHz
Return Loss (path1)	port1=DPAF_95_96; port2=DPAM_95_96		≤ -5dB to 6.9GHz
Return Loss (path2)	port1=DPAF_49_50; port2=DPAM_49_50		≤ -5dB to 6.8 GHz
Near-End Crosstalk	DPAF_65_66	DPAF_63_64	≤ -15dB to 6.8 GHz
	DPAF_111_112	DPAF_63_64	≤ -25dB to 6.8 GHz
	DPAF_109_110	DPAF_63_64	≤ -22dB to 6.8 GHz
Far-End Crosstalk	DPAF_65_66	DPAM_63_64	≤ -15dB to 6.8 GHz
	DPAF_111_112	DPAM_63_64	≤ -22dB to 6.8 GHz
	DPAF_109_110	DPAM_63_64	≤ -25dB to 6.8 GHz

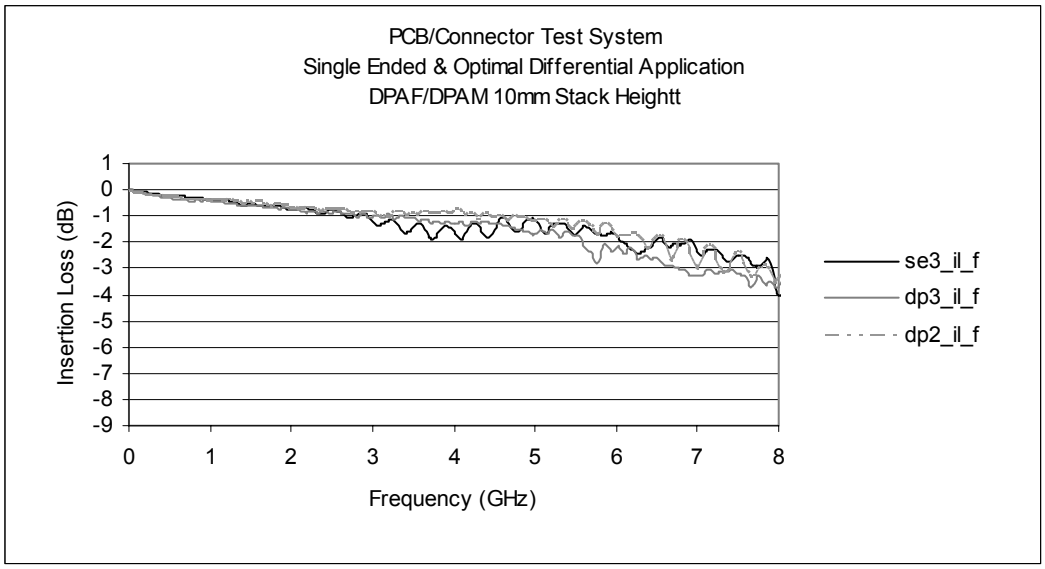
Pin Map (reference Appendix C for full description of test boards)



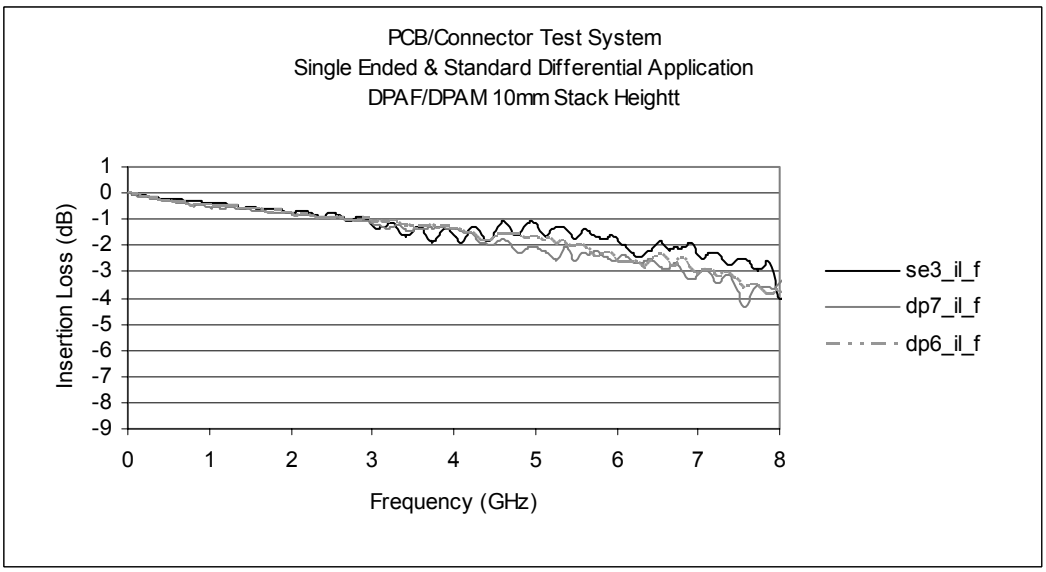
Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Bandwidth Charts – Single-Ended & Differential Insertion Loss

Single-Ended & Optimal Differential Pair



Single-Ended & Standard Differential Pair



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Time Domain Data Summary

Table 4 - Single-Ended Impedance (Ω) – Line 132 (SE3)							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	71.2	68.5	63.4	57.1	54.2	53.1	52.6
Minimum Impedance	42.9	47.0	48.8	50.1	50.3	50.3	50.4

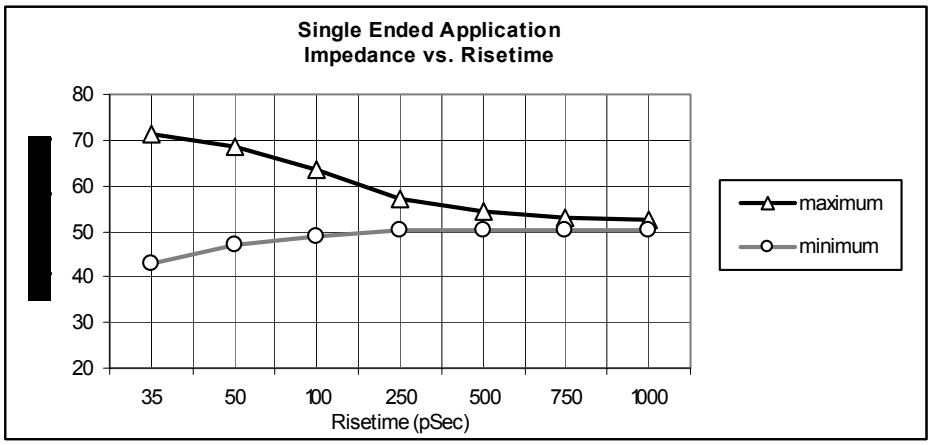
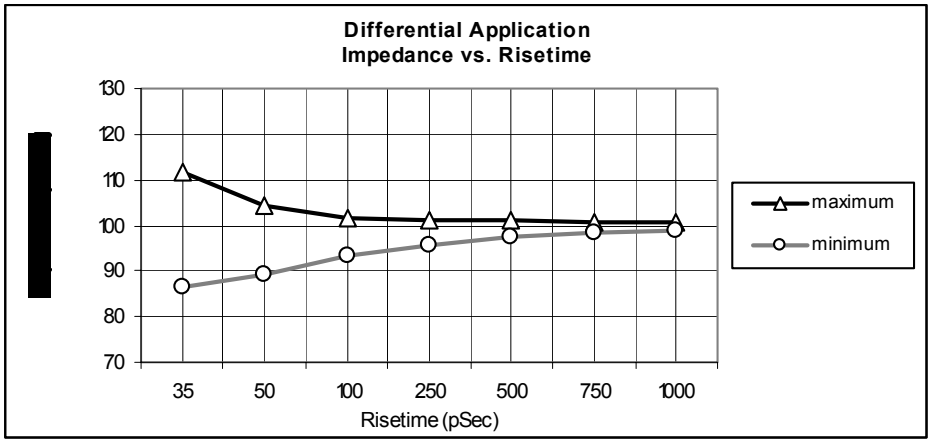


Table 5 - Optimal Differential Impedance (Ω) – DP2, Pair 95_96							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	111.8	104.4	101.5	101.2	101.1	100.9	100.8
Minimum Impedance	86.6	89.3	93.3	95.9	97.6	98.3	98.9



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table 6 - Optimal Differential Impedance (Ω) – DP3, Pair 49_50							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	109.4	102.9	101.2	100.8	100.7	100.3	100.1
Minimum Impedance	85.2	88.3	92.6	95.4	97.1	97.9	98.5

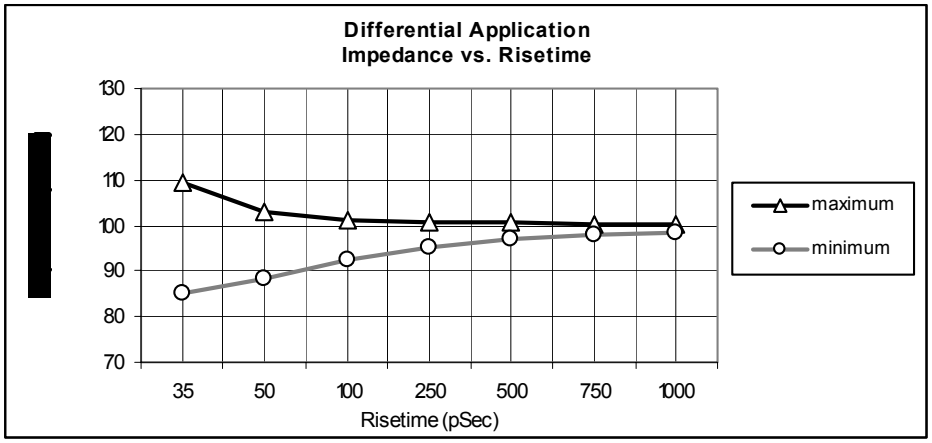
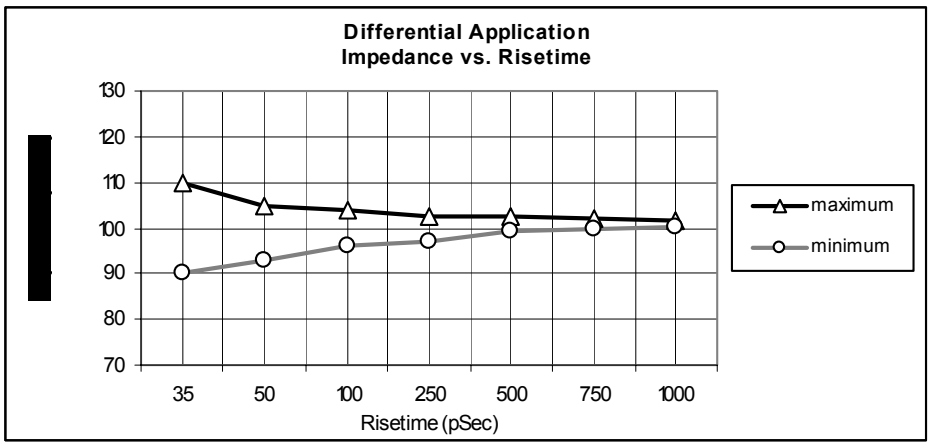
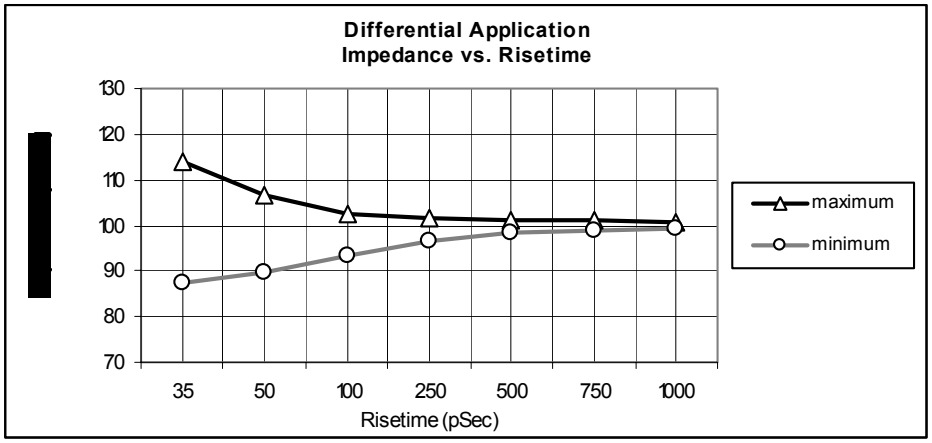


Table 7 – Standard Differential Impedance (Ω) – DP6, Pair 109_110							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	109.8	104.6	103.7	102.7	102.6	101.9	101.7
Minimum Impedance	90.0	92.8	96.0	97.3	99.2	99.9	100.1



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

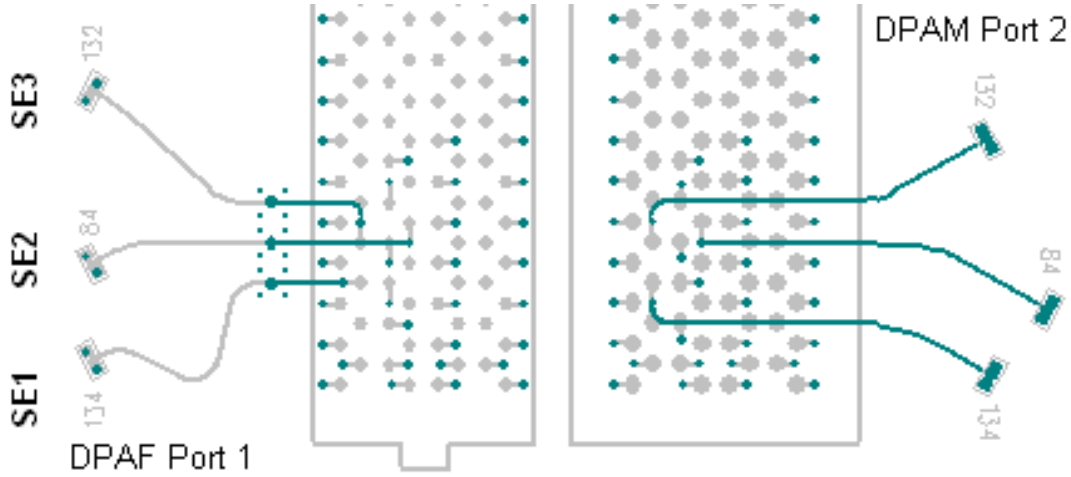
Table 8- Standard Differential Impedance (Ω) – DP7, Pair 49_50							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	113.8	106.6	102.3	101.7	101.3	101.0	100.9
Minimum Impedance	87.5	89.6	93.6	96.7	98.5	99.1	99.3



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table 9- Single-Ended Crosstalk (%)									
Input (t_r)	**Source**	**Victim**	**30±5ps**	**50ps**	**100ps**	**250ps**	**500ps**	**750ps**	**1ns**
NEXT	DPAF _134	DPAF _132	4.7	3.8	3.3	2.0	1.1	< 1.0%	< 1.0%
	DPAF _84	DPAF _132	3.4	1.9	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DPAF _134	DPAM_132	4.0	2.6	1.8	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF _84	DPAM _132	4.7	3.1	1.8	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)

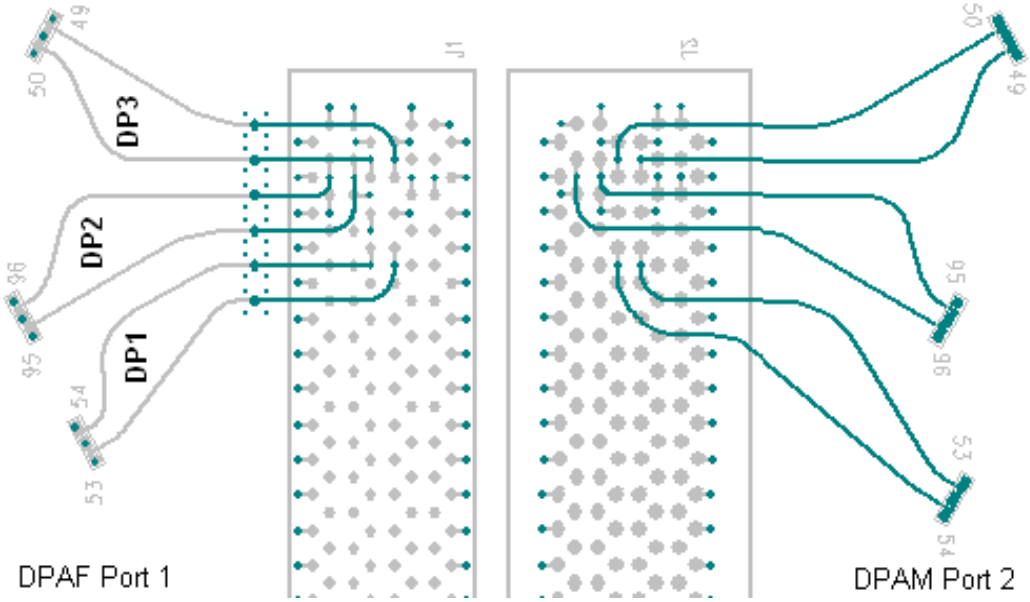


Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table 10 – Optimal Differential Crosstalk (%)

Input (t_r)	Source	Victim	30±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	DPAF_53_54	DPAF_49_50	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF_95_96	DPAF_49_50	2.3	1.9	1.6	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DPAF_53_54	DPAM_49_50	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF_95_96	DPAM_49_50	1.6	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Table 11 – Standard Differential Crosstalk (%)									
Input (t_r)	**Source**	**Victim**	**30±5ps**	**50ps**	**100ps**	**250ps**	**500ps**	**750ps**	**1ns**
NEXT	DPAF_65_66	DPAF_63_64	2.6	2.1	1.7	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF_111_112	DPAF_63_64	1.8	1.7	1.5	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF_109_110	DPAF_63_64	2.4	1.8	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DPAF_65_66	DPAM_63_64	1.8	1.2	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF_111_112	DPAM_63_64	2.1	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DPAF_109_110	DPAM_63_64	1.2	<1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)

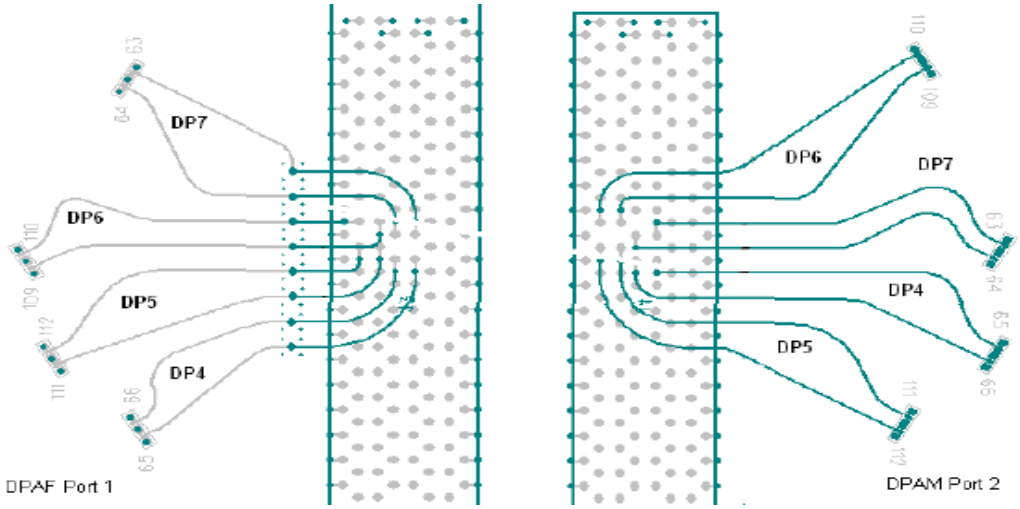


Table 12 – Propagation Delay				
Configuration	**Sig. Path**	Mated Connector Only	**Sig. Path**	Mated Connector Only
Single-Ended	SE3, 132	101ps		-
Optimal Differential	DP2, 95_96	99ps	DP2, 49_50	97ps
Standard Differential	DP6, 109_110	97ps	DP7, 63_64	96ps

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high-speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others; connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

For this connector, the following array configurations are evaluated:

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

	open pin field	X	grounded pin field

P# signal aggressor or signal victim pins

Single-Ended

G45	G43	G41	G39	G37	G35	G33	G31	G29	G27	G25	G23	G21	G19	G17	G15	G13	G11	G9	G7	G5	G3	G1	
	138	136	134	132	130	128	126	124	122	120	118	116	114	112	110	108	106	104	102	100	98	96	94
	137	135	133	131	129	127	125	123	121	119	117	115	113	111	109	107	105	103	101	99	97	95	93
92	90	88	86	84	82	80	78	76	74	72	70	68	66	64	62	60	58	56	54	52	50	48	
91	89	87	85	83	81	79	77	75	73	71	69	67	65	63	61	59	57	55	53	51	49	47	
	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2
	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
G46	G44	G42	G40	G38	G36	G34	G32	G30	G28	G26	G24	G22	G20	G18	G16	G14	G12	G10	G8	G6	G4	G2	

Single-Ended Impedance:

- Vertically Well-referenced (SE1:1), GSGSG

Single-Ended Crosstalk:

- Vertically Well-referenced line; mimics 1:1 S:G ratio (reference SE1:1)
- Horizontal 2:1 S:G ratio (reference SE2:1) GSSG

Only one single-ended signal was driven for crosstalk measurements.

Standard **Optimal**

G45	G43	G41	G39	G37	G35	G33	G31	G29	G27	G25	G23	G21	G19	G17	G15	G13	G11	G9	G7	G5	G3	G1	
	138	136	134	132	130	128	126	124	122	120	118	116	114	112	110	108	106	104	102	100	98	96	94
	137	135	133	131	129	127	125	123	121	119	117	115	113	111	109	107	105	103	101	99	97	95	93
92	90	88	86	84	82	80	78	76	74	72	70	68	66	64	62	60	58	56	54	52	50	48	
91	89	87	85	83	81	79	77	75	73	71	69	67	65	63	61	59	57	55	53	51	49	47	
	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2
	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
G46	G44	G42	G40	G38	G36	G34	G32	G30	G28	G26	G24	G22	G20	G18	G16	G14	G12	G10	G8	G6	G4	G2	

Differential Impedance:

- Standard lines reference to perimeter ground pins
- Optimal lines reference to adjacent ground pins

Differential Crosstalk:

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

- Standard lines reference to perimeter ground pins
- Optimal lines reference to adjacent ground pins

Only one differential pair was driven for crosstalk measurements.

In all cases where a center ground blade is present in the connector it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect, can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 35 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data
Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

generating the SUT's frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Time Domain Data
Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 35 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 35 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

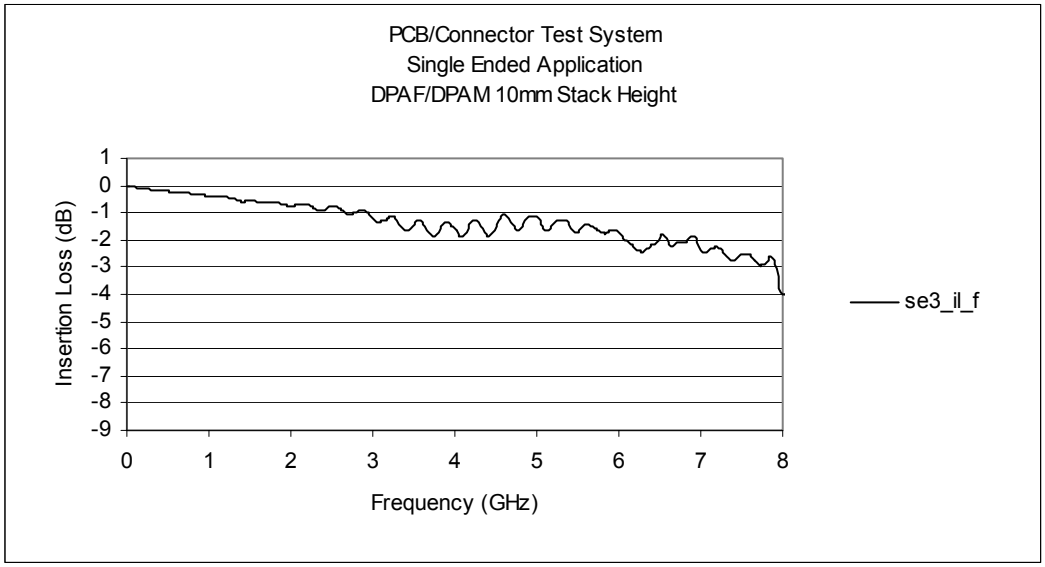
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Appendix A – Frequency Domain Response Graphs

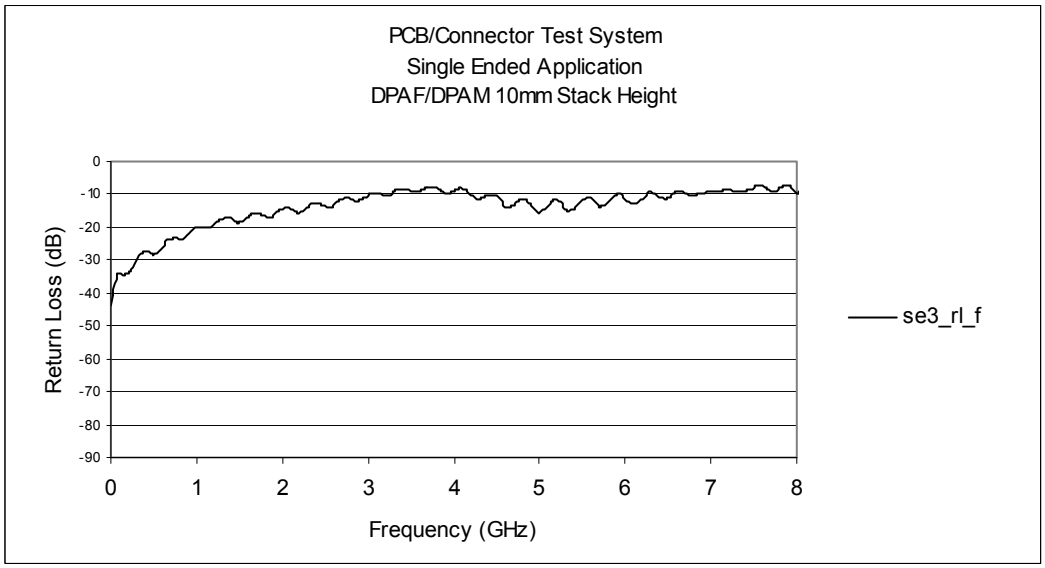
Single-Ended Application – Insertion Loss

Configuration: port1=DPAF_132; port3=DPAM_132



Single-Ended Application – Return Loss

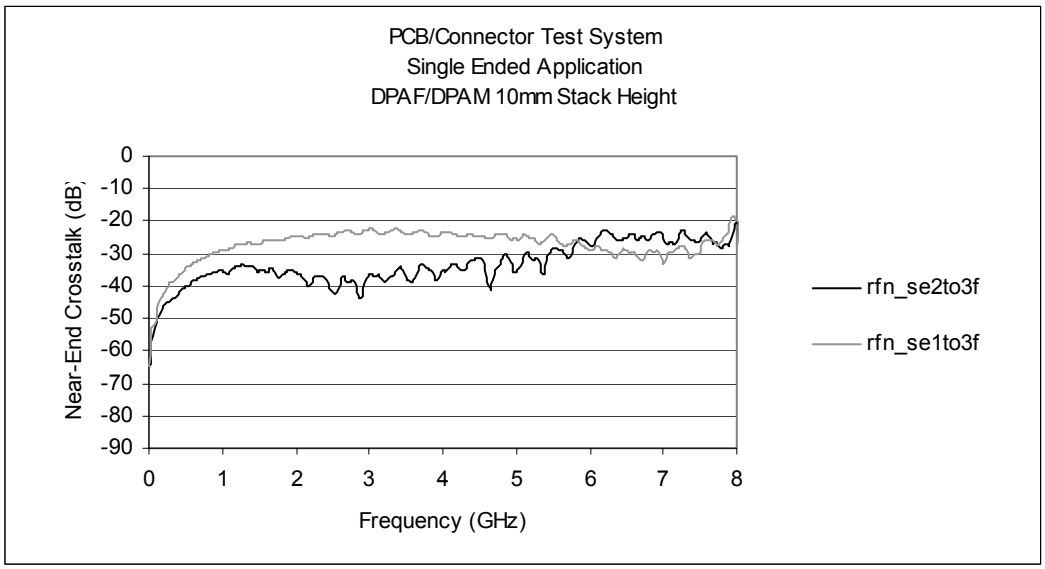
Configuration: port1=DPAF_132; port3=DPAM_132



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

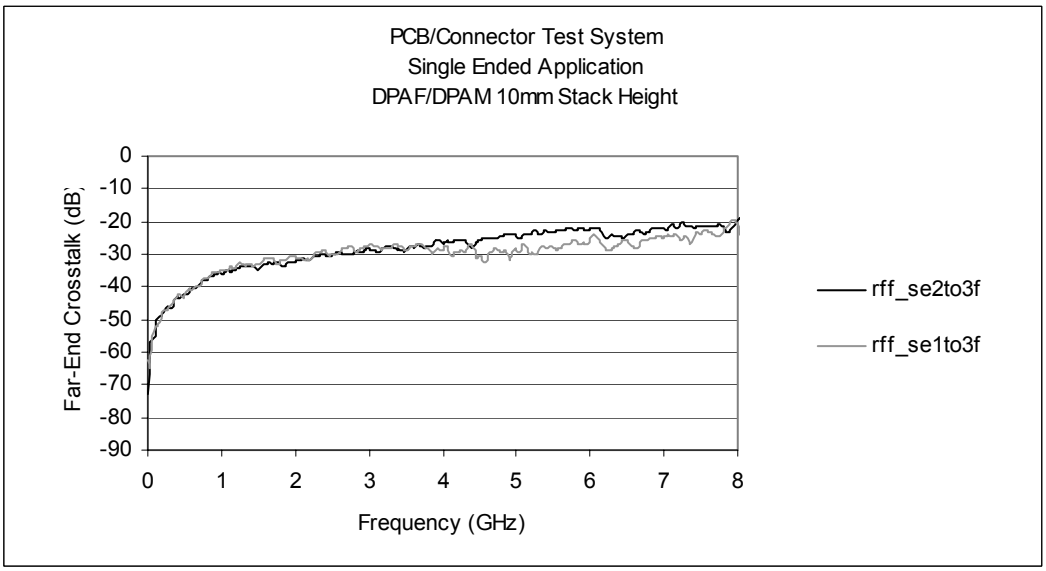
Single-Ended Application – NEXT

Configuration: port2=DPAF_84; port2=DPAF_132
Configuration: port2=DPAF_134; port1=DPAF_132



Single-Ended Application – FEXT

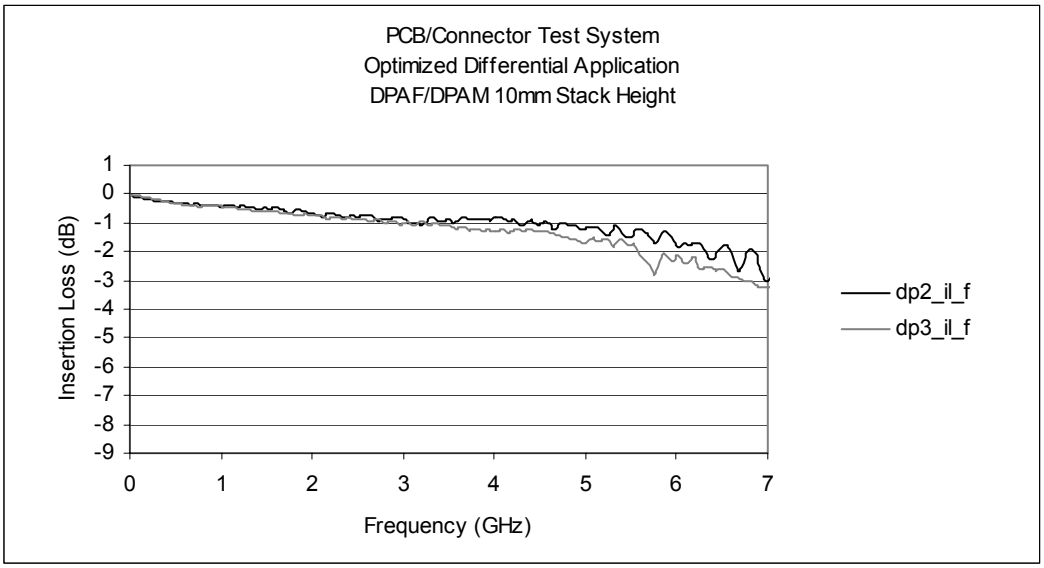
Configuration: port2=DPAF_84; port2=DPAM_132
Configuration: port2=DPAF_134; port1=DPAM_132



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

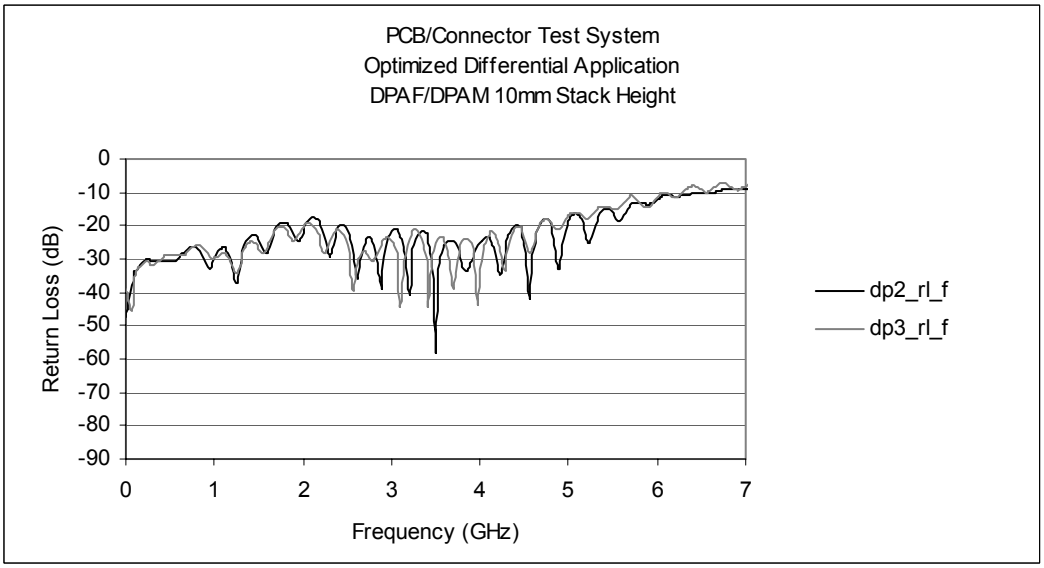
Optimized Differential Application – Insertion Loss

Configuration: port2=DPAF_95_96; port4=DPAM_95_96
Configuration: port1=DPAF_49_50; port3=DPAM_49_50



Optimized Differential Application – Return Loss

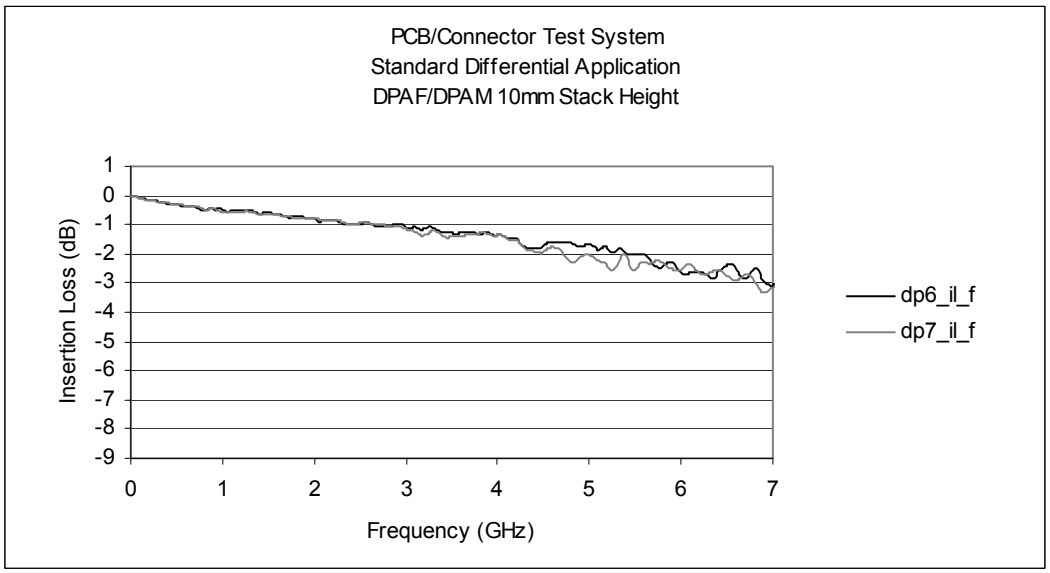
Configuration: port2=DPAF_95_96; port4=DPAM_95_96
Configuration: port1=DPAF_49_50; port3=DPAM_49_50



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

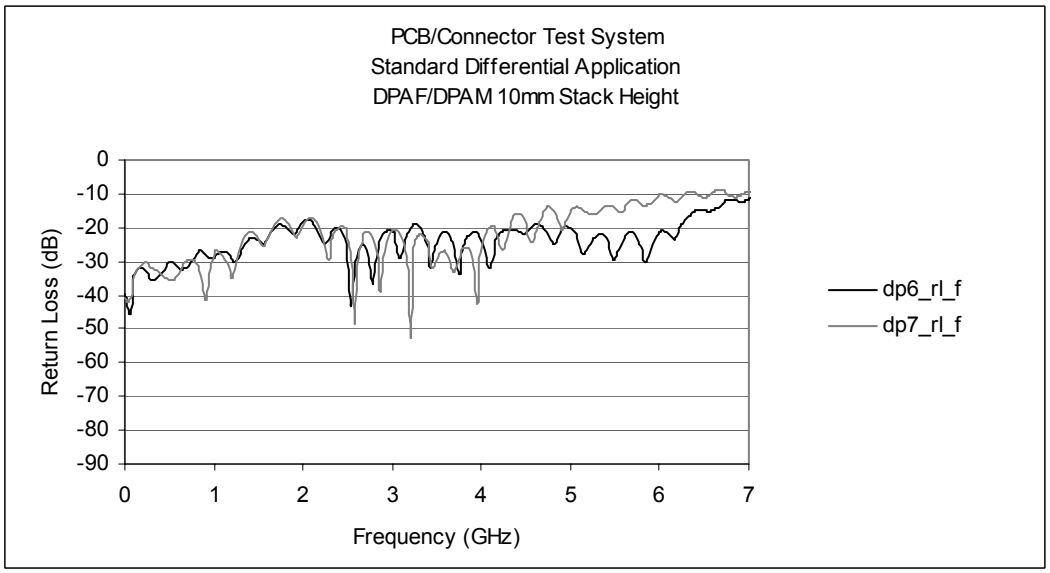
Standard Differential Application – Insertion Loss

Configuration #1: port2=DPAF_109_110; port3=DPAM_109_110
Configuration #2: port1=DPAF_63_64; port4=DPAM_63_64



Standard Differential Application – Return Loss

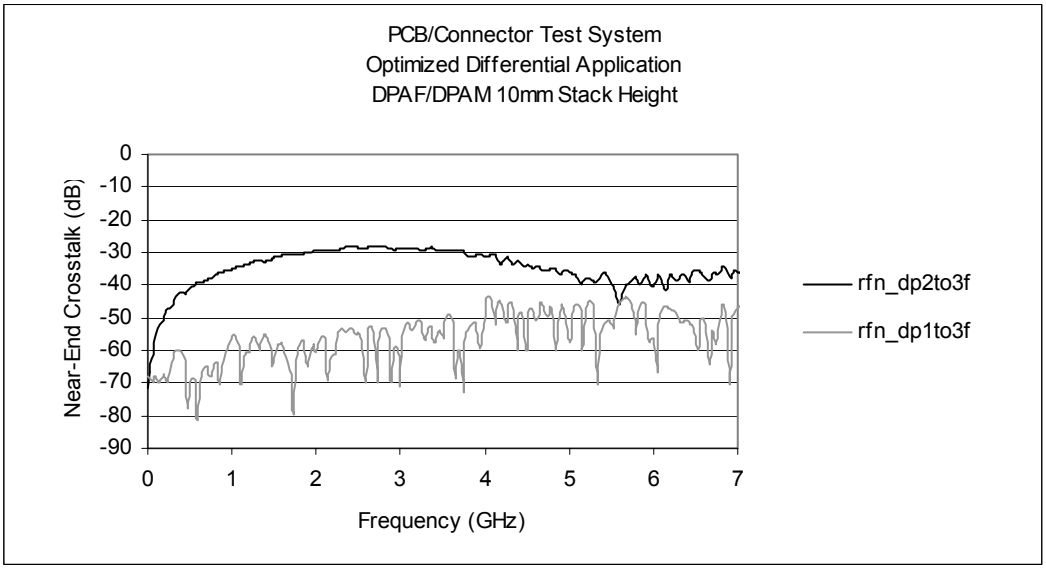
Configuration #1: port2=DPAF_109_110; port3=DPAM_109_110
Configuration #2: port1=DPAF_63_64; port4=DPAM_63_64



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

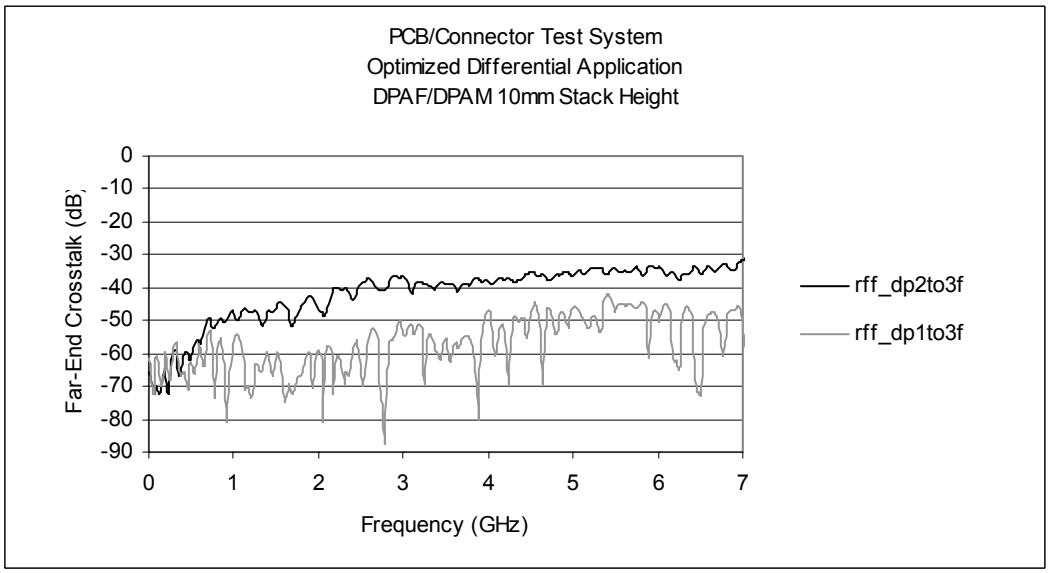
Optimized Differential Application – NEXT Configurations

Configuration: port2=DPAF_95_96; port1=DPAF_49_50
Configuration: port2=DPAF_53_54; port1=DPAF_49_50



Optimized Differential Application – FEXT Configurations

Configuration: port2=DPAF_95_96; port3=DPAM_49_50
Configuration: port2=DPAF_53_54; port3=DPAM_49_50

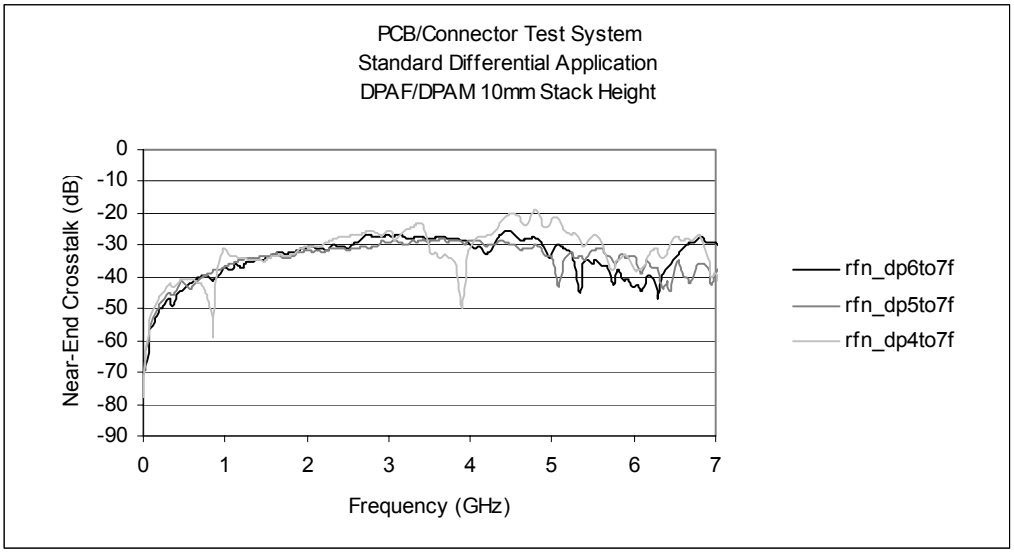


©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

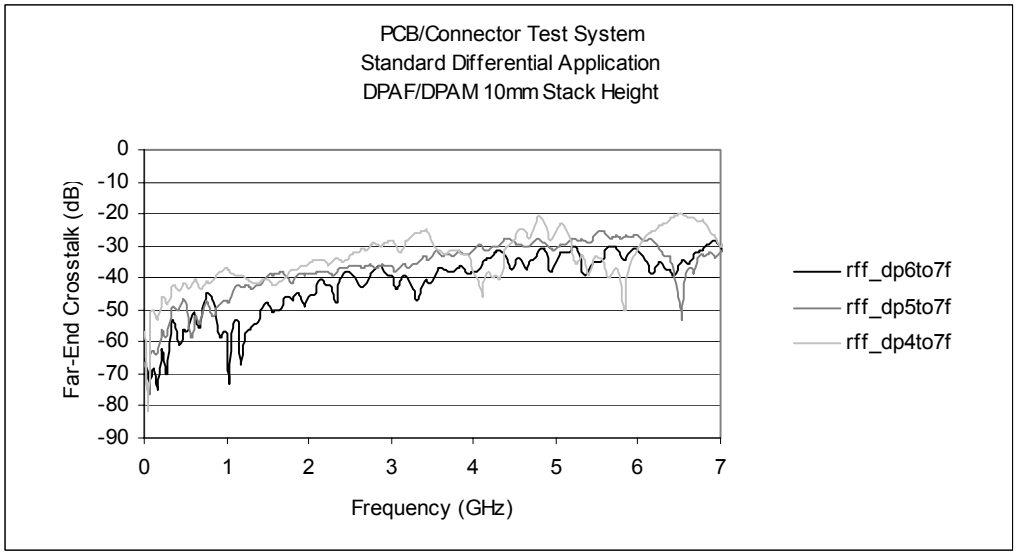
Standard Differential Application – NEXT Configurations

Configuration: port2=DPAF_109_110; port1=DPAF_63_64
Configuration: port2=DPAF_111_112; port1=DPAF_63_64
Configuration: port2=DPAF_65_66; port1= DPAF_63_64



Standard Differential Application – FEXT Configurations

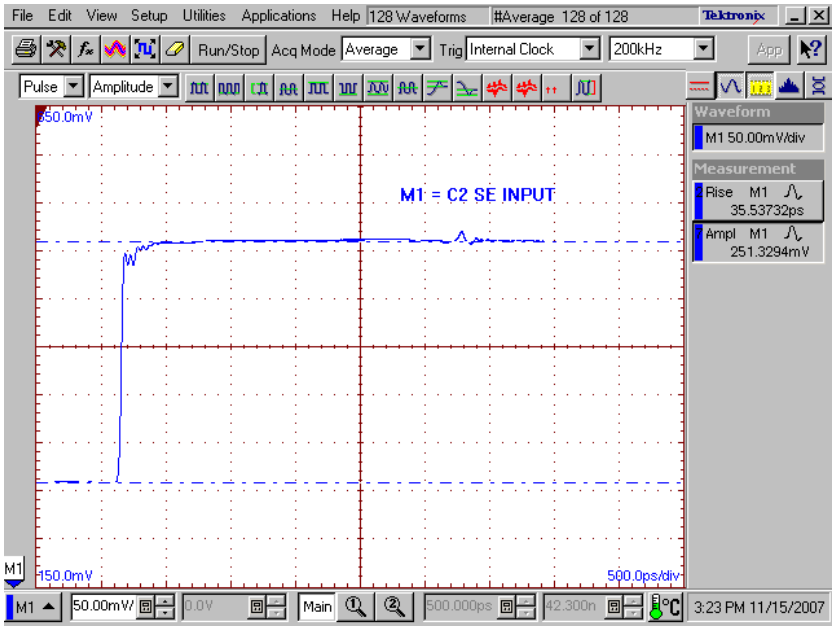
Configuration: port2= DPAF_109_110; port4=DPAM_63_64
Configuration: port2= DPAF_111_112; port4=DPAM_63_64
Configuration: port2= DPAF_65_66; port4=DPAM_63_64



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Appendix B – Time Domain Response Graphs

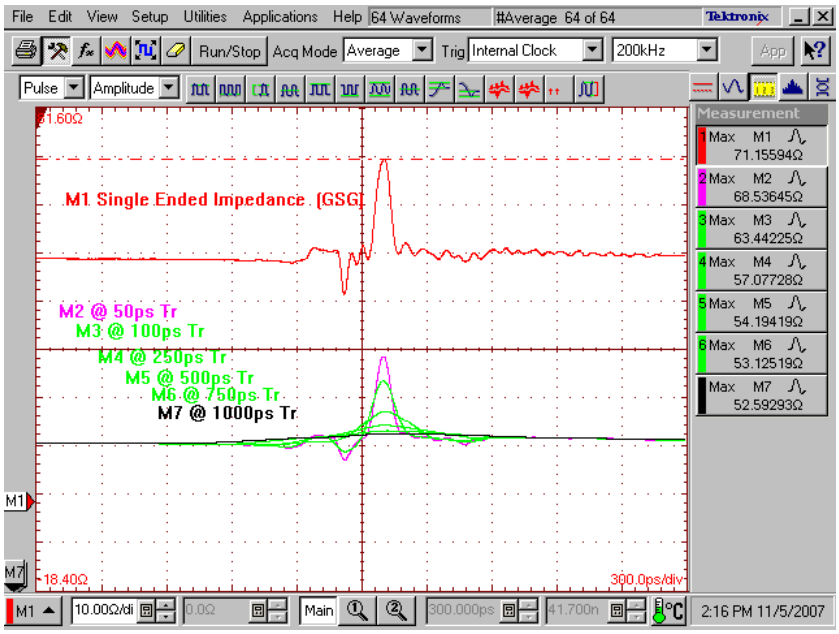
Single-Ended Application – Input Pulse



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

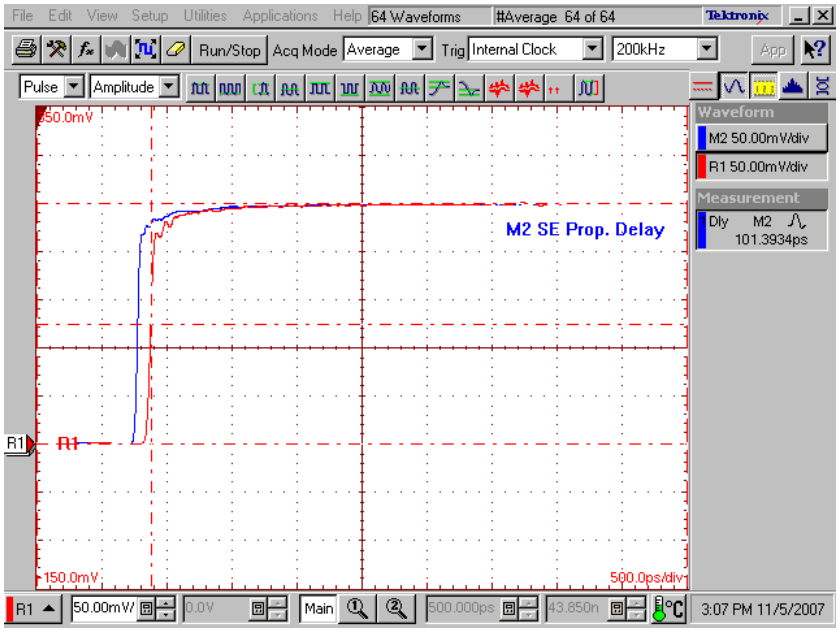
Single-Ended Application – Impedance

Configuration: port1=DPAF_132; port3=DPAM_132



Single-Ended Application – Propagation Delay

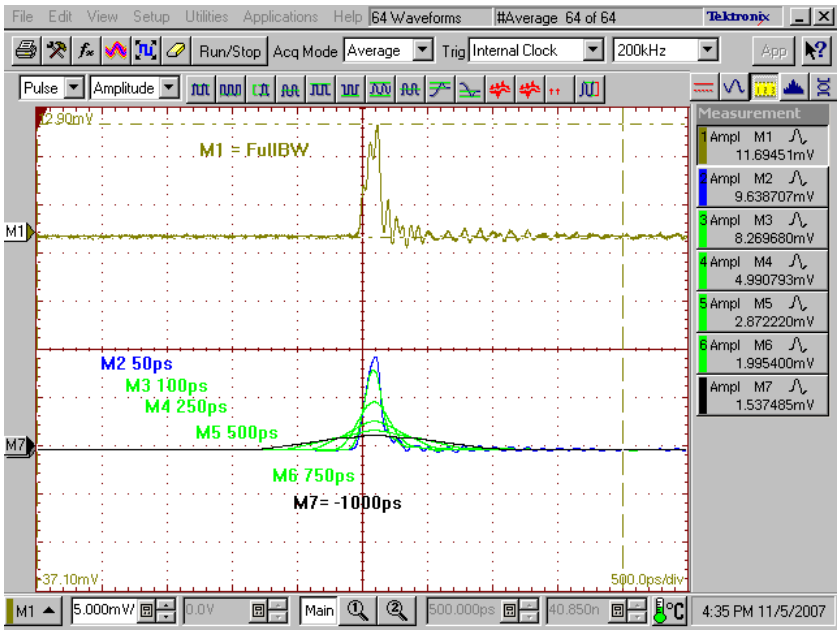
Configuration: port1=DPAF_132; port3=DPAM_132



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

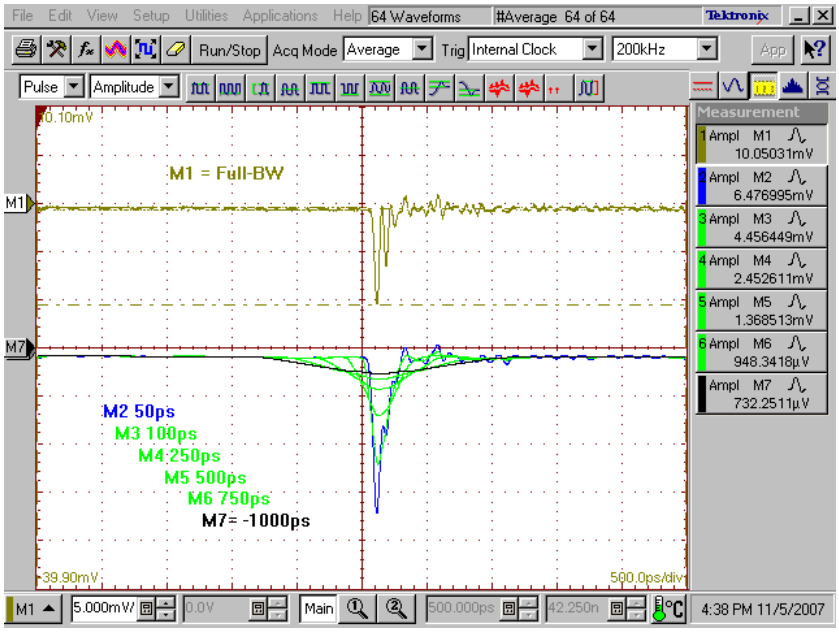
Single-Ended Application – NEXT "SE1 to SE3"

Source: DPAF _134; Victim: DPAM _132



Single-Ended Application – FEXT, "SE 1 to SE3"

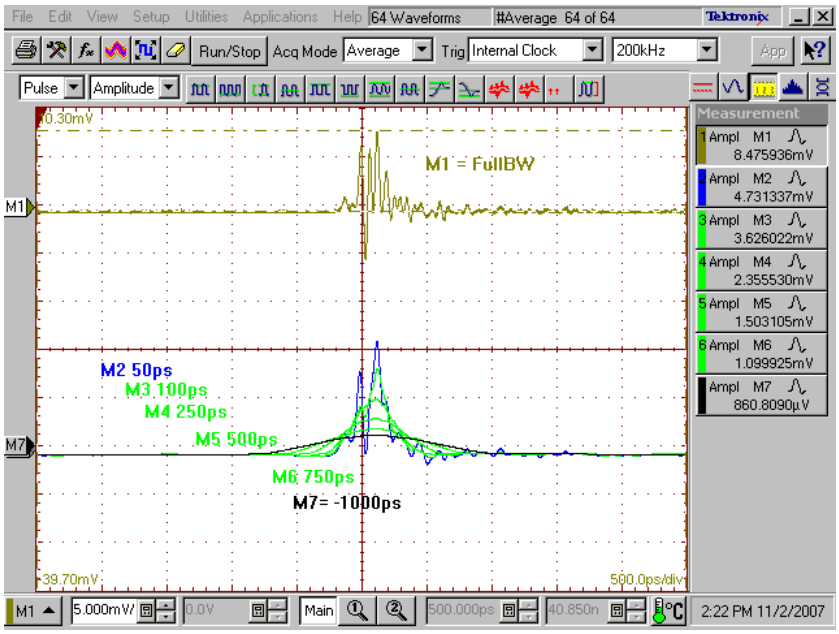
Source: DPAF _134; Victim: DPAM _132



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

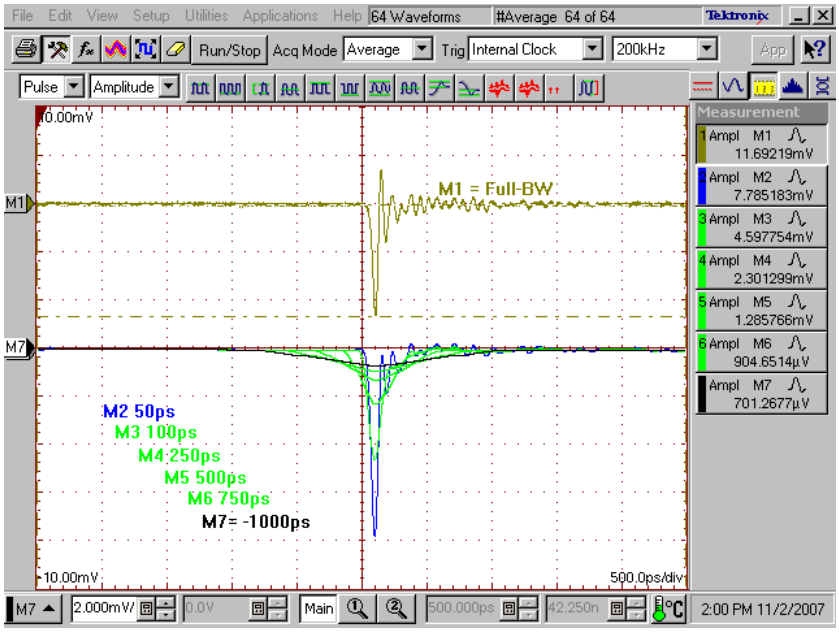
Single-Ended Application – NEXT, "SE2 to SE3"

Source: DPAF _84; Victim: DPAM _132



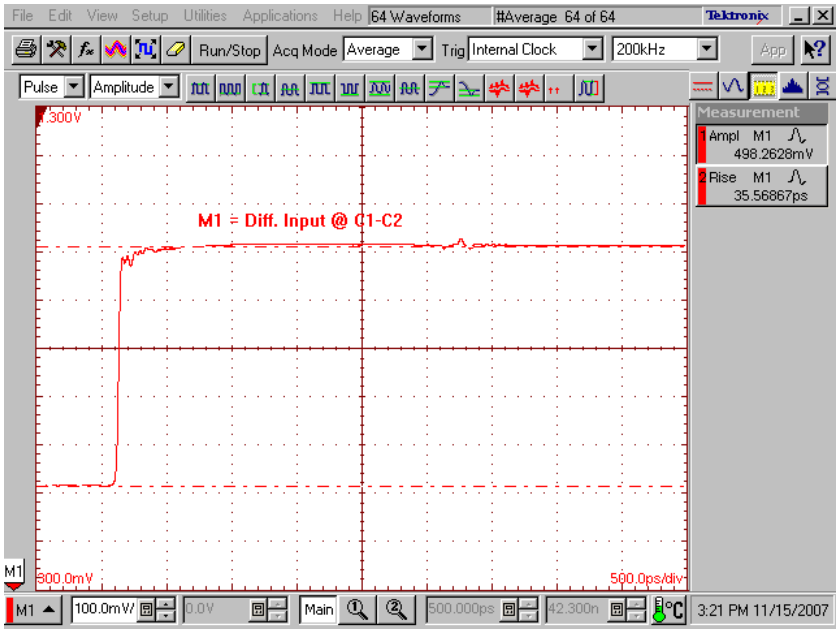
Single-Ended Application – FEXT, "SE2 to SE3"

Source: DPAF_84; Victim: DPAM _132



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

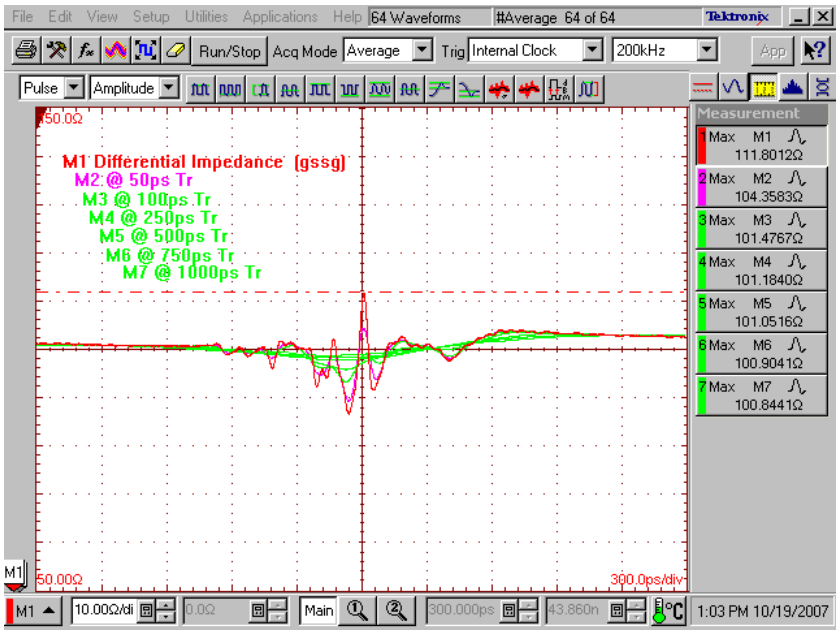
Differential Application – Input Pulse



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

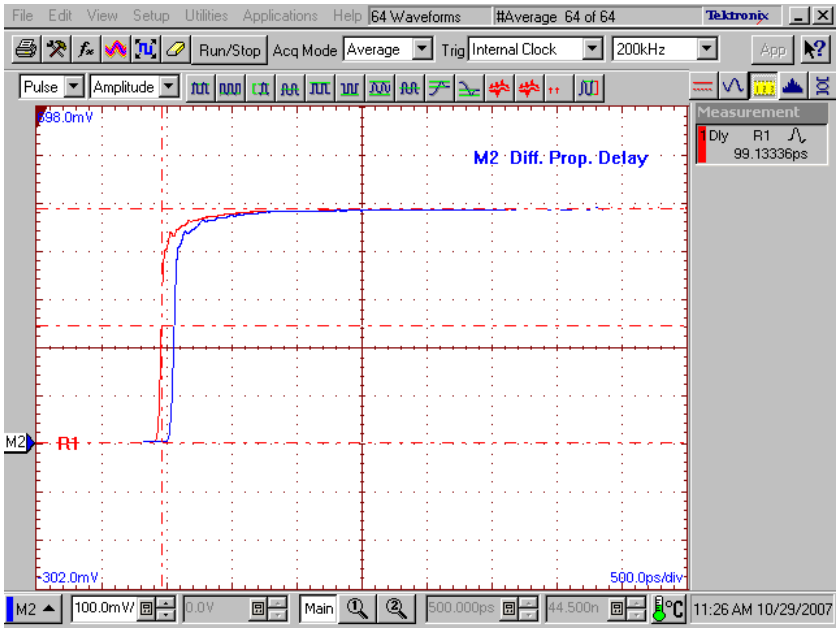
Differential Application –Impedance, Optimized Path 1

Configuration: port2=DPAF_95_96; port4=DPAM_95_96



Differential Application – Propagation Delay, Optimized Path 1

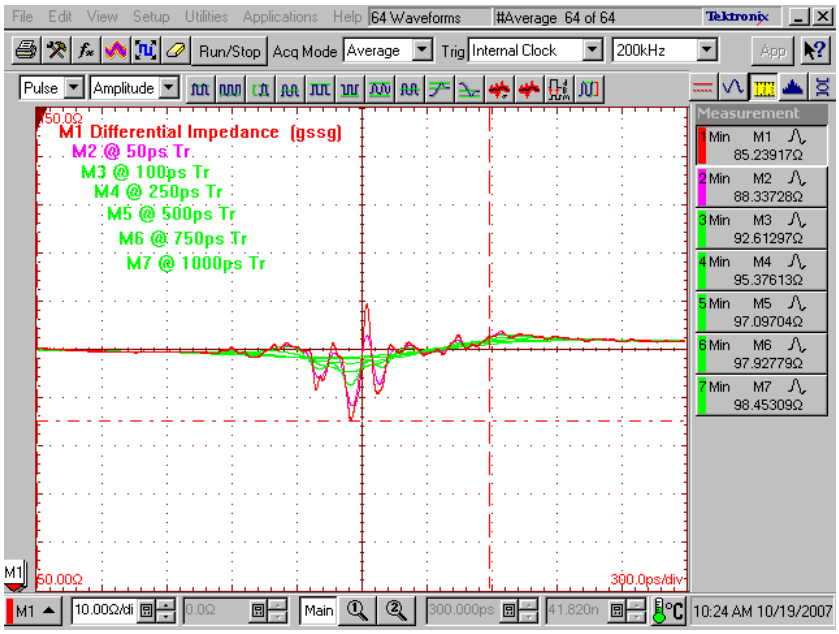
Configuration: port2=DPAF_95_96; port4=DPAM_95_96



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

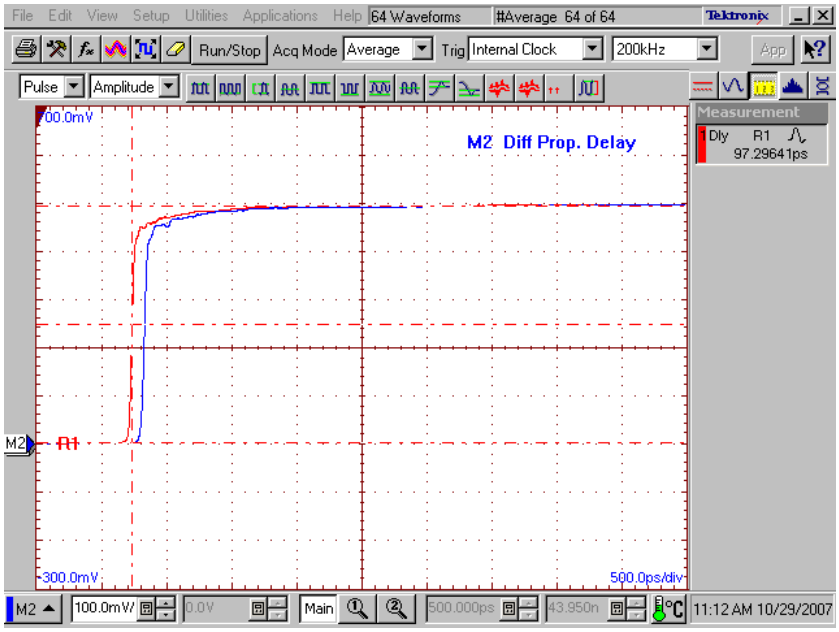
Differential Application –Impedance, Optimized Path 2

Configuration: port1=DPAF_49_50; port3=DPAM_49_50



Differential Application – Propagation Delay, Optimized Path 2

Configuration: port1=DPAF_49_50; port3=DPAM_49_50

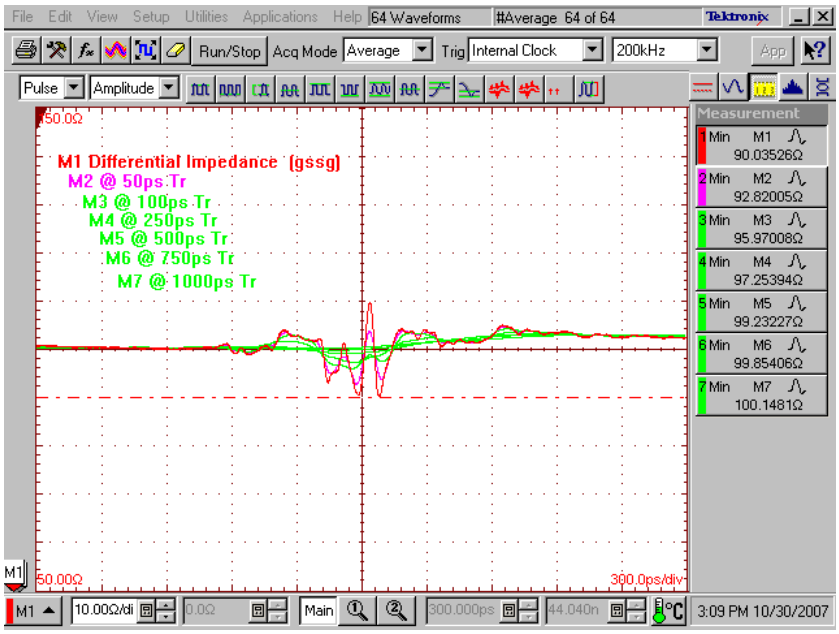


©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

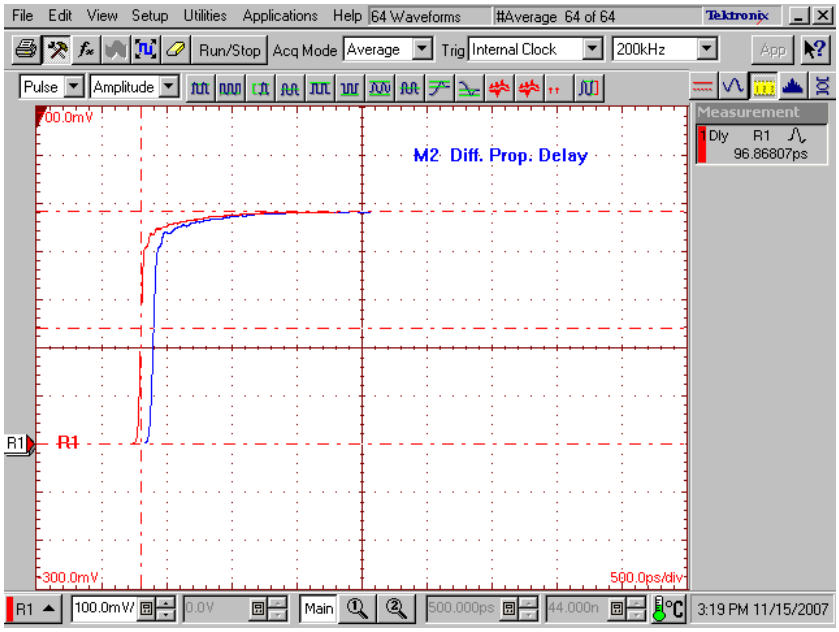
Differential Application –Impedance, Standard Path 1

Configuration: port2=DPAF_109_110; port3=DPAM_109_110



Differential Application – Propagation Delay, Standard Path 1

Configuration: port2=DPAF_109_110; port3=DPAM_109_110

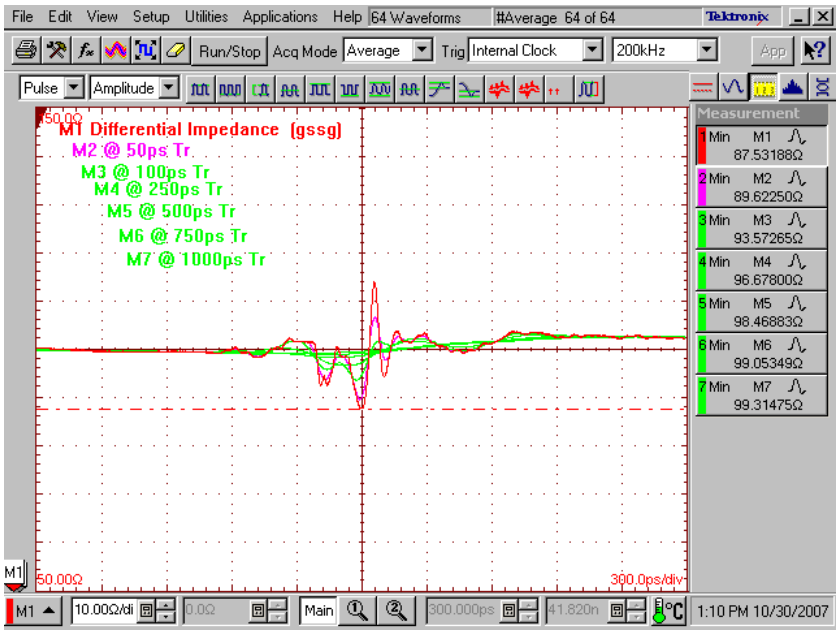


©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

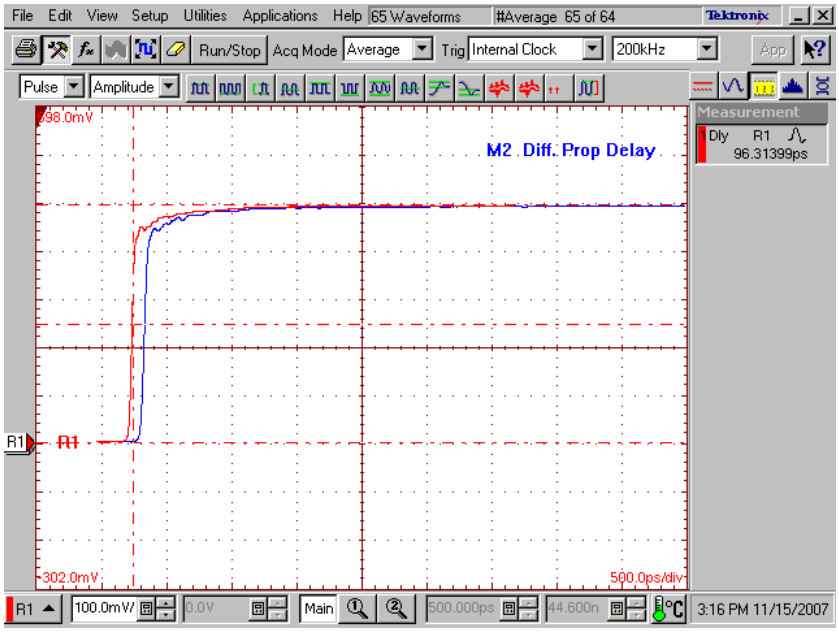
Differential Application –Impedance, Standard Path 2

Configuration: port1=DPAF_63_64; port4=DPAM_63_64



Differential Application – Propagation Delay, Standard Path 2

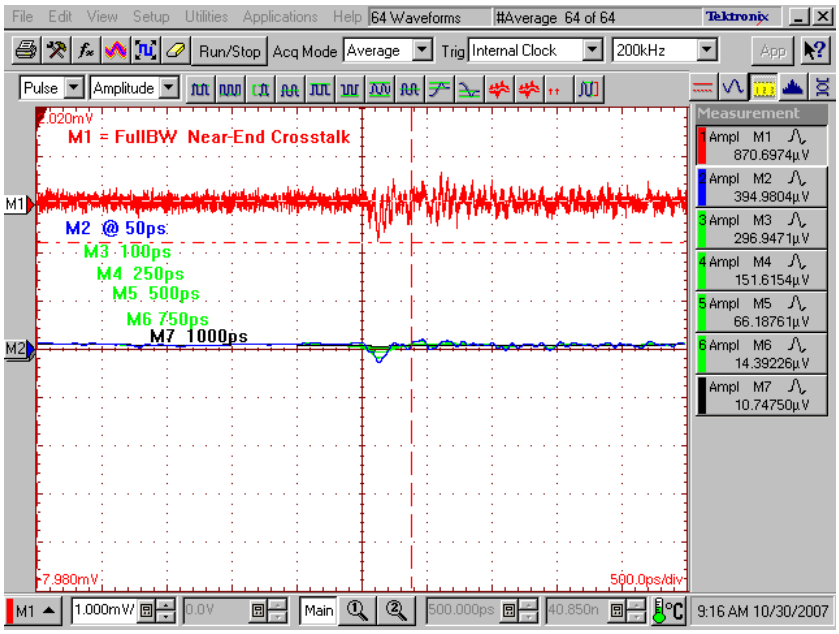
Configuration: port1=DPAF_63_64; port4=DPAM_63_64



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

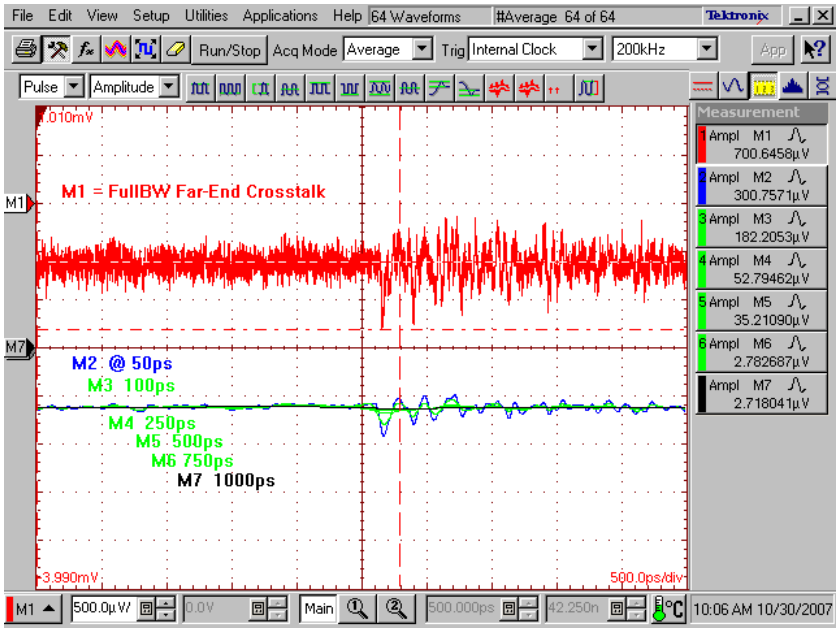
Optimized Differential Application – NEXT, "DP1 to DP3"

Source: DPAF_53_54; Victim: DPAF _49_50



Optimized Differential Application – FEXT, "DP1 to DP3"

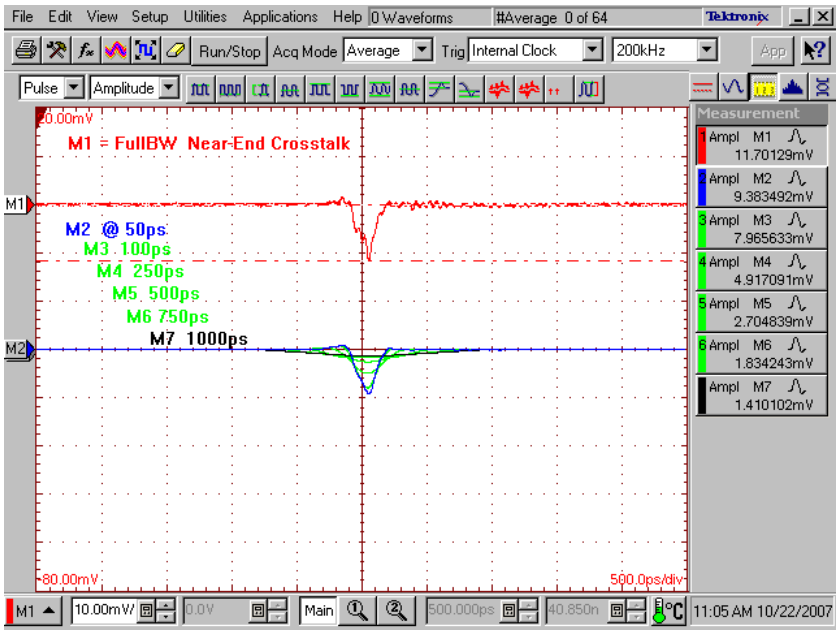
Source: DPAF_53_54; Victim: DPAM _49_50



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

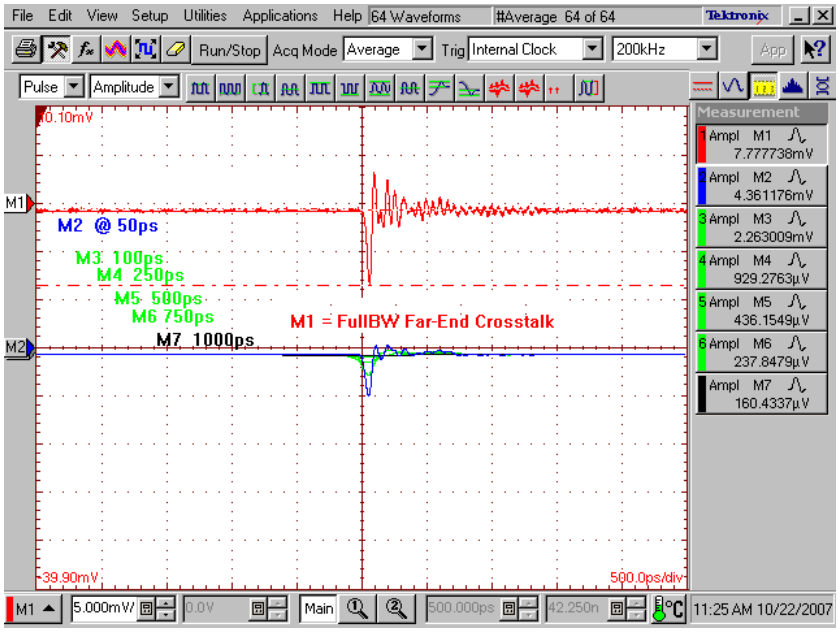
Optimized Differential Application – NEXT, "DP2 to DP3"

Source: DPAF_95_96; Victim: DPAF _49_50



Optimized Differential Application – FEXT, "DP2 to DP3"

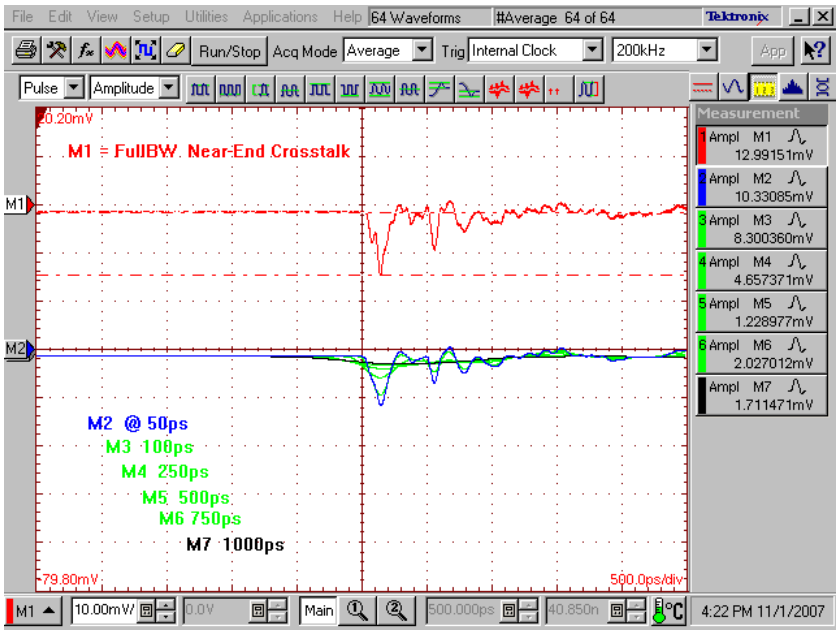
Source: DPAF_95_96; Victim: DPAM _49_50



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

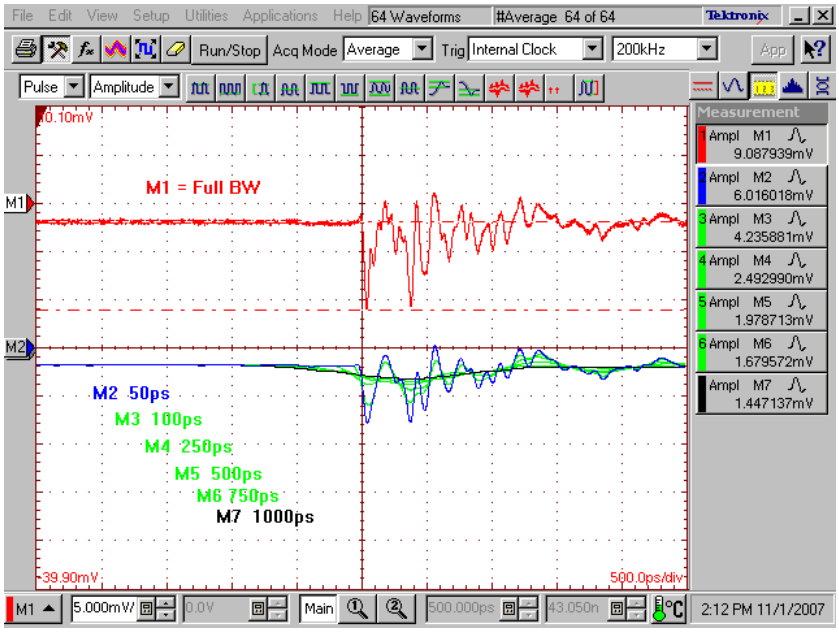
Standard Differential Application – NEXT, "DP4 to DP7"

Source: DPAF_65_66; Victim: DPAF_63_64



Standard Differential Application – FEXT, "DP4 to DP7"

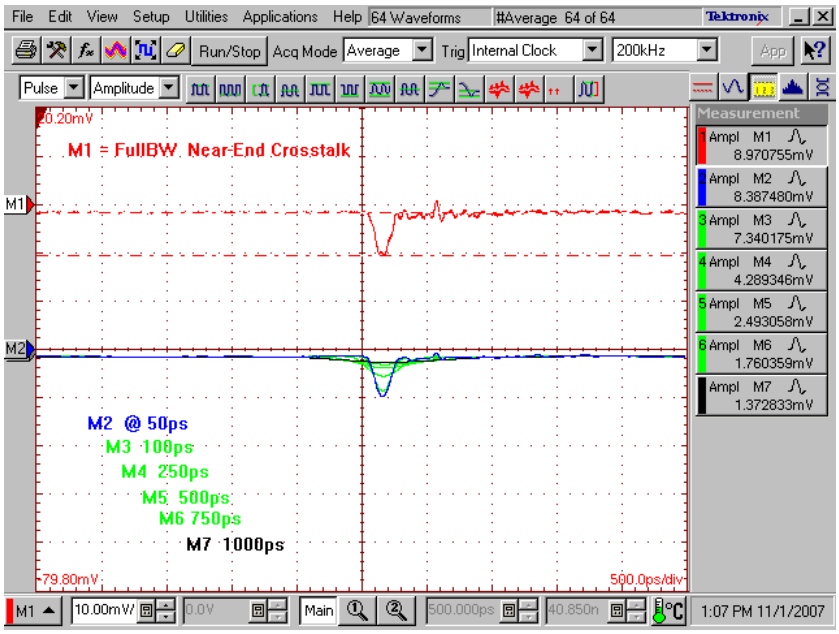
Source: DPAF_65_66; Victim: DPAM_63_64



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

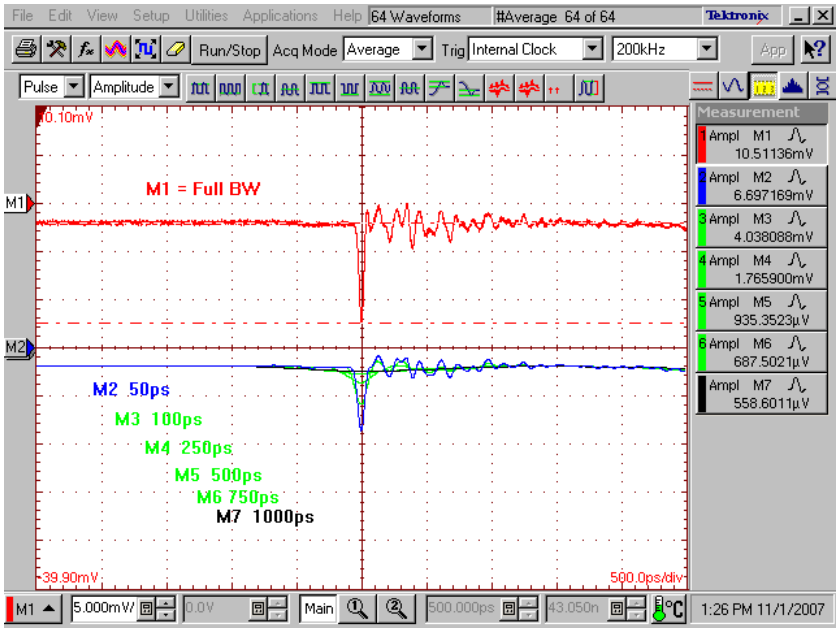
Standard Differential Application – NEXT, "DP5 to DP7"

Source: DPAF_111_112; Victim: DPAF_63_64



Standard Differential Application – FEXT, "DP5 to DP7"

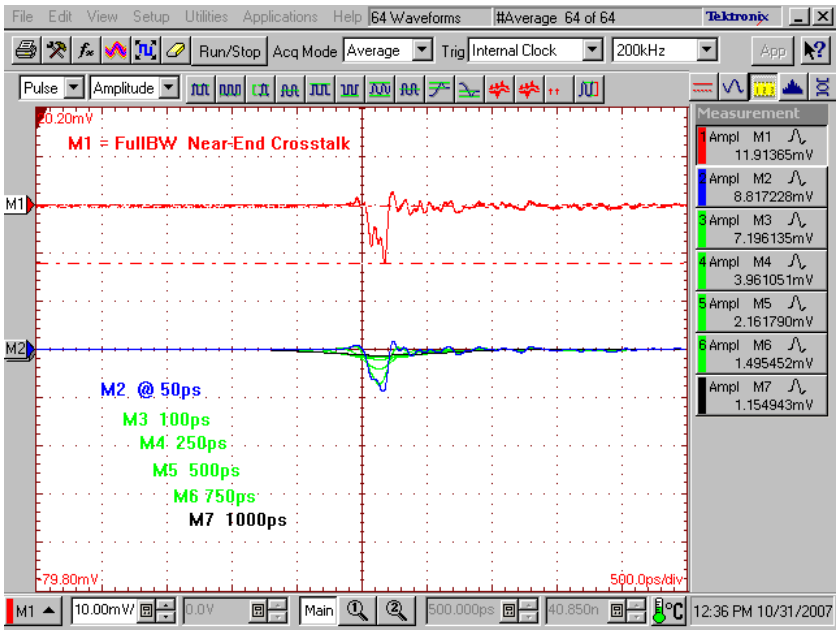
Source: DPAF_111_112; Victim: DPAM_63_64



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

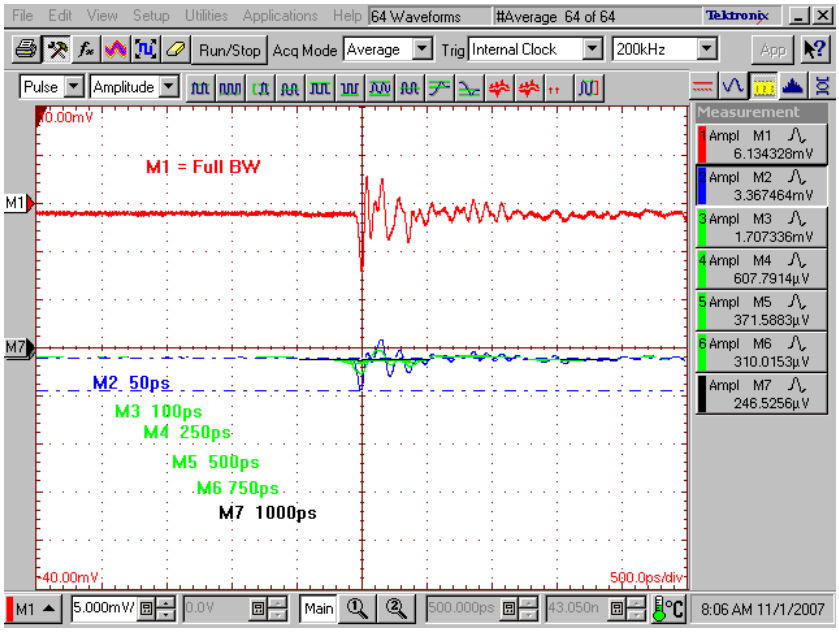
Standard Differential Application – NEXT, "DP6 to DP7"

Source: DPAF_109_110; Victim: DPAF_63_64



Standard Differential Application – FEXT, "DP6 to DP7"

Source: DPAF_109_110; Victim: DPAM_63_64



©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

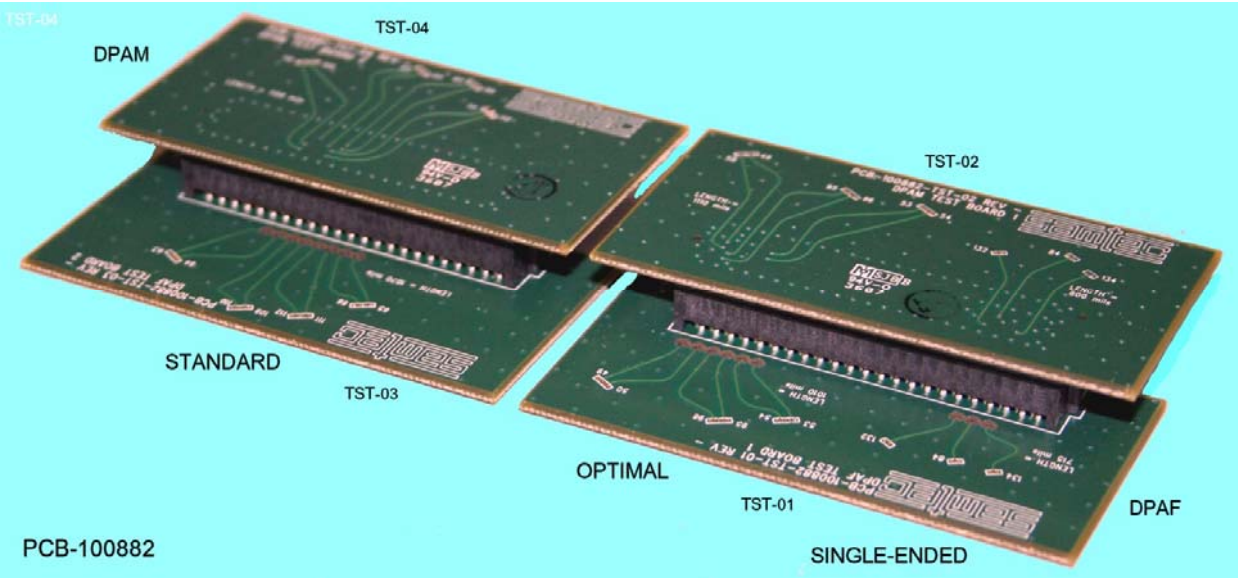
Appendix C – Product and Test System Descriptions

Product Description

DPAF/DPAM Series is an differential signal design bounded by common ground perimeter contacts. Test samples are DPAF-23-03.0-H-3-1-A and DPAM-23-03.0-H-3-1-A The connector style consists of an open pin field array of 3 rows providing 23 signal pairs per row. When mated a 10mm elevation exists between boards.

Test System Description

The test fixtures are composed of a 4-layer FR-4 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec high-speed connector products. The pictured fixture characterizes single ended signaling. Three similar fixtures (not pictured) exist for the various differential signaling options offered for this product.. Configuration conventions and the application details are on the following pages.



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Single-Ended Configuration

Fixture Identity
PCB-100882-TST-01 REV – DPAF TEST BOARD
PCB-100882-TST-02 REV – DPAM TEST BOARD

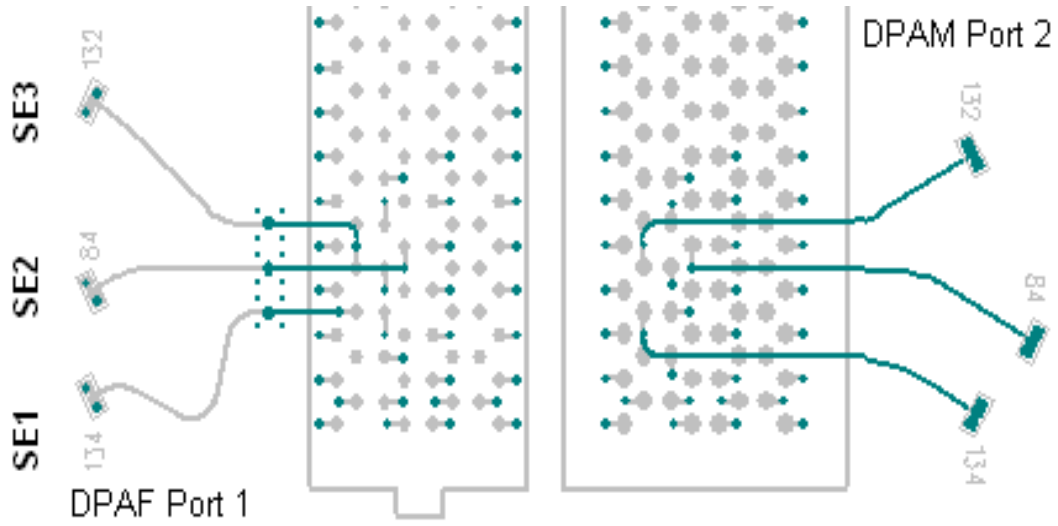
SE THRU Parameters - Insertion Loss, Return Loss, Propagation Delay, Impedance
Configuration: GSG
SE1 DPAF_132, DPAM_132

Crosstalk Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT
Configuration: GAVG, 2:1

Near-End	DPAF_134; SE1	DPAF_132; SE3
Far-End	DPAF_134; SE1	DPAM_132; SE3

Configuration: GAVG, 1:1

Near-End	DPAF_84; SE2	DPAF_132; SE3
Far-End	DPAF_84; SE2	DPAM_132; SE3



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Optimized Differential Configuration

Fixture Identity

PCB-100882-TST-01 REV – DPAF TEST BOARD
PCB-100882-TST-02 REV – DPAM TEST BOARD

Thru Parameters - Insertion Loss, Return Loss, Propagation Delay, Impedance

Optimized Configuration:

port2=DPAF_95_96; port4=DPAM_95_96; path 1
port1=DPAF_49_50; port3=DPAM_49_50; path 2

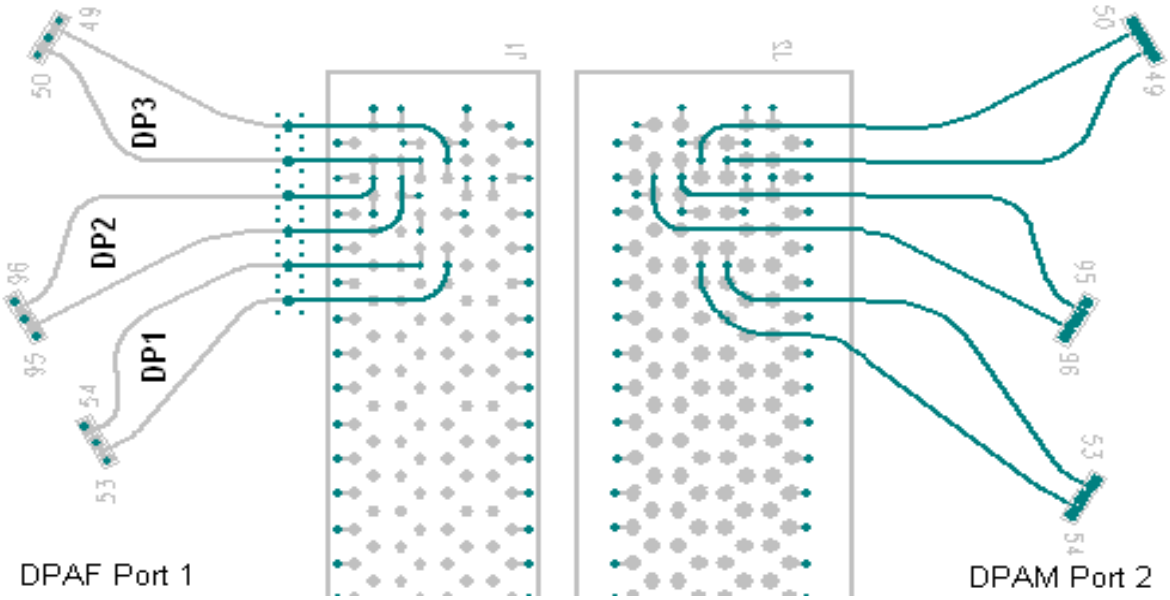
Crosstalk Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT

Optimal Configuration: DP1 to DP3

Near-End DPAF_53_54; DPAF_49_50
Far-End DPAF_53_54; DPAM_49_50

Optimal Configuration: DP2 to DP3

Near-End DPAF_95_96; DPAF_49_50
Far-End DPAF_95_96; DPAM_49_50



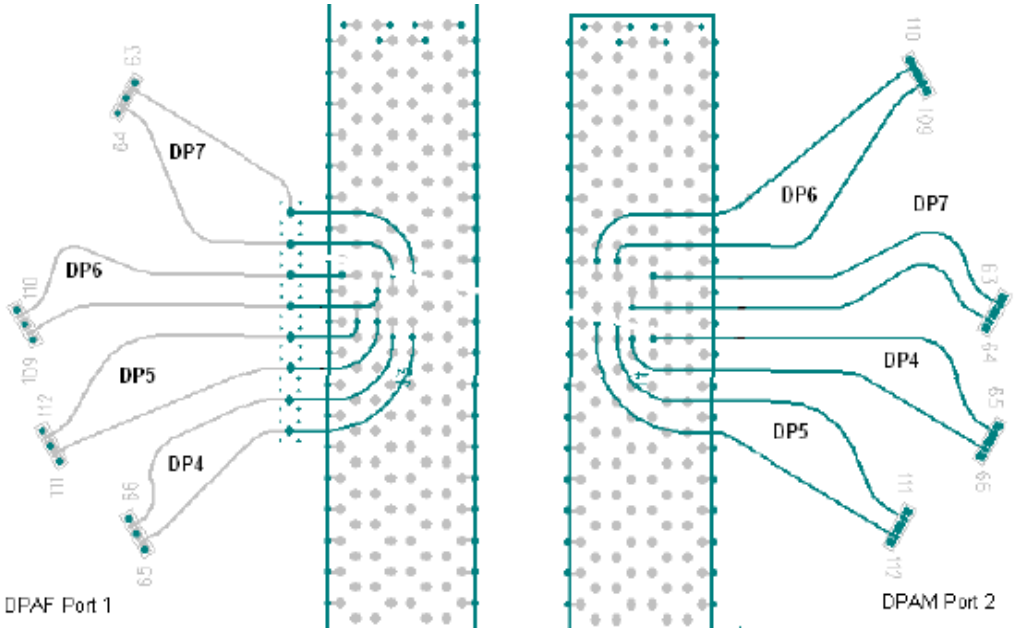
Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Standard Differential Configuration

Fixture Identity
PCB-100688-TST-03 REV – DPAF TEST BOARD 2
PCB-100688-TST-04 REV – DPAM TEST BOARD 2

Thru Parameters - Insertion Loss, Return Loss, Propagation Delay, Impedance
Standard Configuration:
port2=DPAF_109_110; port4=DPAM_109_110; path 1
port1=DPAF_63_64; port3=DPAM_63_64; path 2

Crosstalk Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT
Standard Configuration: DP4 to DP7
Near-End DPAF 65_66; DPAF 63_64
Far-End DPAF 65_66; DPAM 63_64
Standard Configuration: DP5 to DP7
Near-End DPAF 111_112; DPAF 63_64
Far-End DPAF 111_112; DPAM 63_64
Standard Configuration: DP6 to DP7
Near-End DPAF 109_110; DPAF 63_64
Far-End DPAF 109_110; DPAM 63_64



Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

DPAX Calibration Board

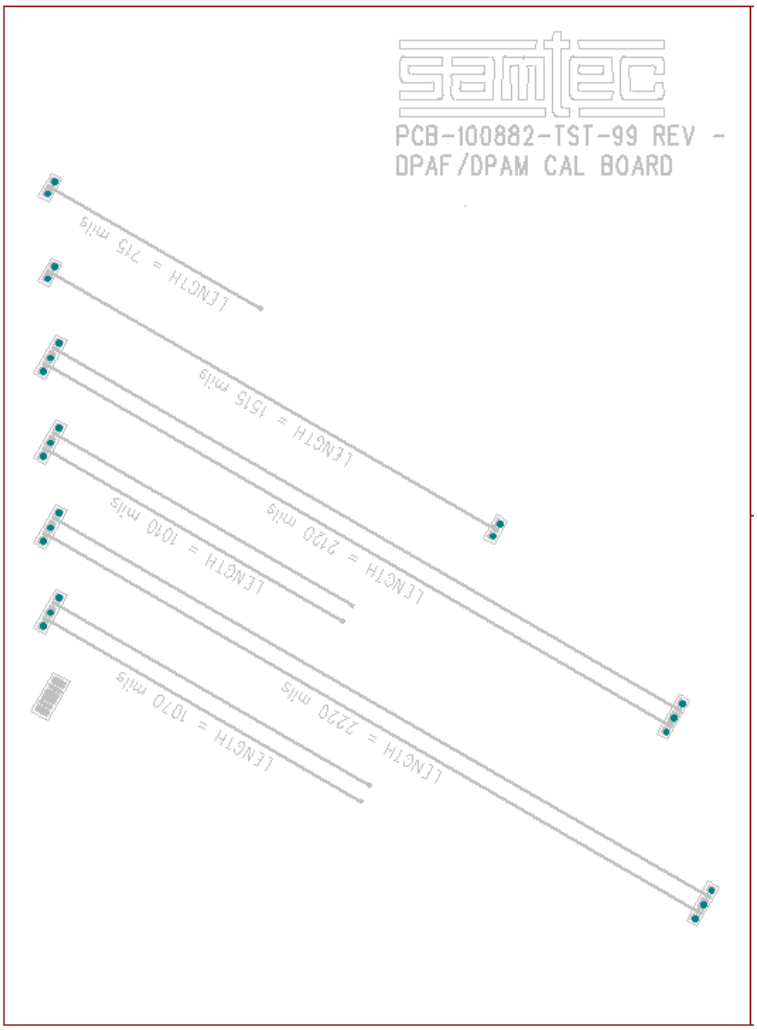
Reference Lengths

Single-Ended, 1515 mils

Optimal Differential, 2120 mils

Standard Differential, 2220 mils

TDA Step Waveform Transmission/Reflection Standard

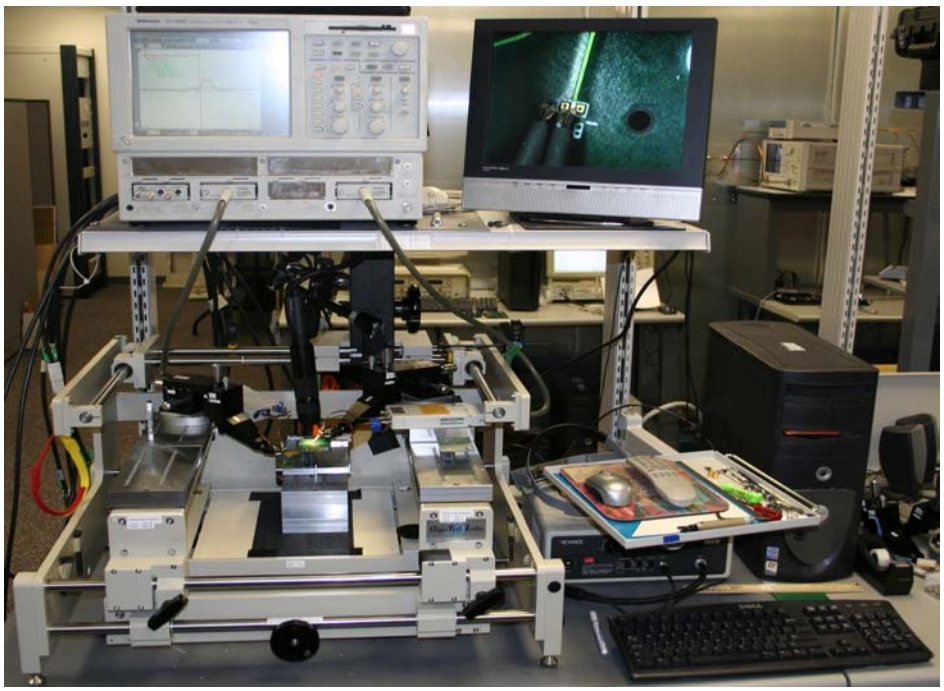


Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Appendix D – Test and Measurement Setup

The test instrument is the Tektronix CSA8000 Communication Signal Analyzer Mainframe. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. Time domain results are generated using the TDR/Sampling Head capability. S-parameter data is generated from a TDR based software tool called I-Connect Probing is accomplished using a video microscopy system, microprobe positioners, and 40GHz capable probes. The 450 micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a ≥18 dB return loss, and an isolation of 38 dB providing high-bandwidth and low parasitic measurement results. Combined, the above technology provides a stable measurement environment along with the electrical accuracies for obtaining precise calibrations and signal launch capabilities

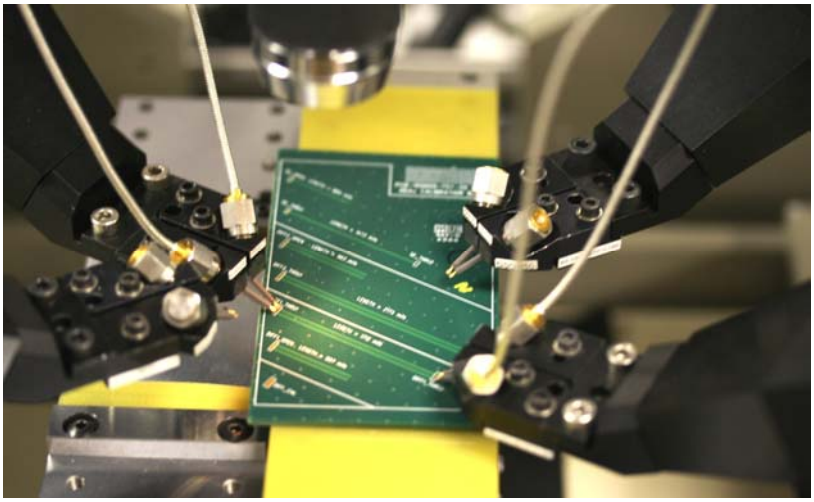
CSA8000/TDA IConnect Measurements Capability



©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Four Position Dual 40 GHz Microprobe Setup



Test Instruments

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
4	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Tektronix 80E03 Dual Channel 20 GHz Sampling Module

Measurement Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
4	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

QTY	Description
4	Pasternack Enterprises 2.9mm Semi-Rigid (.086) 9” Cable Assemblies
4	Tektronix 1 Meter Module Extenders

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Record domain parameters utilizing the same test points simultaneously.

Sample Preparation
Determine signal launch and monitoring test points by referencing the layout maps of interest

Single-Ended Characterization:	SE
Optimal Differential	OD
Standard Differential	SD
Calibration Board	DPAX

Terminate all non-active signal lines immediately adjacent to the designated active or quiet signal lines under test.

Frequency (S-Parameter) Domain Procedures
Frequency data extraction is a two-step process. The first step is to create two time domain waveforms that relate to as-parameter frequency response. The second step post-processes these time-based waveforms into the s-parameter of interest using the TDA Systems IConnect software tool. TDA Systems refers to these time related conversion waveforms as the *Step* and *DUT* waveform references. This section establishes the procedures for defining the *Step* and *DUT* reference waveforms.

CSA8000 Setup
Listed below is the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. Rules for vertical scale settings are (1) that all time domain waveforms recorded for post-processing are observable on the instruments screen and (2) differential math function amplitudes not appear clipped by the TDR channel offset settings. The averaging function serves to smooth any noise appearing on a processed waveform.

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Frequency bandwidth and step frequency boundaries are resolved by adjusting CSA8000 instruments window length and record length settings. Longer window lengths and maximum record lengths increase bandwidth and step frequency resolution. The single channel pulsed source processes s-parameters in single-ended format. A dual channel differential pulsed source processes s-parameters in differential format. The nested table below offers the functional settings of the CSA8000 used in gathering the time domain waveforms for this test.

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss (TDA conversion)

Step Waveform - determine TD waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Complete signal paths by inserting a negligible length of transmission standard between the system test probes. Calibration or waveform referencing utilizes three pads for each probe touchdown (eg; se thru = six pads or diff thru = twelve pads). Reference DPAX, calibration board and use 1mm (0.390") length calibration reflection/transmission standard for TDA step waveform characterization.

DUT Waveform - determine TD waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the reflection/transmission standard and record the measurement. The DPAF/DPAM characterization examines one single-ended and four differential insertion loss responses.

Return Loss (TDA conversion)

Step Waveform – determine TD waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. Calibration or waveform referencing utilizes 3 pads for each probe touchdown (ie; se reflect = 3 pads or diff reflect = 6 pads). Reference DPAX, calibration board and use 1mm (0.390") length calibration reflection/transmission standard for TDA step waveform characterization.

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

DUT Waveform – determine waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the reflection/transmission standard and record the measurement. In this condition cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. The DPAF/DPAM characterization examines one single-ended and four differential return loss responses.

Near-End Crosstalk (TDA conversion)

Step Waveform – Use Return Loss step waveform.

DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent near-end signal line. DPAF/DPAM examines two single-ended and five differential NEXT configurations. Reference the single-ended layout SE for an appropriate near-end crosstalk configuration. Reference the optimized differential OD and standard differential SD for the appropriate near-end crosstalk configuration.

Far-End Crosstalk (TDA conversion)

Step Waveform - Use Insertion Loss step waveform.

DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent far-end signal line. DPAF/DPAM examines two single-ended and five differential FEXT configurations. Reference the single-ended layout SE for an appropriate far-end crosstalk configuration. Reference the optimized differential OD and standard differential SD for the appropriate far-end crosstalk configuration.

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Time Domain Procedures

Measurements involving digital type pulses utilize the Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. Impedance utilizes TDR exclusively. Propagation delay and crosstalk characterization measurements utilize TDT. The Tektronix 80E04 TDR/ Sampling Head provide the signaling type and sampling capabilities necessary in accurately characterizing the SUT.

Impedance (TD)

Energize with a TDR pulse the signal line(s) of interest. Terminate the far-end of the energized signal line with either a quality termination or quality high-speed cables and adapters matching the test systems characteristic impedance (e.g.; 50Ω or 100Ω). The DPAF/DPAM characterization examines one single-ended and four differential impedance configurations. Use the single-ended characterization SE to determine the signal path for the SE impedance profile. Use OD or SD differential characterization layouts to determine the differential impedance profile of interest.

Propagation Delay (TD)

This test reports differential or single ended signal delay as the measured difference of propagation between a combined electrical length of the input/output signal pads and traces (30 ± 5 ps edge rate) and the device under test (DUT) plus a referenced electrical length of the signal pads and signal traces ($PD^{pads/traces}$- $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$). $PD^{pads/traces}$ is the nomenclature representing the electrical length of PCB signal pads & traces equal to physical lengths of PCB pads & traces entering and leaving the device under test (DUT). The PD^{DUT} + $PD^{pads/traces}$ variable is the mated DUT fixture. Measure and record the 50% amplitude of the $PD^{pads/traces}$ waveform and the 50% amplitude of $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$ waveform response. The distance in time between the rising edges is the propagation delay of the device under test (DUT). To find the appropriate $PD^{pads/traces}$ reference line reference the DPAX calibration board. To locate the appropriate PD^{DUT} configuration reference characterization layout SE, OD, or SD.

Near-End Crosstalk (TD)

Energize a pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the near-end for a magnitude of coupled energy. Terminate adjacent signal lines not undergoing testing into the test systems characteristic impedance. DPAF/DPAM examines two single-ended and five differential time domain NEXT responses. Reference the single-ended layout SE for an appropriate near-end crosstalk configuration. Reference the optimized differential OD and standard differential SD for the appropriate near-end crosstalk configuration.

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Far-End Crosstalk (TD)

Energize a pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the far-end for a magnitude of coupled energy. Terminate adjacent signal lines not undergoing testing into the test systems characteristic impedance. DPAF/DPAM examines two single-ended and five differential time domain FEXT responses. Reference the single-ended layout SE for the appropriate far-end crosstalk configuration. Reference the optimized differential OD and standard differential SD for the appropriate far-end crosstalk configuration.

©Samtec, Inc. 2005
All Rights Reserved

Series: DPAM/DPAF Array, 2.16mm x 2.54mm Differential Pair Interconnect
Description: Perimeter Contacts Common to PCB Ground, 10mm Stack Height

Appendix F – Glossary of Terms

TD – Time Domain
FD – Frequency domain
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
EC6 – Edge Card with a .635mm signal pad pitch
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
LEC6 – Signal Launch Edge Card with a .635 mm signal pad pitch
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
BC – Best Case crosstalk configuration
Z – Impedance (expressed in ohms)
OV – Optimal Vertical
OH – Optimal Horizontal
HDV – High Density Vertical
PPO – Pin Population Option
OD – Optimal Differential
SD – Standard Differential

©Samtec, Inc. 2005
All Rights Reserved