# High Speed Characterization Report

## ECUE-12-050-C1-FF-01

**Mated with**:
**UEC5-019-01-L-D-RA-A**

## Description:

## FireFly™ Micro Flyover System,
## 38 AWG Coax Cable, 50cm Cable Length

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## Cable Assembly Overview

Samtec's FireFly™ Micro Flyover System is a complete interconnect system that uses either micro footprint optical or copper interconnects. The FireFly™ system enables chip-to-chip, board-to-board, and system-to-system connectivity at rates up to 28Gbps. FireFly™ is based on a high performance interconnect system which allows the utilization of low-cost copper cables or high performance active optical engines. Firefly uses a 2 stage connector system. The UEC5 caries the high speed digital signals while the UCC8 caries the DC/low frequency status lines. The data in this report is applicable only to an 18 inch copper Firefly™ system.

The performance of the ECUE to UCC8 is not considered in this report. The UCC8 is intended for low-speed signals and power only.

## Cable Assembly Speed Rating

The cable assembly Speed Rating is based on the –7 dB insertion loss point of the mated cable assembly. The –7 dB point can be used to estimate usable system bandwidth in a typical two-level signaling environment.

To calculate the Speed Rating, the measured –7 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for any loss from the test board traces. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps). The following table summarizes the Cable Assembly Speed Ratings for the ECUE cable assemblies tested.

| Assembly | -7 dB Frequency | Speed Rating |
|---|---|---|
| ECUE-12-050-C1-FF-01 | 5.5 GHz | 11.0 Gbps |

**Table 1: Cable Assembly Speed Ratings**

The Samtec Speed Rating is best considered a figure of merit for comparing relative performance between cable assemblies. The Speed Rating becomes less meaningful in systems using multi-level signaling or where crosstalk or impedance mismatch are more critical parameters. Modern high-speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The –7 dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

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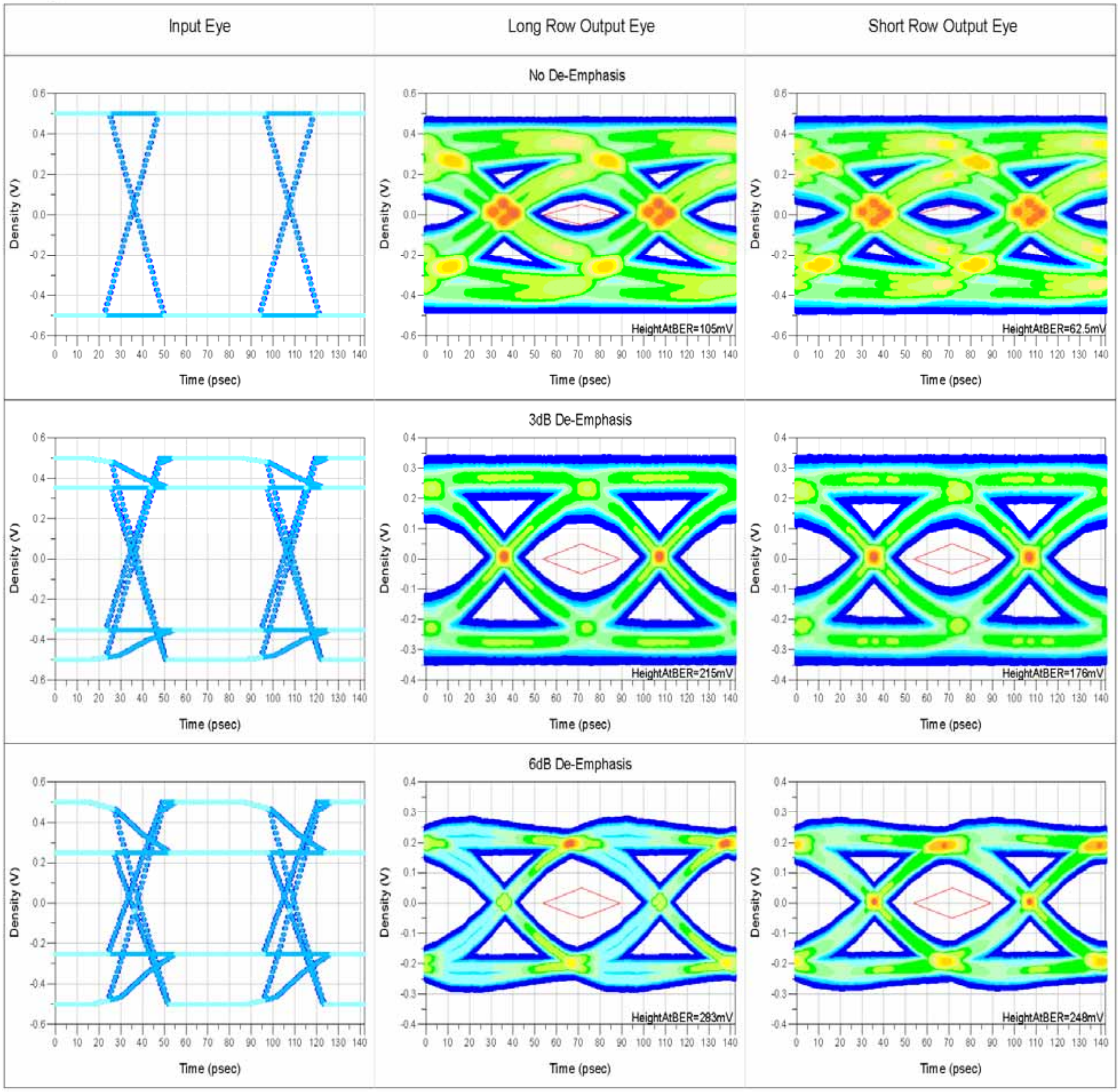
## Eye Pattern Summary

***14Gbps***



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## Frequency Domain Data Summary

| Table 2 - Differential Cable assembly System Performance | | |
|---|---|---|
| **Test Parameter** | **Configuration** | **Threshold Limits** |
| **Insertion Loss** | Long Row | -7dB @ 5.938 GHz |
| | Short Row | -7dB @ 5.188 GHz |
| **Return Loss** | Long Row | >10dB to 10.863 GHz |
| | Short Row | >10dB to 4.525 GHz |
| **Near-End Crosstalk** | In Row-Long Row | < -20dB to 20 GHz |
| | In Row-Short Row | < -20dB to 20 GHz |
| | Xrow | < -20dB to 20 GHz |
| | Diagonal | < -20dB to 20 GHz |
| **Far-End Crosstalk** | In Row-Long Row | < -20dB to 20 GHz |
| | In Row-Short Row | < -20dB to 20 GHz |
| | Xrow | < -20dB to 20 GHz |
| | Diagonal | < -20dB to 20 GHz |

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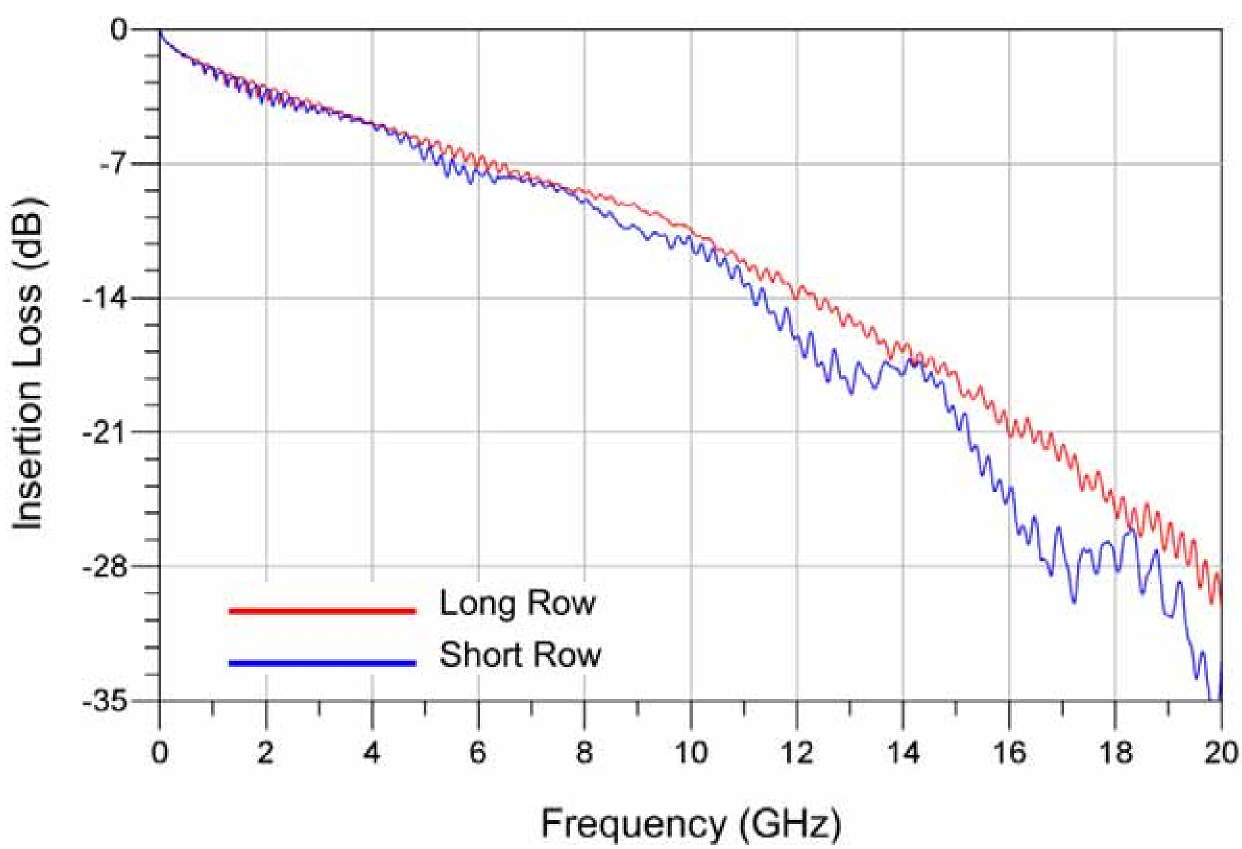
## Bandwidth Chart – Differential Insertion Loss



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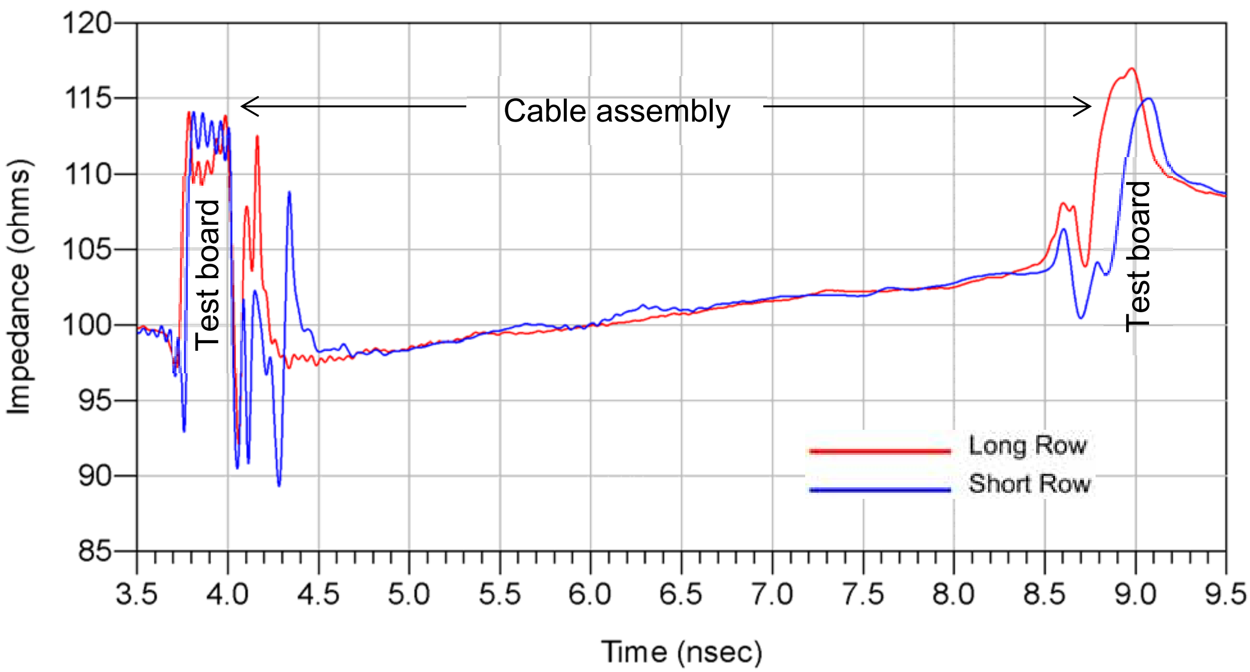
## Time Domain Data Summary




| Table 3 - Propagation Delay (Cable Assembly) | |
|---|---|
| **Long Row** | 2.45ns |
| **Short Row** | 2.44ns |
| **Long/Short Delay Skew** | 12ps |

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## Characterization Details

This report presents data that characterizes the signal integrity response of a cable assembly in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the mating connectors, cable assembly, and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the cable assembly's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

### Differential and Single-Ended Data

Most Samtec cable assemblies can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for "GSSG" differential drive configuration only.

### Cable assembly Signal to Ground Ratio

Samtec cable assemblies are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some cable assemblies, a ground plane or blade, or an outer shield, is used as the signal return, while in others, cable assembly pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a cable assembly. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

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For this cable assembly, the following array configurations are evaluated:

Differential Impedance**:**
- Long Row (upper terminals, furthest from test fixture)
- Short Row (bottom terminals, closest to test fixture)

Differential Crosstalk**:**
- In Row: Long Row (adjacent terminals in the long row)
- In Row: Short Row (adjacent terminals in the short row)
- Cross Row: “Xrow”: (from one row of terminals to the other row)
- Diagonal Cross Row: “Diagonal”: (diagonally opposed terminals from one row to the other row)

See Appendix D – Product and Test System Descriptions for details

Only one differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

<u>Signal Edge Speed (Rise Time)</u>
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the cable assembly than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

Unless otherwise stated, measured rise times were at 10%-90% signal levels.

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## Eye Diagram Data

Eye patterns are a time domain characterization of system level performance. Eye patterns are generated by sending continuous streams of data from a transmitter to a receiver, and overlaying the received signals upon one another. Over time, the received data builds to resemble an eye. Negative SI effects in the transmission path can cause the signal to distort, which over time, will cause the eye to "close". Specifications, such as an eyemask template, can be placed on the amount of open area required in the eye to ensure a functional system.

An eyemask template is a representation of the receiver's sensitivity and is often used as a metric of performance. While there are lot-to-lot and vendor-to-vendor variations in receiver sensitivity, some general guidelines can be developed. After reviewing several major industry standards (PCIe, Gigabit Ethernet) we find similar eyemask requirements and we will use these as the basis for a generic template in this report. For this report we will assume a receiver amplitude sensitivity of 50 mVpp and a jitter margin of 0.5 UI. This results in a diamond shape eyemask template that is 50 mV high and 0.5 UI wide.

Please contact our Signal Integrity Group at sig@samtec.com for more information.

## Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the cable assembly system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, Near-End and Far-End Crosstalk, and Mode Conversion. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

## Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, and signal propagation time in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Agilent ADS to obtain the time domain response. Time Domain procedure is provided in Appendix F of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

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In this report, propagation delay is defined as the signal propagation time through the cable assembly, mating connectors, and connector footprint. It also includes 40 mils of PCB trace on each connector side. Delay is measured at 30 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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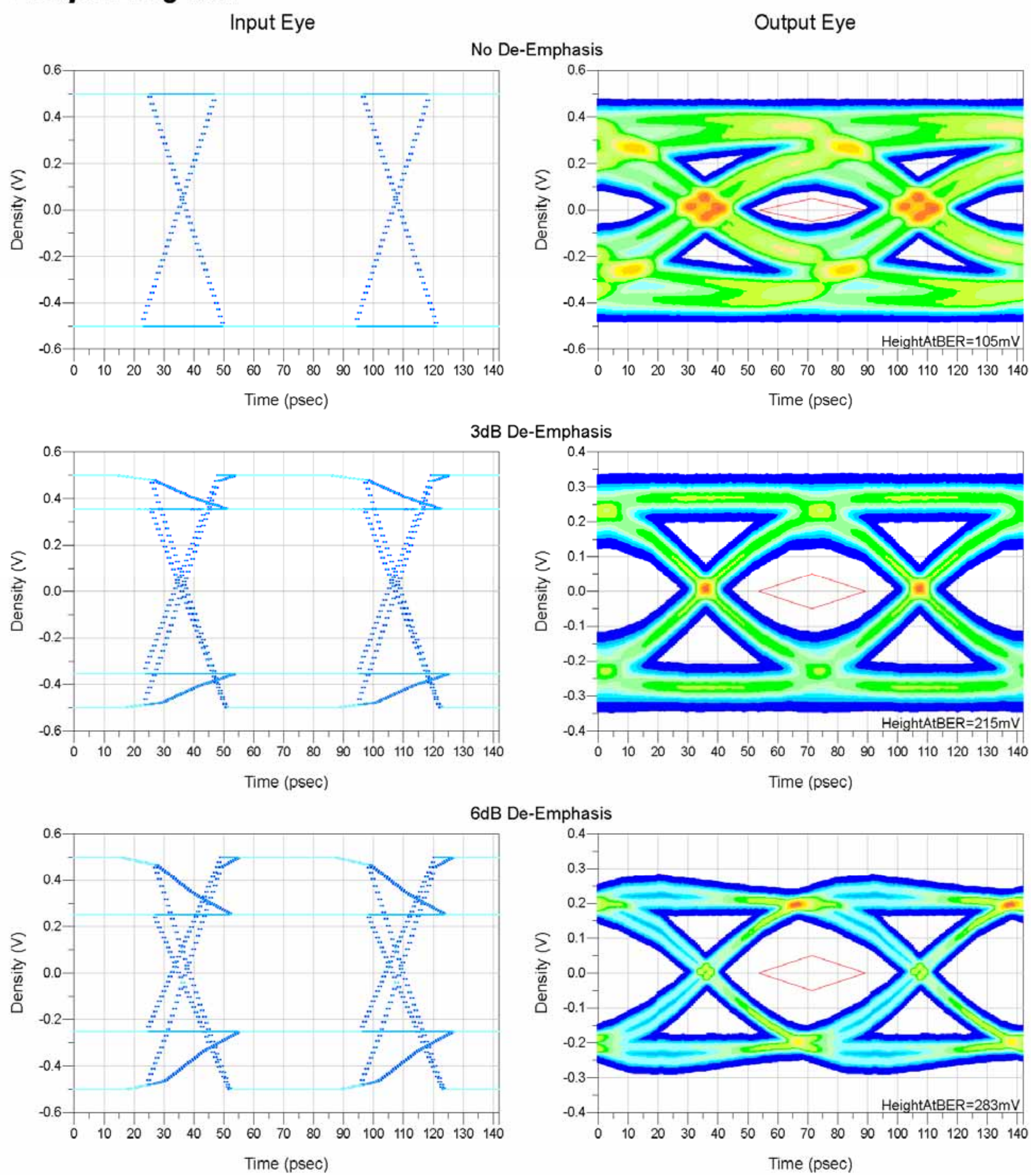
## Appendix A – Eye Diagrams

***14Gbps: Long Row***

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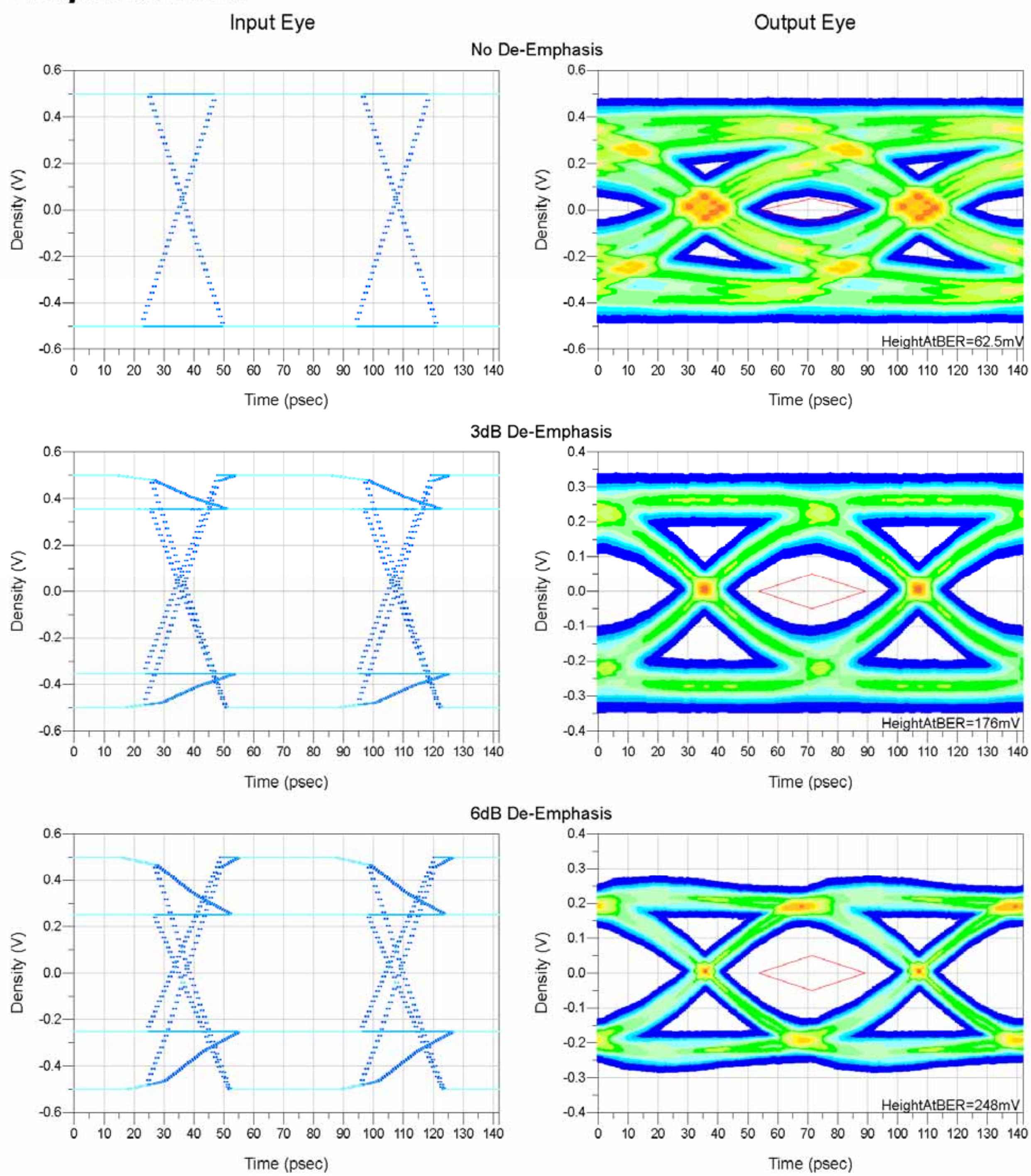
### *14Gbps: Short Row*



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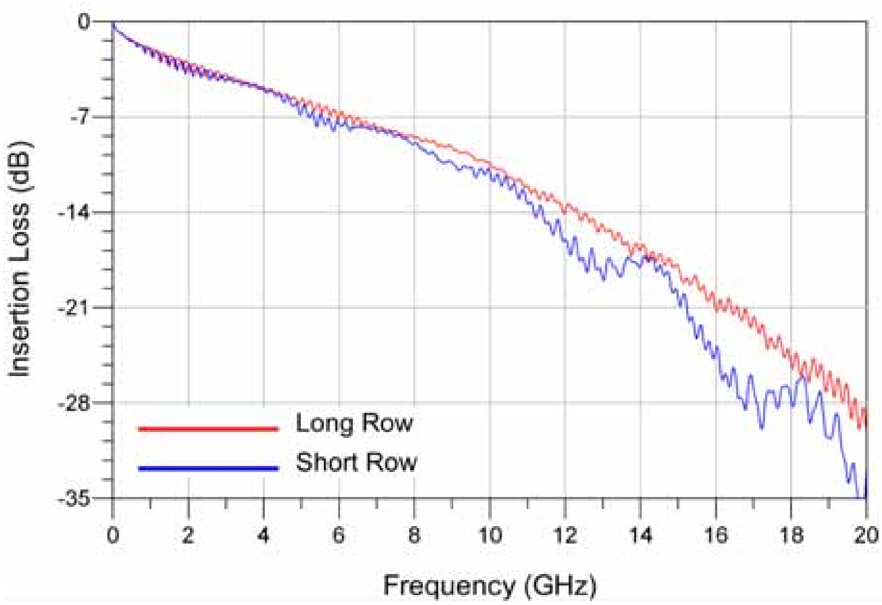
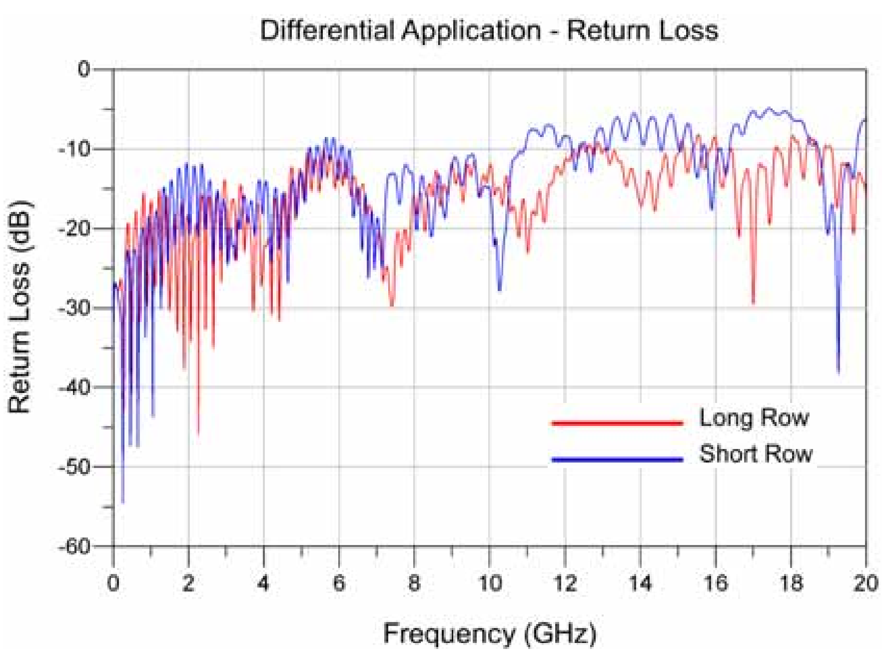
# Appendix B – Frequency Domain Response Graphs

## Differential Application – Insertion Loss




## Differential Application – Return Loss



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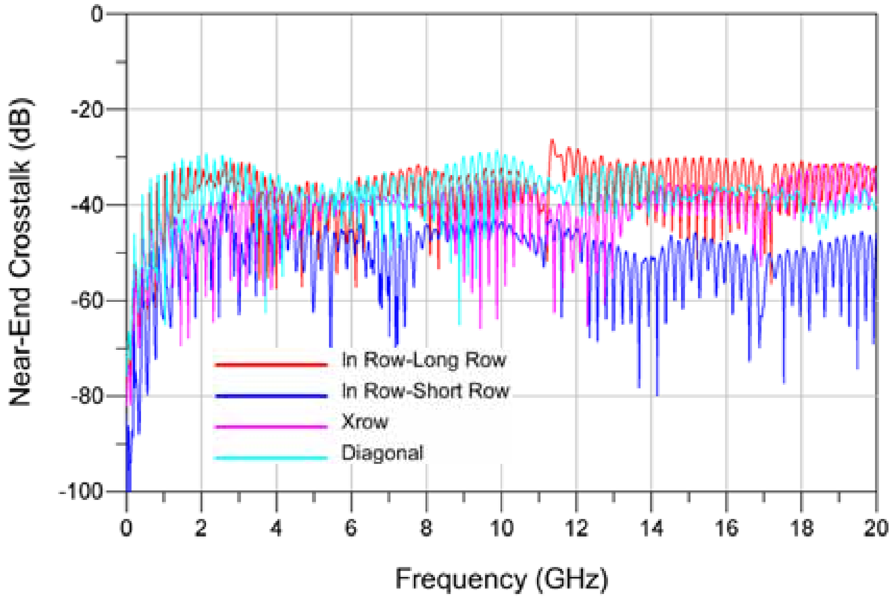
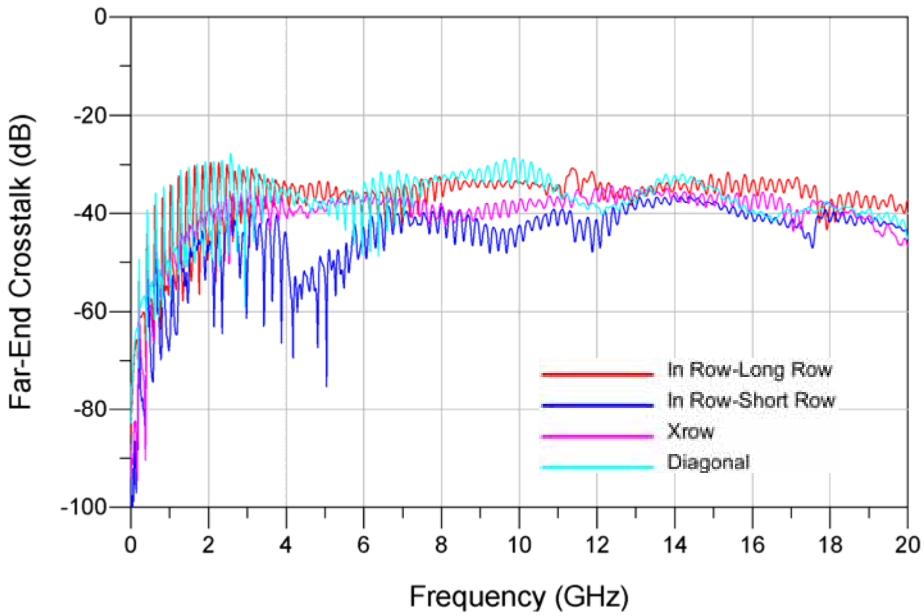
## Differential Application – NEXT Configurations




## Differential Application – FEXT Configurations



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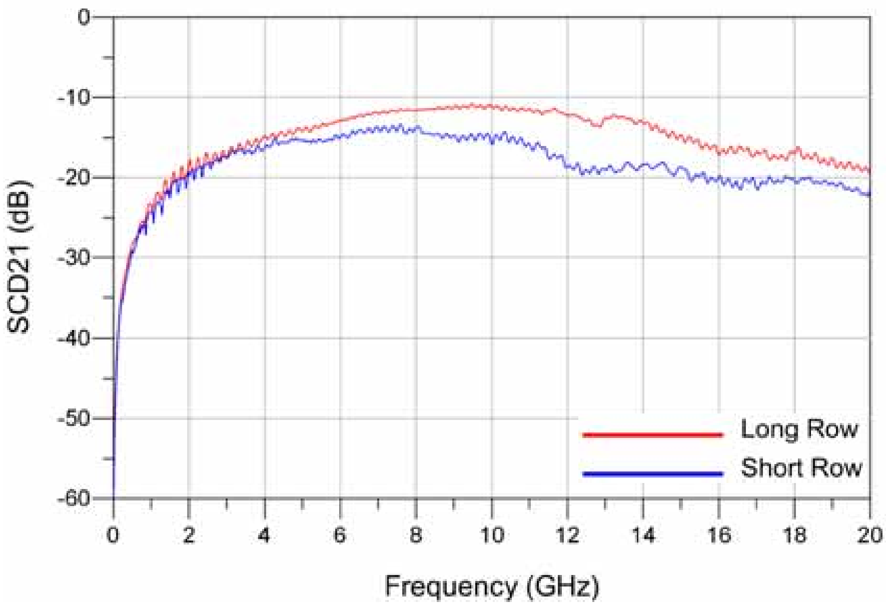
## Differential Application – Differential to Common Mode Conversion



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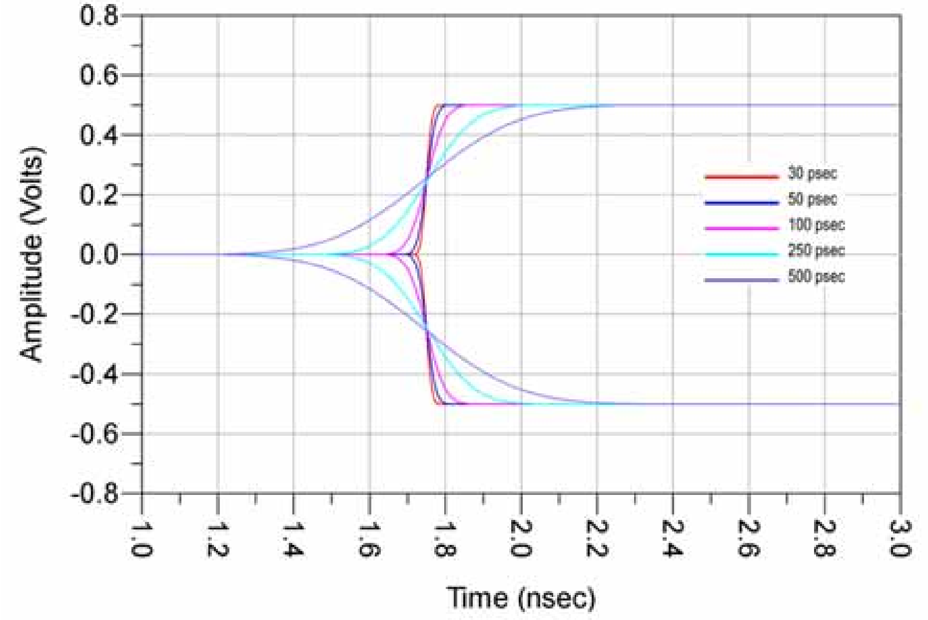
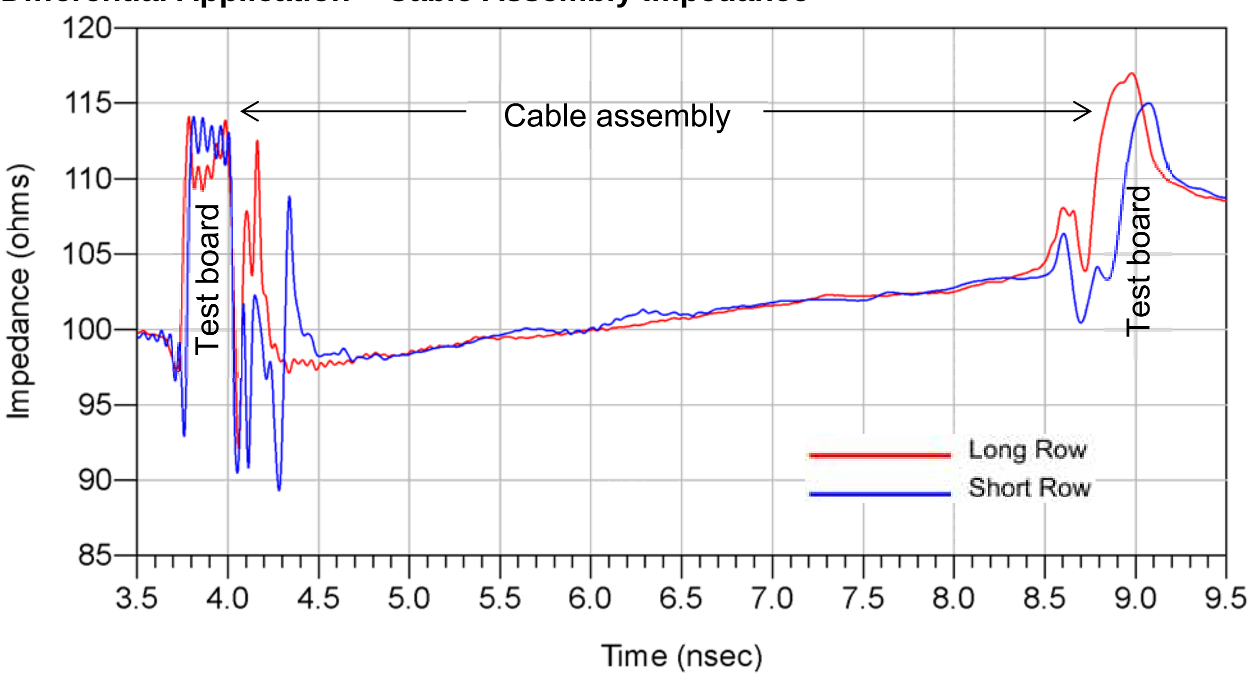
# Appendix C – Time Domain Response Graphs

## Differential Application – Input Pulse




## Differential Application – Cable Assembly Impedance



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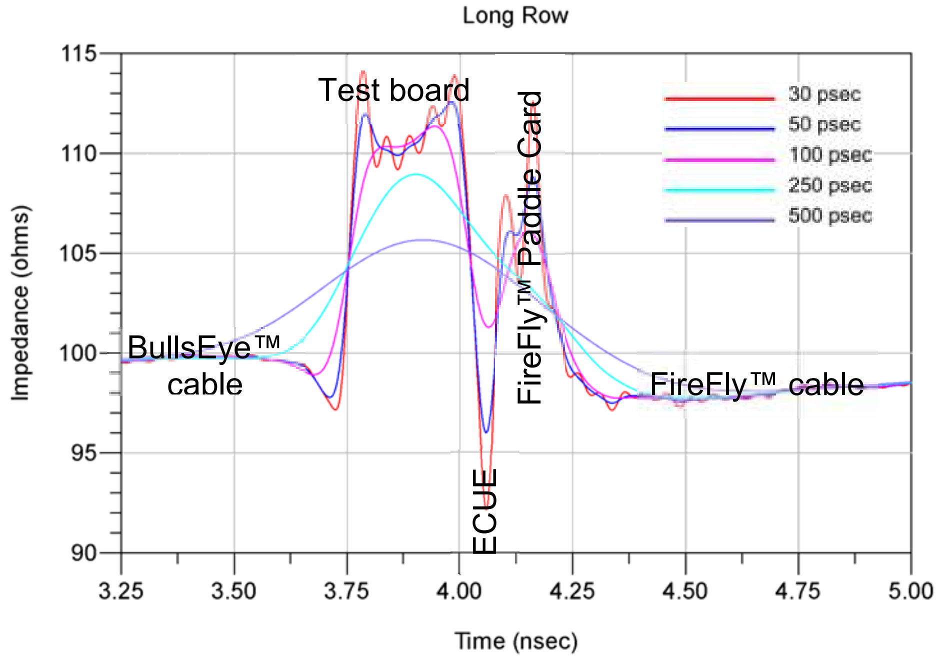
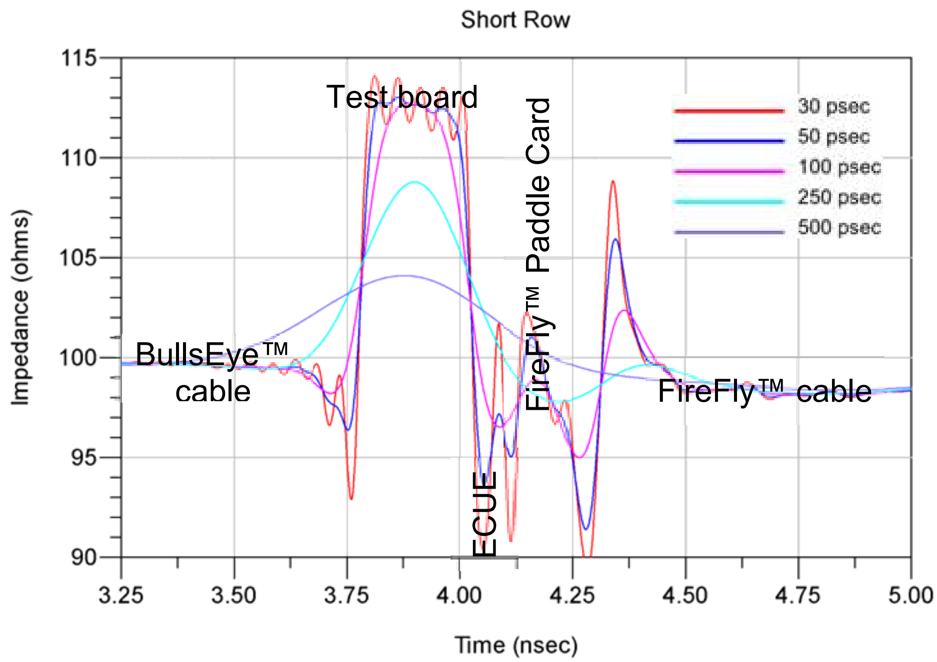
## Differential Application – Cable assembly Impedance



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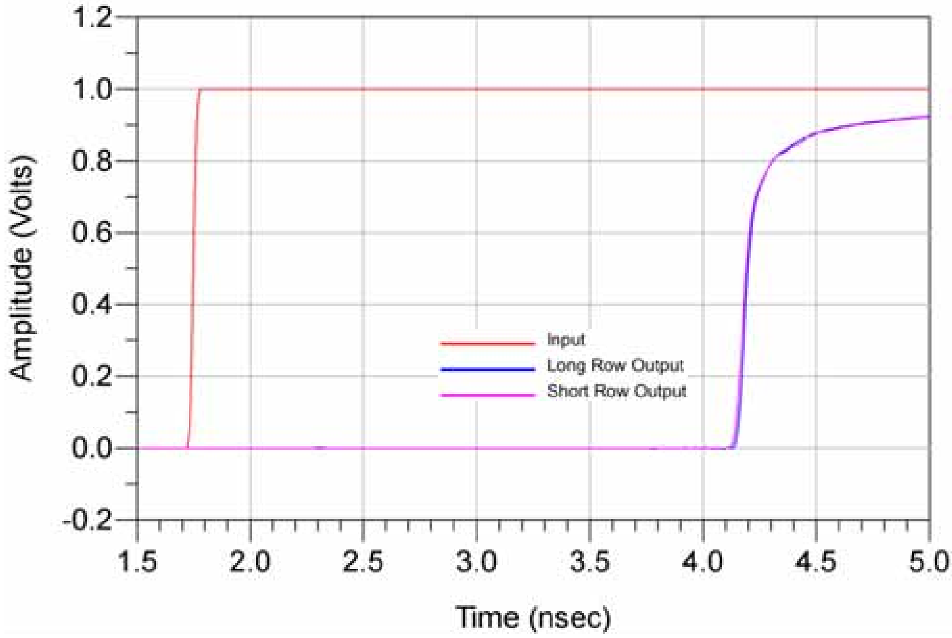
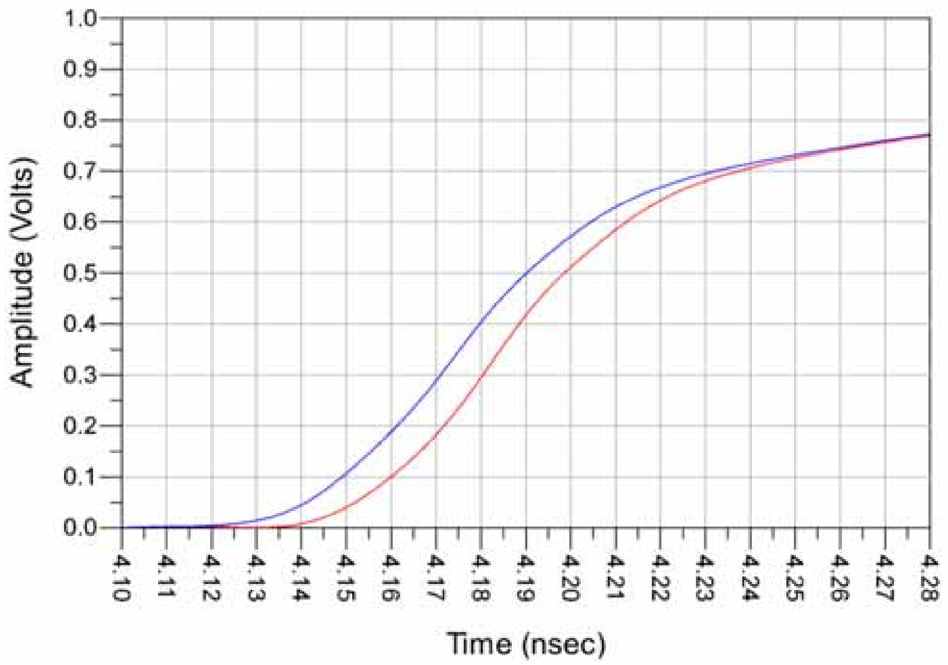
## Differential Application – Propagation Delay




## Differential Application – Row to Row Skew



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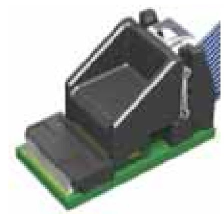
## Appendix D – Product and Test System Descriptions

### Product Description

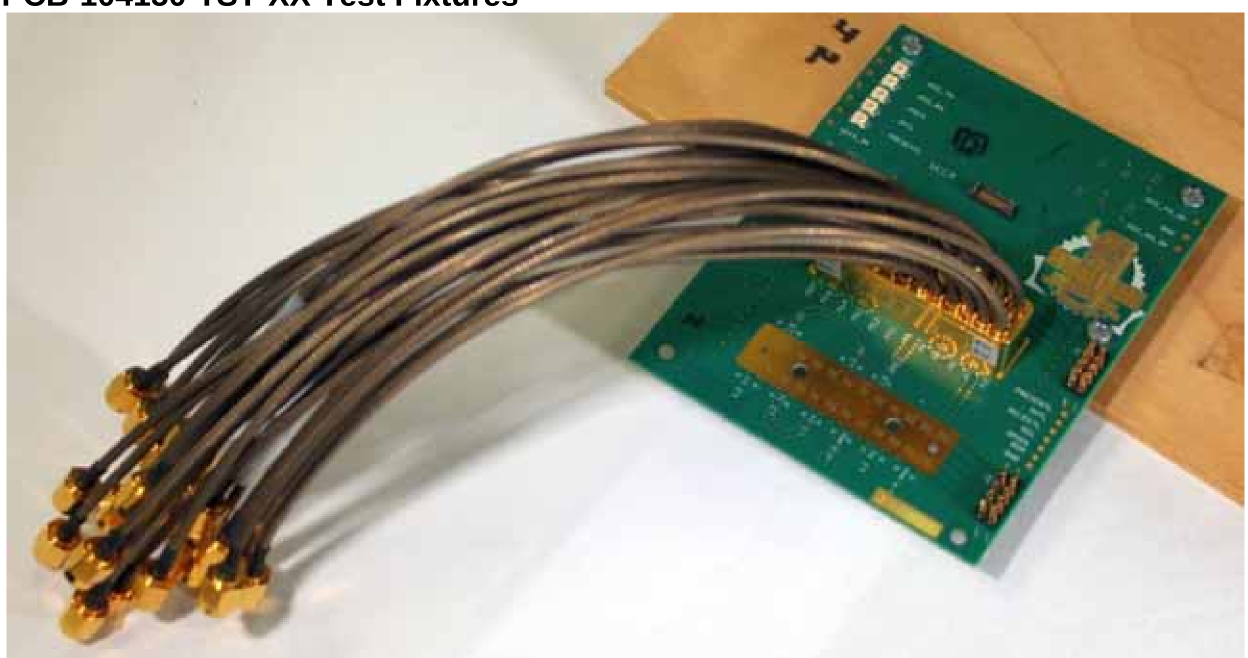
Product test samples are copper FireFly™ cable assemblies. The part number is ECUE-12-050-C1-FF-01 and it mates to UEC5-019-01-L-D-RA-A. The cable assembly has two rows of 19 contacts evenly spaced on a 0.5 mm (0.0197”) pitch, in a GSSG configuration. A representative image of the mated test article mounted to SI test boards is shown at right.



### Test System Description

The test fixtures are composed of six-layer FR-406 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed cable assembly products. A PCB mount BullsEye™ connector is used to interface the VNA test cables to the test fixtures. BullsEye™ launch optimization is attained using full wave simulation tools to minimize reflections. There is one test fixture specific to the FireFly™ series cable assembly set. The Auto Fixture Removal (AFR) calibration structures designed specifically for the FireFly™ series are on the same test fixture. Displayed on the following pages is information for the BullsEye™/AFR calibration structure and directives for mating FireFly™ fixtures.

### PCB-104150-TST-XX Test Fixtures



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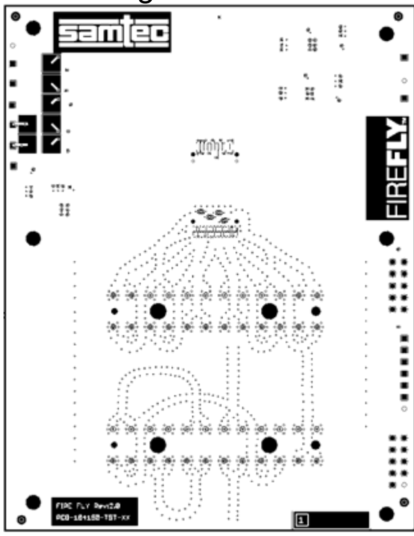
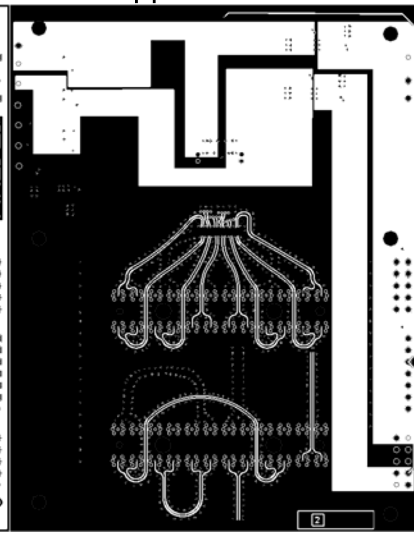
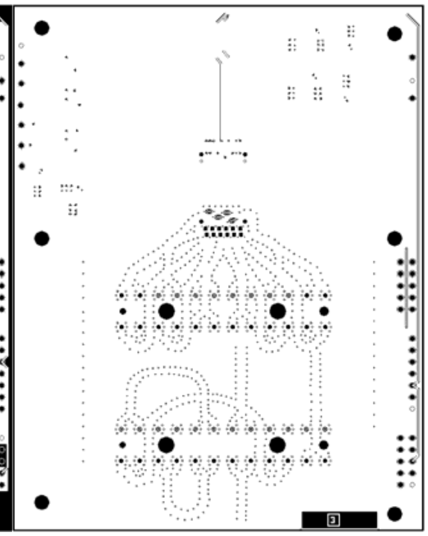
PCB design artwork shown below. Copper is shown in white.



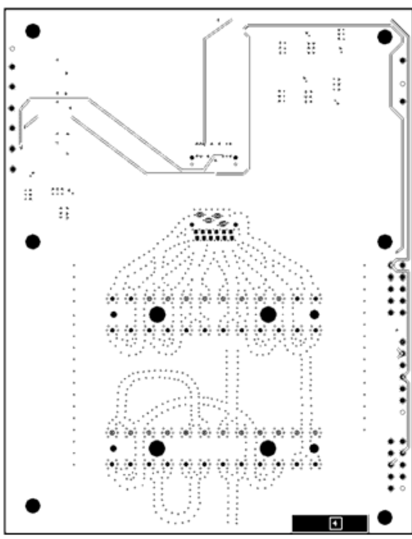

Layer 1



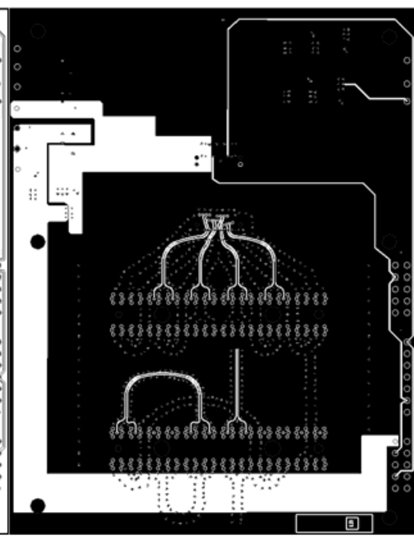
Layer 2



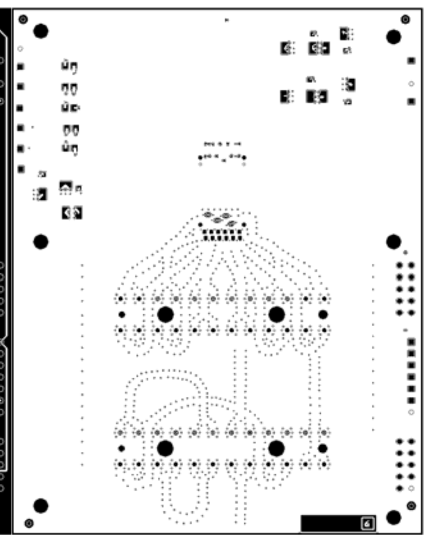
Layer 3



Layer 4



Layer 5



Layer 6

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## PCB Fixtures

The test fixtures used are as follows:

### INSERTION LOSS: Long Row

| | NEAR END | | FAR END | | |
|---|---|---|---|---|---|
| | Long | Short | Short | Long | |
| | A17 | B17 | B3 | A3 | |
| | A18 | B18 | B2 | A2 | |
| | A14 | B15 | B5 | A6 | |
| | A15 | B14 | B6 | A5 | |
| | A12 | B12 | B8 | A8 | |
| | A11 | B11 | B9 | A9 | |
| 3 | **A9** | B9 | B11 | **A11** | 4 |
| 1 | **A8** | B8 | B12 | **A12** | 2 |
| | A5 | B6 | B14 | A15 | |
| | A6 | B5 | B15 | A14 | |
| | A2 | B2 | B18 | A18 | |
| | A3 | B3 | B17 | A17 | |

### INSERTION LOSS: Short Row

| NEAR END | | | | FAR END | |
|---|---|---|---|---|---|
| Long | Short | | | Short | Long |
| A17 | B17 | | | B3 | A3 |
| A18 | B18 | | | B2 | A2 |
| A14 | B15 | | | B5 | A6 |
| A15 | B14 | | | B6 | A5 |
| A12 | B12 | | | B8 | A8 |
| A11 | B11 | | | B9 | A9 |
| A9 | **B9** | 3 | 4 | **B11** | A11 |
| A8 | **B8** | 1 | 2 | **B12** | A12 |
| A5 | B6 | | | B14 | A15 |
| A6 | B5 | | | B15 | A14 |
| A2 | B2 | | | B18 | A18 |
| A3 | B3 | | | B17 | A17 |

All adjacent unused pairs terminated

### NEXT: IN ROW - Long Row

| | NEAR END | | FAR END | |
|---|---|---|---|---|
| | Long | Short | Short | Long |
| | A17 | B17 | B3 | A3 |
| | A18 | B18 | B2 | A2 |
| | A14 | B15 | B5 | A6 |
| | A15 | B14 | B6 | A5 |
| 4 | **A12** | B12 | B8 | A8 |
| 2 | **A11** | B11 | B9 | A9 |
| 3 | **A9** | B9 | B11 | A11 |
| 1 | **A8** | B8 | B12 | A12 |
| | A5 | B6 | B14 | A15 |
| | A6 | B5 | B15 | A14 |
| | A2 | B2 | B18 | A18 |
| | A3 | B3 | B17 | A17 |

### NEXT: IN ROW - Short Row

| NEAR END | | | FAR END | |
|---|---|---|---|---|
| Long | Short | | Short | Long |
| A17 | B17 | | B3 | A3 |
| A18 | B18 | | B2 | A2 |
| A14 | B15 | | B5 | A6 |
| A15 | B14 | | B6 | A5 |
| A12 | **B12** | 4 | B8 | A8 |
| A11 | **B11** | 2 | B9 | A9 |
| A9 | **B9** | 3 | B11 | A11 |
| A8 | **B8** | 1 | B12 | A12 |
| A5 | B6 | | B14 | A15 |
| A6 | B5 | | B15 | A14 |
| A2 | B2 | | B18 | A18 |
| A3 | B3 | | B17 | A17 |

All adjacent unused pairs terminated

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## PCB Fixtures (Cont.)

### NEXT: CROSS ROW (Xrow)

| | NEAR END Long | NEAR END Short | | FAR END Short | FAR END Long |
|---|---|---|---|---|---|
| | A17 | B17 | | B3 | A3 |
| | A18 | B18 | | B2 | A2 |
| | A14 | B15 | | B5 | A6 |
| | A15 | B14 | | B6 | A5 |
| | A12 | B12 | | B8 | A8 |
| | A11 | B11 | | B9 | A9 |
| 4 | **A9** | **B9** | 3 | B11 | A11 |
| 2 | **A8** | **B8** | 1 | B12 | A12 |
| | A5 | B6 | | B14 | A15 |
| | A6 | B5 | | B15 | A14 |
| | A2 | B2 | | B18 | A18 |
| | A3 | B3 | | B17 | A17 |

All adjacent unused pairs terminated

### NEXT: Diagonal Cross Row (Diagonal)

| | NEAR END Long | NEAR END Short | | FAR END Short | FAR END Long |
|---|---|---|---|---|---|
| | A17 | B17 | | B3 | A3 |
| | A18 | B18 | | B2 | A2 |
| | A14 | B15 | | B5 | A6 |
| | A15 | B14 | | B6 | A5 |
| 4 | **A12** | B12 | | B8 | A8 |
| 2 | **A11** | B11 | | B9 | A9 |
| | A9 | **B9** | 3 | B11 | A11 |
| | A8 | **B8** | 1 | B12 | A12 |
| | A5 | B6 | | B14 | A15 |
| | A6 | B5 | | B15 | A14 |
| | A2 | B2 | | B18 | A18 |
| | A3 | B3 | | B17 | A17 |

### FEXT: IN ROW - Long Row

| | NEAR END Long | NEAR END Short | FAR END Short | FAR END Long | |
|---|---|---|---|---|---|
| | A17 | B17 | B3 | A3 | |
| | A18 | B18 | B2 | A2 | |
| | A14 | B15 | B5 | A6 | |
| | A15 | B14 | B6 | A5 | |
| | A12 | B12 | B8 | **A8** | 2 |
| | A11 | B11 | B9 | **A9** | 4 |
| 3 | **A9** | B9 | B11 | A11 | |
| 1 | **A8** | B8 | B12 | A12 | |
| | A5 | B6 | B14 | A15 | |
| | A6 | B5 | B15 | A14 | |
| | A2 | B2 | B18 | A18 | |
| | A3 | B3 | B17 | A17 | |

All adjacent unused pairs terminated

### FEXT: IN ROW - Short Row

| NEAR END Long | NEAR END Short | | | FAR END Short | FAR END Long |
|---|---|---|---|---|---|
| A17 | B17 | | | B3 | A3 |
| A18 | B18 | | | B2 | A2 |
| A14 | B15 | | | B5 | A6 |
| A15 | B14 | | | B6 | A5 |
| A12 | B12 | | 2 | **B8** | A8 |
| A11 | B11 | | 4 | **B9** | A9 |
| A9 | **B9** | 3 | | B11 | A11 |
| A8 | **B8** | 1 | | B12 | A12 |
| A5 | B6 | | | B14 | A15 |
| A6 | B5 | | | B15 | A14 |
| A2 | B2 | | | B18 | A18 |
| A3 | B3 | | | B17 | A17 |

**Series:** ECUE
**Description:** FireFly™ Micro Flyover System, 38 AWG Coax Cable, 50cm Cable Length

## PCB Fixtures (Cont.)

### FEXT: CROSS ROW (Xrow)

| | NEAR END | | | FAR END | |
|---|---|---|---|---|---|
| | Long | Short | | Short | Long |
| | A17 | B17 | | B3 | A3 |
| | A18 | B18 | | B2 | A2 |
| | A14 | B15 | | B5 | A6 |
| | A15 | B14 | | B6 | A5 |
| | A12 | B12 | | B8 | A8 |
| | A11 | B11 | | B9 | A9 |
| 3 | **A9** | B9 | 2 | **B11** | A11 |
| 1 | **A8** | B8 | 4 | **B12** | A12 |
| | A5 | B6 | | B14 | A15 |
| | A6 | B5 | | B15 | A14 |
| | A2 | B2 | | B18 | A18 |
| | A3 | B3 | | B17 | A17 |

All adjacent unused pairs terminated

### FEXT: Diagonal Cross Row (Diagonal)

| | NEAR END | | | FAR END | |
|---|---|---|---|---|---|
| | Long | Short | | Short | Long |
| | A17 | B17 | | B3 | A3 |
| | A18 | B18 | | B2 | A2 |
| | A14 | B15 | | B5 | A6 |
| | A15 | B14 | | B6 | A5 |
| | A12 | B12 | 2 | **B8** | A8 |
| | A11 | B11 | 4 | **B9** | A9 |
| 3 | **A9** | B9 | | B11 | A11 |
| 1 | **A8** | B8 | | B12 | A12 |
| | A5 | B6 | | B14 | A15 |
| | A6 | B5 | | B15 | A14 |
| | A2 | B2 | | B18 | A18 |
| | A3 | B3 | | B17 | A17 |

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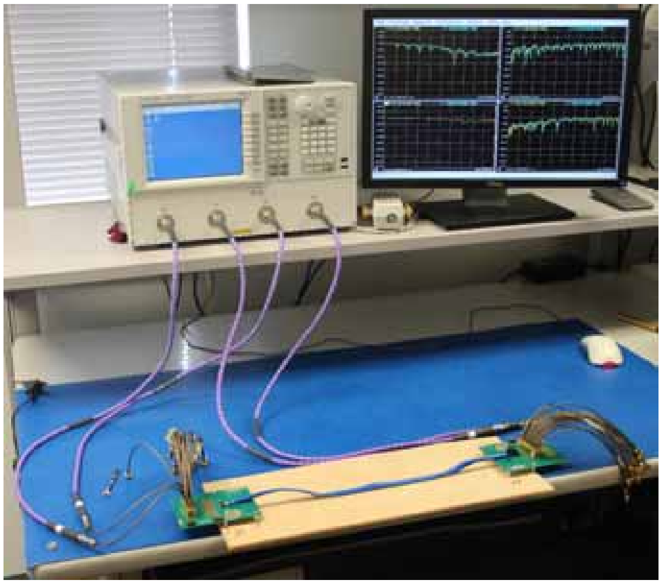
## Appendix E – Test and Measurement Setup

The test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

| | |
|---|---|
| Start Frequency – 300 KHz | Number of points -1601 |
| Stop Frequency – 20 GHz | IFBW – 1 KHz |

With these settings, the measurement time is approximately 20 seconds.

### N5230C Measurement Setup



### Test Instruments

| QTY | Description |
|---|---|
| 1 | Agilent N5230C PNA-L 4-Port Network Analyzer (300 KHz to 20 GHz) |
| 1 | Agilent N4433A Ecal module (300 KHz to 20 GHz) |

### Test Cables & Adapters

| QTY | Description |
|---|---|
| 4 | WL Gore –Z0CJ0CK0360 3.5 mm(f) to 3.5mm(m) Test Port Cables |

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## Appendix F - Frequency and Time Domain Measurements

### Eye Diagram Procedures

Eye Diagrams and statistical eye diagram metrics such as eye height can be generated by post-processing Frequency Domain measurements using Agilent ADS. Simulated data is sent over a touchstone model and the bits are overlain into an eye pattern.

Currently, no CEI specification is available for 14Gbps, so *CEI-28-VSR Working Clause Proposal, CEI Implementation agreement Draft 7.0*, dated May 14, 2012 was used for this report.

The simulation circuit is modeled as:
Agilent's Advanced Design System Tx and Rx modules that are configured to the *CEI-28-VSR Working Clause Proposal, CEI Implementation agreement Draft 7.0*, dated May 14, 2012.

- Tx parameters are specified in Section 1.3.3, *Module-to-Host Specifications*, Table 1-4, Page 7.
- Rx parameters defined in Section 1.3.2 *Host-to-Module Electrical Specifications*, Table 1-1, Page 5.
- A 1.0 inch length of Tx interconnect trace segment at the transmitter.
- SUT Cable Assembly S-Parameter measurements
    - 40 mils of 5 mil wide differential stripline signal trace
    - Test board vias, pads (footprint effects) for the UEC5 connector
    - The UEC5 series connector J1
    - The ECUE cable assembly
    - The UEC5 series connector J2
    - Test board vias, pads (footprint effects) for the UEC5 connector
    - 40 mils of 5 mil wide differential stripline signal trace
- A 1.0 inch length of Rx interconnect trace segment at the receiver.

All traces were modeled as microstrip on FR4 with the following parameters:

- The FR4 parameters are modeled using:
    - Er = 4.2 @ 1 GHz
    - Loss Tangent = 0.02 @ 1 GHz

- Copper is modeled as:
    - Conductivity = 4.5E+7 S-m
    - Surface roughness = 0.6 micron

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- Traces are differential microstrip with the following geometry:
  - 100 ohm differential impedance
  - 4.25 mil trace width
  - 2 mil trace copper thickness
  - 5.75 mil center-to-center spacing
  - 4.4 mil FR4 dielectric thickness

    No differential coupling to neighboring differential channels

Eye Mask
The eye mask is set for 50mVpp, with a jitter margin of 0.5 UI.

Rise Time
The 10-90 risetime of the 14Gbps signal was determined to be 25 psec, using the following formula:

Risetime = 0.35/Bandwidth

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Report Revision: 2/3/2014

**Series:** ECUE
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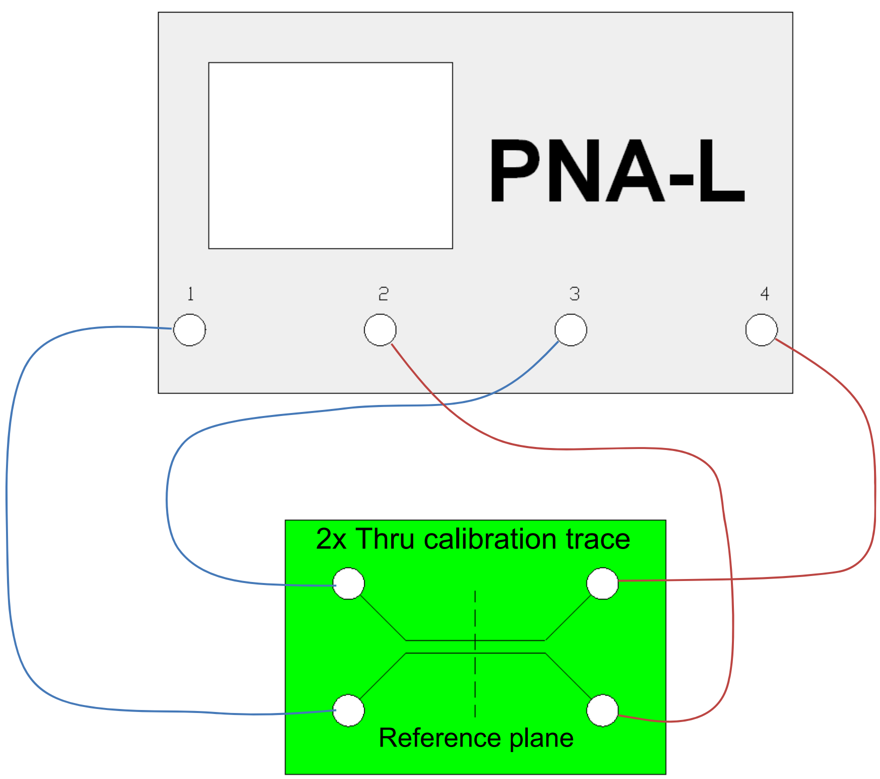
**Frequency (S-Parameter) Domain Procedures**

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the AFR calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the AFR calibration standards. A coaxial SOLT calibration is performed using an N4433A E-cal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the FireFly™ test boards, this is greater than 20 GHz.

The figure below shows how the THRU reference traces are utilized to compensate for the losses due to the coaxial test cables and the test fixture during testing. The calibration board is characterized to obtain parameters required to define the 2x Thru.



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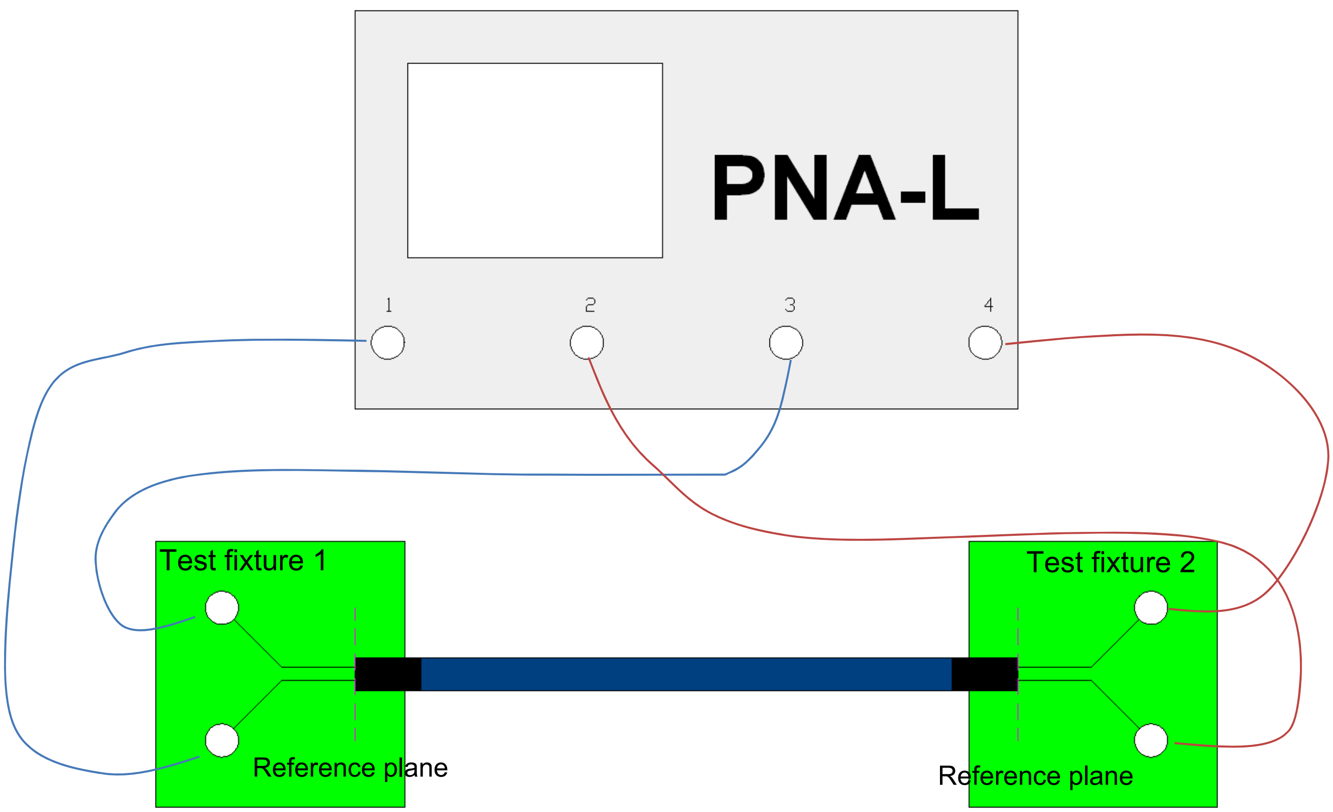
Measurements are then performed using the test boards as shown below. The test board effects are removed in post-processing via AFR in Agilent PLTS. The calibrated reference plane is located 40 mils from the connector footprint on each side. The S-Parameter measurements include:

A. 40 mils of 5 mil wide differential stripline signal trace
B. Test board vias, pads (footprint effects) for the UEC5 connector
C. The UEC5 series connector J1
D. The ECUE test cable
E. The UEC5 series connector J2
F. Test board vias, pads (footprint effects) for the UEC5 connector
G. 40 mils of 5 mil wide differential stripline signal trace

The test boards used for this characterization had a differential trace impedance of 112 ohms. Unfortunately, this impedance offset cascades through the AFR process and distorting the impedance and return loss measurements. For this reason, AFR was not applied to the impedance and return loss data in this report.

The figure below shows the location of the measurement reference plane.



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## Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 10. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Documents/WebFiles/Technical_Library/Reference/Articles/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)
A step pulse is applied to the touchstone model of the cable assembly and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the cable assembly and footprint. A step pulse is applied to the touchstone model of the cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

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## Appendix G – Glossary of Terms

ADS – Agilent Advanced Design System
AFR – Automatic Fixture Removal
CTLE – Continuous Time Linear Analyzer
CuFireFly™ - Copper FireFly™ assembly
DUT – Device under test
FD – Frequency domain
FEXT – Far-End Crosstalk
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PLTS – Agilent Physical Layer Design System
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
UI – Unit Interval
XROW – Across Row
Z – Impedance (expressed in ohms)