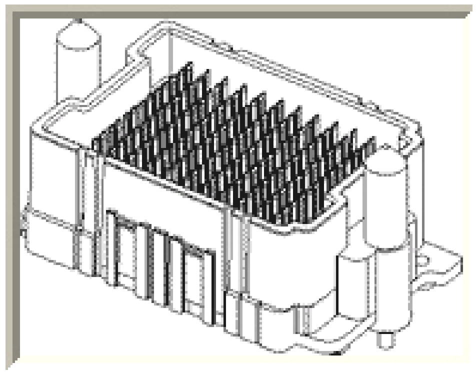
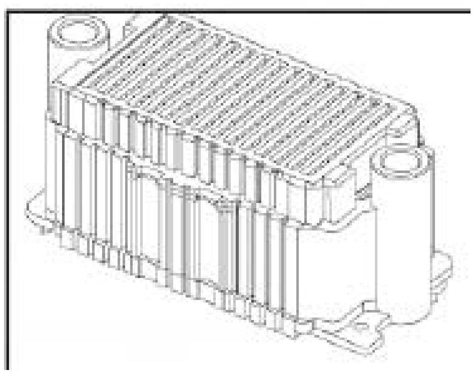
High Speed Characterization Report

HDAM-15-17.0-S-13-2



Mates with

HDAF-15-08.0-S-13-2



Description:
HDMezz Elevated Array, 1.2mm x 2mm Grid Interconnect
25mm Stack Height

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Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

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Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Connector Overview

HDAM/HDAF is a 1.2mm x 2mm grid interconnects system for elevated high-speed board-to-board applications. The high density array's open pin field design allows both single-ended and differential pair routing. The HDAM/HDAF Series is developed with 143, 195, or 299 signal routing selections. The series is available in 20mm, 25mm 30mm, and 35 mm stack heights. This report depicts the hi-speed electrical characteristics specific to a mated 25mm stack height HDAM/HDAF board-to-board test system.

Connector System Speed Rating

HDAM/HDAF Series, 1.2mm x 2mm (.0472" x .0875") grid interconnect, 25mm Stack Height

Signaling	Speed Rating
Single-Ended:	**8.5 GHz / 17Gbps**
Differential:	**8.5 GHz / 17Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board's trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

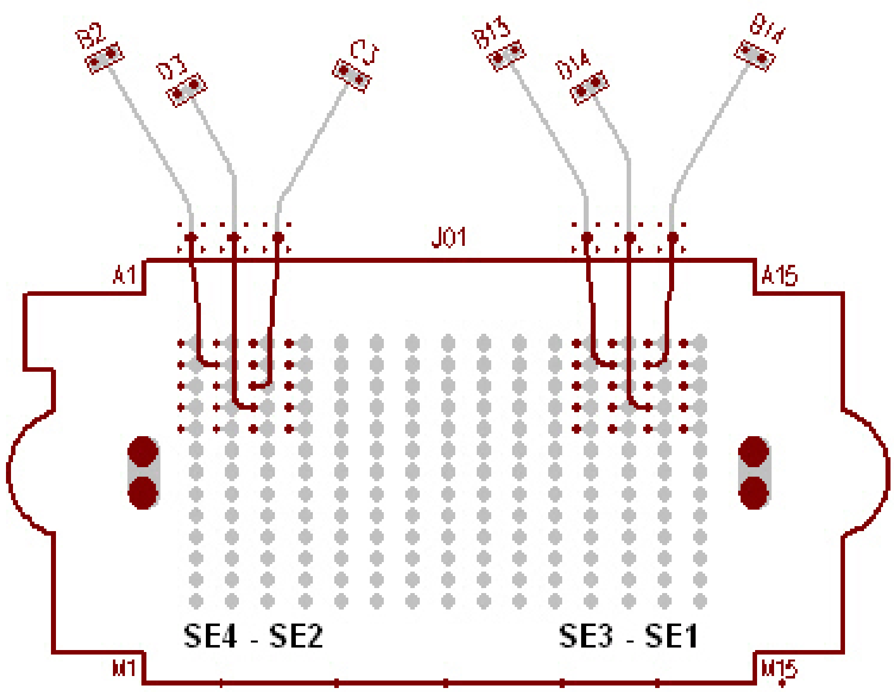
For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Frequency Domain Data Summary

Table 1 - Single-Ended Signaling System Performance			
Test Parameter	**Source**	**Victim**	
Insertion Loss	port1=HDAM_B14; port2=HDAF_B14	[redacted]	-3dB @ 8.20 GHz
Return Loss	port1=HDAM_B14; port2=HDAF_B14	[redacted]	≤ -5dB to 8.20 GHz
Near-End Crosstalk	HDAM_C3	HDAM_D3	≤ - 8dB to 8.20 GHz
	HDAM_B14	HDAM_D14	≤ -25dB to 8.20 GHz
	HDAM_B14	HDAM_B13	≤ -22dB to 8.20 GHz
	HDAM_C3	HDAM_B2	≤ -22dB to 8.20 GHz
Far-End Crosstalk	HDAM_C3	HDAF_D3	≤ -10dB to 8.20 GHz
	HDAM_B14	HDAF_D14	≤ -18dB to 8.20 GHz
	HDAM_B14	HDAF_B13	≤ -20dB to 8.20 GHz
	HDAM_C3	HDAF_B2	≤ -22dB to 8.20 GHz

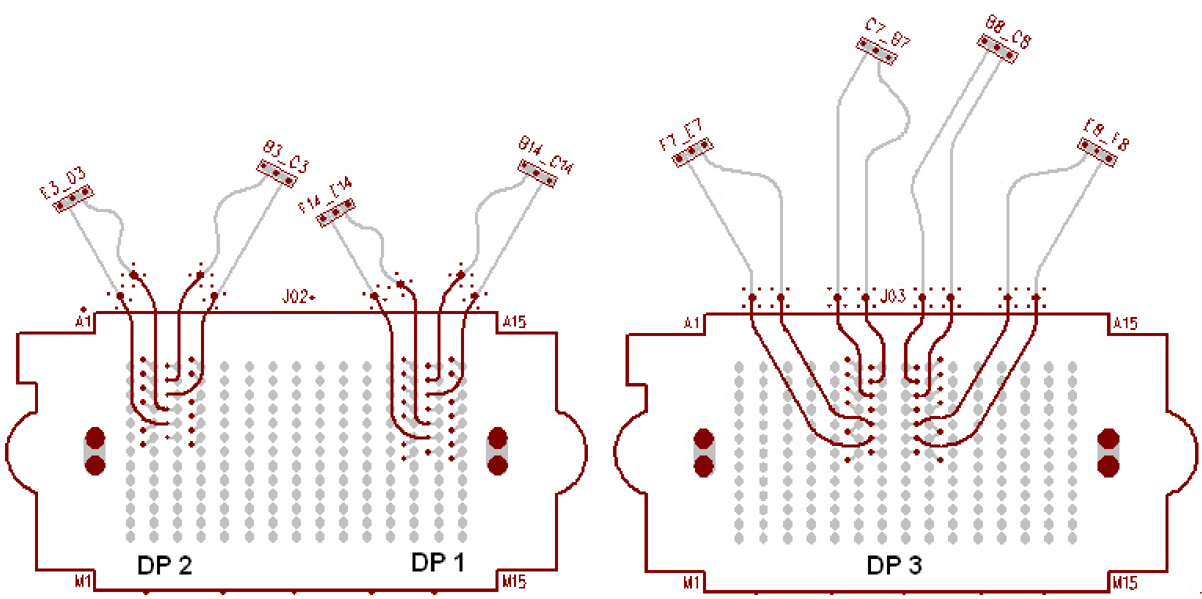
Pin Map (reference Appendix C for full description of test boards)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

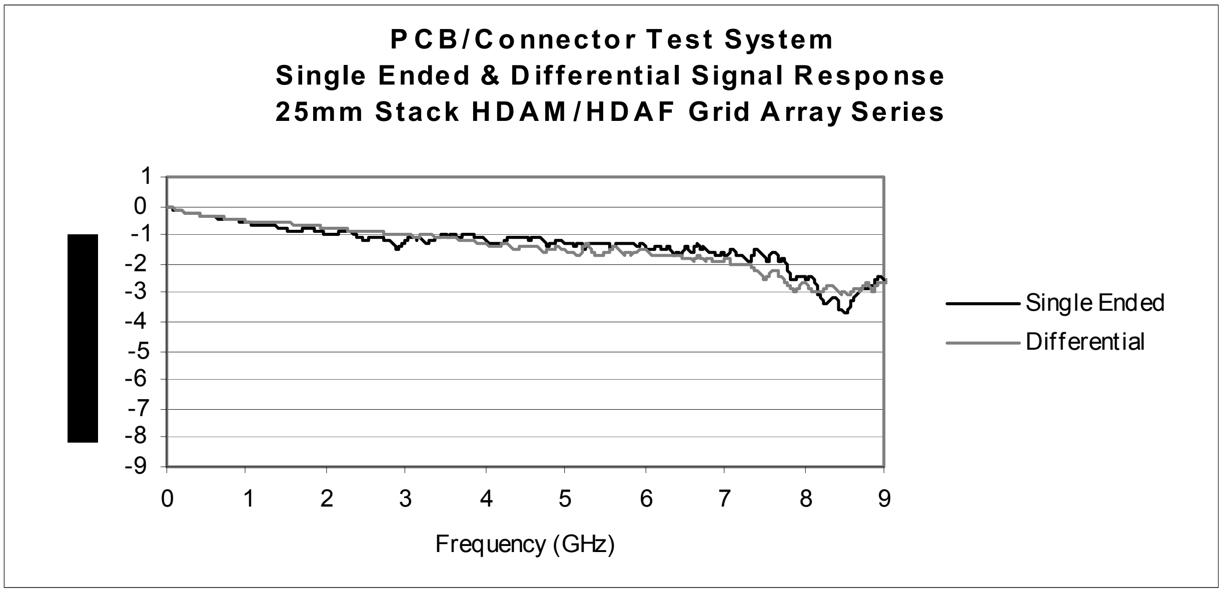
Table 2 – Differential Pair Signaling System Performance			
Test Parameter	**Source**	**Victim**	
Insertion Loss	port1=HDAM_B14-C14; port2=HDAF_B14-C14	[redacted]	-3dB @ 8.20 GHz
Return Loss	port1=HDAM_B14-C14; port2=HDAF_B14-C14		≤ -5dB to 8.20 GHz
Near-End Crosstalk	HDAM_B3-C3	HDAM_D3-E3	≤ -15dB to 8.20 GHz
	HDAM_B14-C14	HDAM_E14-F14	≤ -35dB to 8.20 GHz
	HDAM_E8-F8	HDAM_E7-F7	≤ -28dB to 8.20 GHz
	HDAM_E8-F8	HDAM_B7-C7	≤ -38dB to 8.20 GHz
Far-End Crosstalk	HDAM_B3-C3	HDAF_D3-E3	≤ -25dB to 8.20 GHz
	HDAM_B14-C14	HDAF_E14-F14	≤ -32dB to 8.20 GHz
	HDAM_E8-F8	HDAM_E7-F7	≤ -28dB to 8.20 GHz
	HDAM_E8-F8	HDAM_B7-C7	≤ -38dB to 8.20 GHz

Pin Map (reference Appendix C for full description of test boards)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Bandwidth Chart – Single-Ended & Differential Insertion Loss



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω) – Line B14 (SE1)							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	65.3	64.7	63.2	59.6	56.1	54.8	54.0
Minimum Impedance	46.6	48.1	49.1	49.8	50.2	50.4	50.5

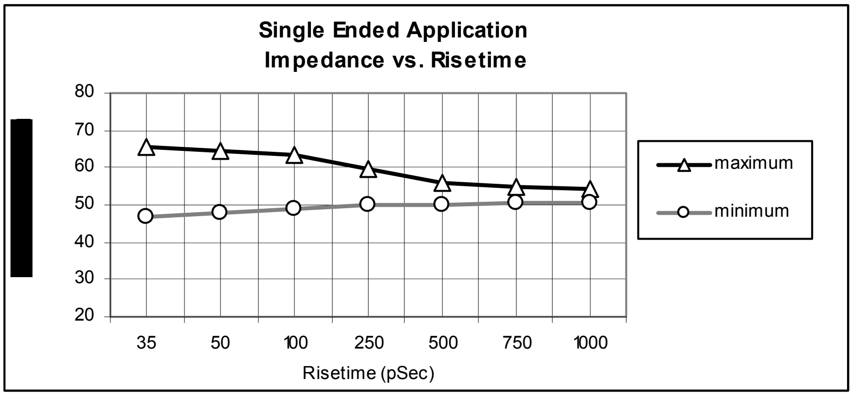
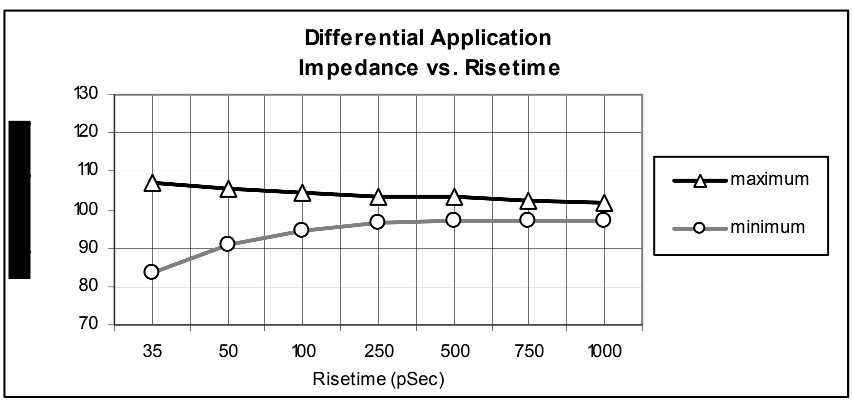


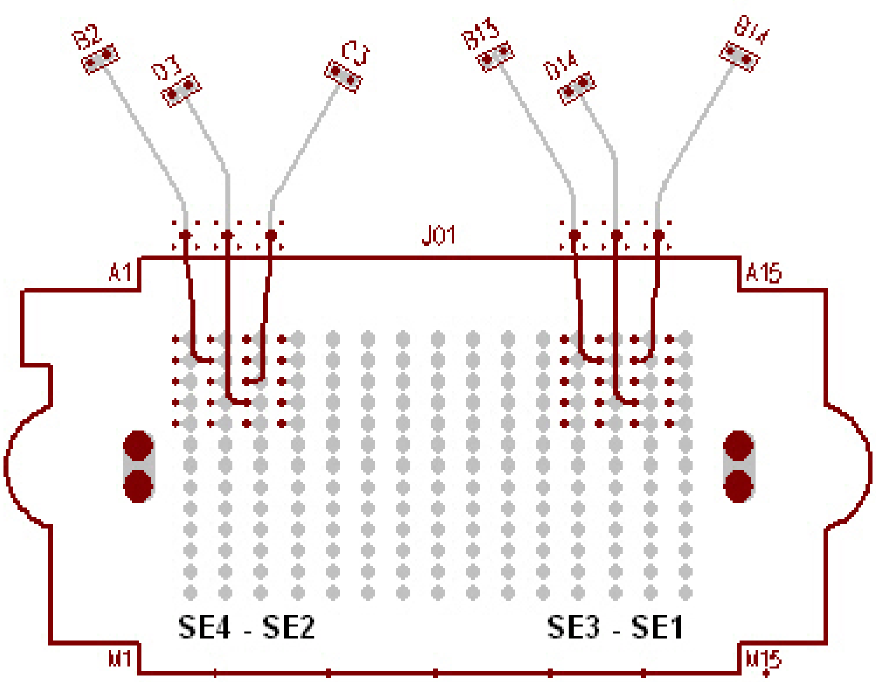
Table 4 - Differential Impedance (Ω) – Pair B14-C14 (DP1)							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	107.1	105.6	104.5	103.6	103.2	102.5	101.9
Minimum Impedance	83.6	91.0	94.7	96.8	97.0	97.1	97.1



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Table 5 - Single-Ended Crosstalk (%)									
Input (t_r)	**Source**	**Victim**	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
NEXT	HDAM_C3	D3	15.9	15.2	14.7	12.0	7.8	5.7	4.5
	HDAM_B14	D14	1.2	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	HDAM_B14	B13	3.8	3.3	3.1	2.5	1.6	1.2	< 1.0%
	HDAM_C3	B2	2.2	2.1	1.9	1.5	1.0	< 1.0%	< 1.0%
FEXT	HDAM_C3	D3	7.9	5.3	3.7	3.2	2.1	1.6	1.3
	HDAM_B14	D14	1.6	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	HDAM_B14	B13	4.1	2.7	1.7	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	HDAM_C3	B2	2.3	1.6	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%

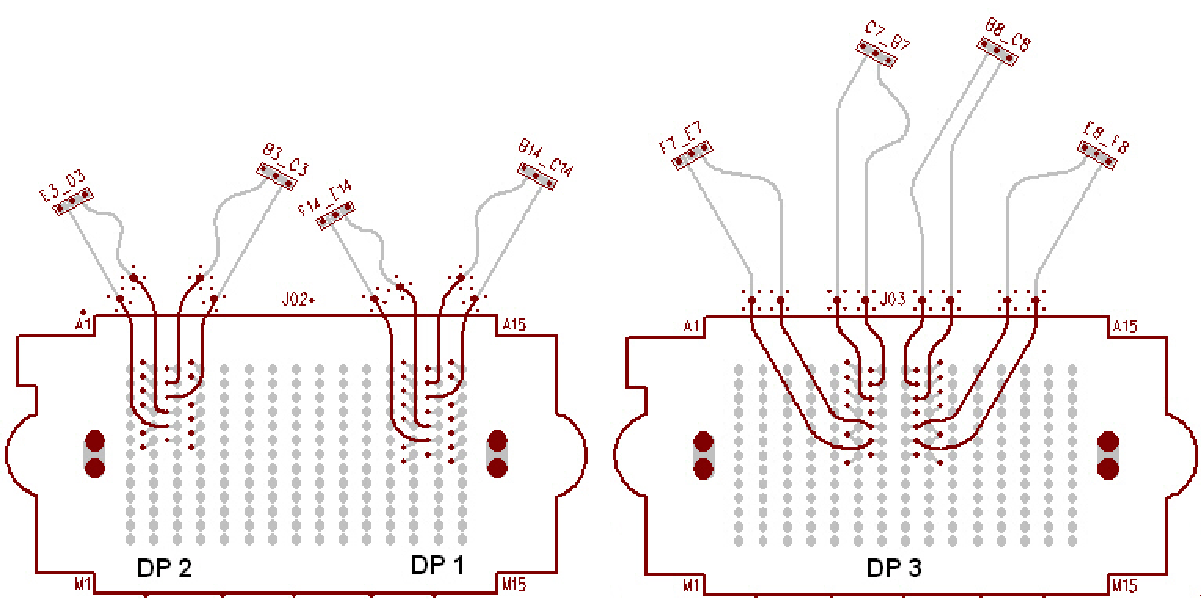
Pin Map (reference Appendix C for full description of test boards)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Table 6 – Differential Crosstalk (%)									
Input (t_r)	**Source**	**Victim**	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
NEXT	HDAM B3-C3	D3-E3	5.4	5.2	5.0	4.1	2.5	1.8	1.4
	HDAM B14-C14	E14-F14	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	HDAM E8-F8	E7-F7	1.9	1.6	1.5	1.3	< 1.0%	< 1.0%	< 1.0%
	HDAM E8-F8	B7-C7	1.1	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	HDAM B3-C3	D3-E3	3.9	2.6	1.8	1.6	1.0	< 1.0%	< 1.0%
	HDAM B14-C14	E14-F14	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	HDAM E8-F8	E7-F7	2.0	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	HDAM E8-F8	B7-C7	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)



Series: HDAM/HDAF Series (HDMezz)
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Table 7 - Propagation Delay (Mated Connector)	
Single-Ended	151ps
Differential	166ps

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Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others; connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

For this connector, the following array configurations are evaluated:

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

	open pin field
X	grounded pin field
P#	signal aggressor or signal victim pins

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
M																M
L																L
K																K
J																J
I																I
H																H
G																G
F																F
E	X	X	X	X								X	X	X	X	E
D	X	X	D3	X								X	X	D14	X	D
C	X	X	C3	X								X	X	X	X	C
B	X	B2	X	X								X	B13	B14	X	B
A	X	X	X	X								X	X	X	X	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
		SE4	SE2										SE3	SE 1		

<u>Single-Ended Impedance</u>**:**

- Well-referenced line (reference SE1:1)

<u>Single-Ended Crosstalk</u>**:**

- Well-referenced line; mimics 1:1 S:G ratio (reference SE1:1)
- 2:1 S:G ratio (reference SE2:1)

Only one single-ended signal was driven for crosstalk measurements.

Series: HDAM/HDAF Series (HDMezz)
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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
M																M
L																L
K																K
J																J
I																I
H																H
G													X	X	X	G
F	X	X	X	X									X	F14	X	F
E	X	X	E3	X									X	E14	X	E
D	X	X	D3	X									X	X	X	D
C	X	X	C3	X									X	C14	X	C
B	X	X	B3	X									X	B14	X	B
A	X	X	X	X									X	X	X	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

DP 2 DP 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
M																M
L																L
K																K
J																J
I																I
H																H
G						X	X	X	X							G
F						X	F7	F8	X							F
E						X	E7	E8	X							E
D						X	X	X	X							D
C						X	C7	C8	X							C
B						X	B7	B8	X							B
A						X	X	X	X							A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

DP3

Differential Impedance:

- Well-referenced line (reference DP1)

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Differential Crosstalk**:**

- Well-referenced line; mimics 1:1 S:G ratio (reference DP1)
- Higher Signal Density (reference DP3)
- Full-Column Differential (reference DP2)

Only one differential pair was driven for crosstalk measurements.

In all cases where a center ground blade is present in the connector it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect, can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 35 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT's frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 35 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 35 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

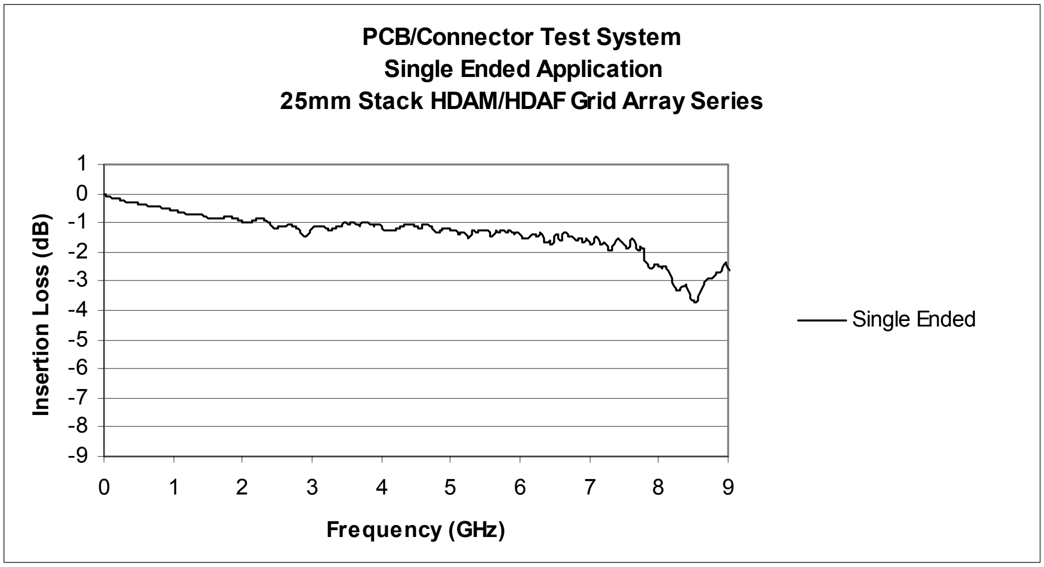
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Appendix A – Frequency Domain Response Graphs

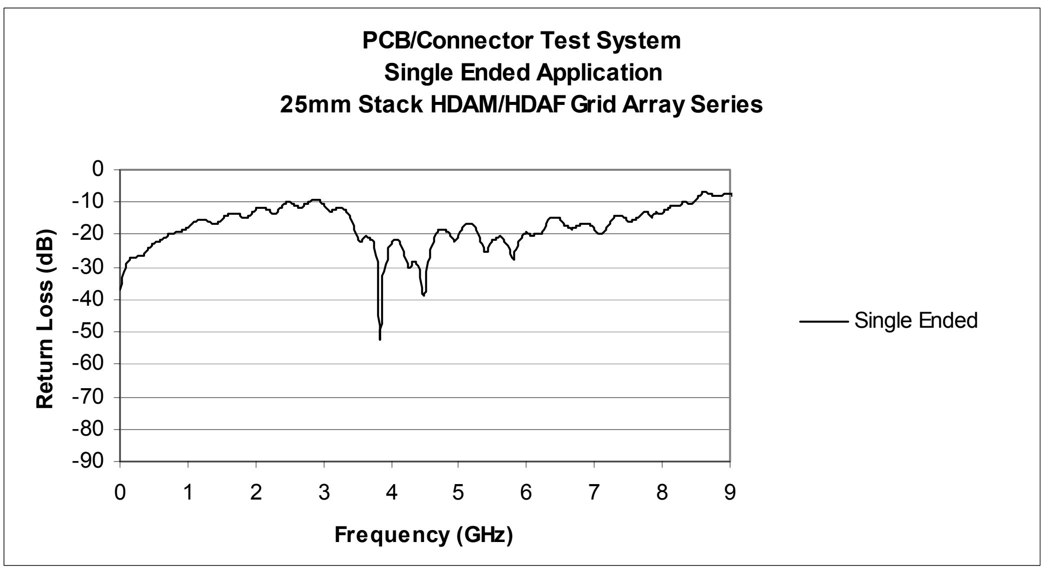
Single-Ended Application – Insertion Loss

Configuration: (Port1 = HDAM_B14; Port2 = HDAF_B14)



Single-Ended Application – Return Loss

Configuration: (Port1 = HDAM_B14)



Series: HDAM/HDAF Series (HDMezz)
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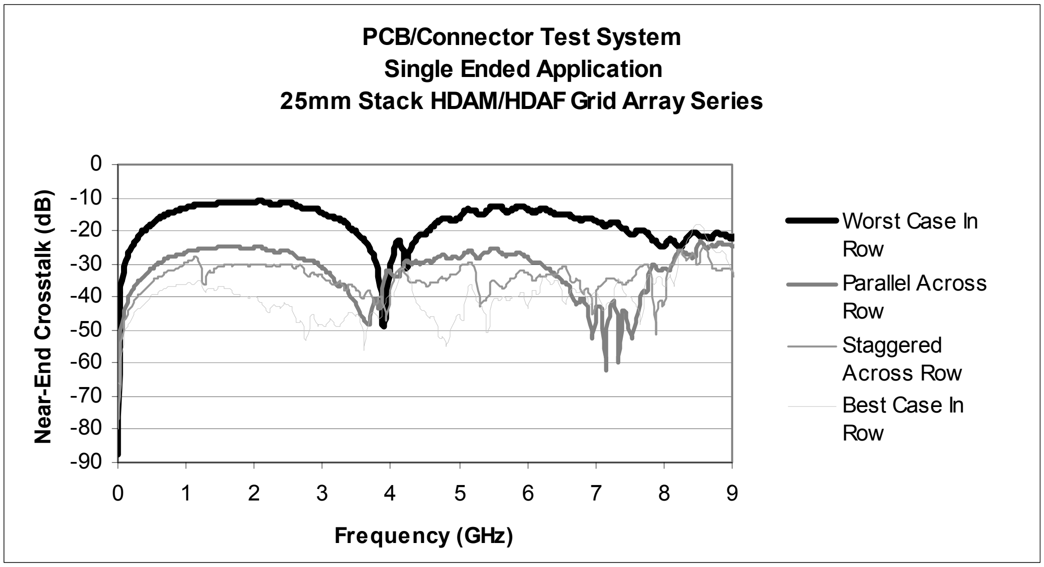
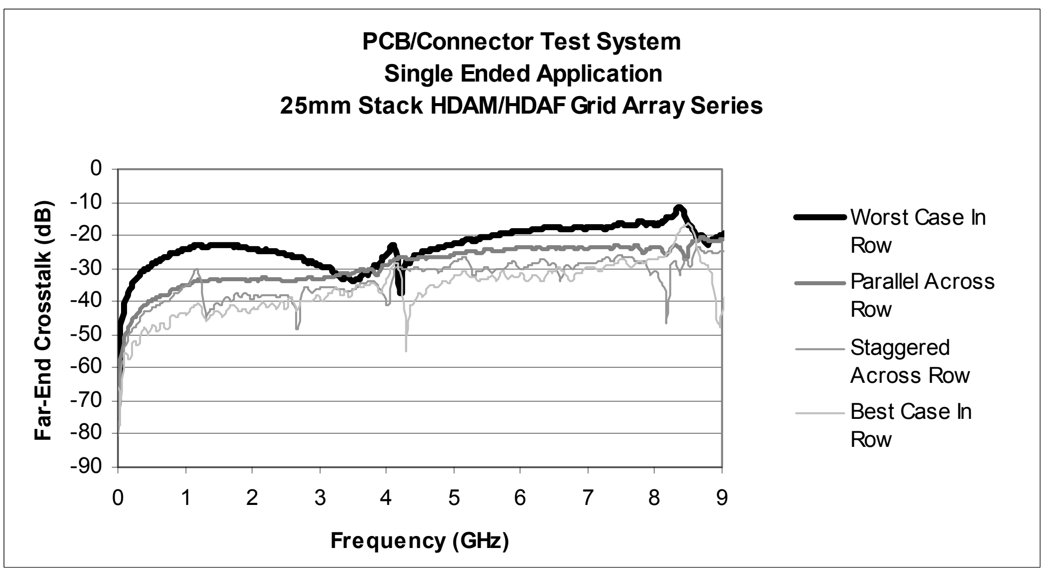
Single-Ended Application – NEXT



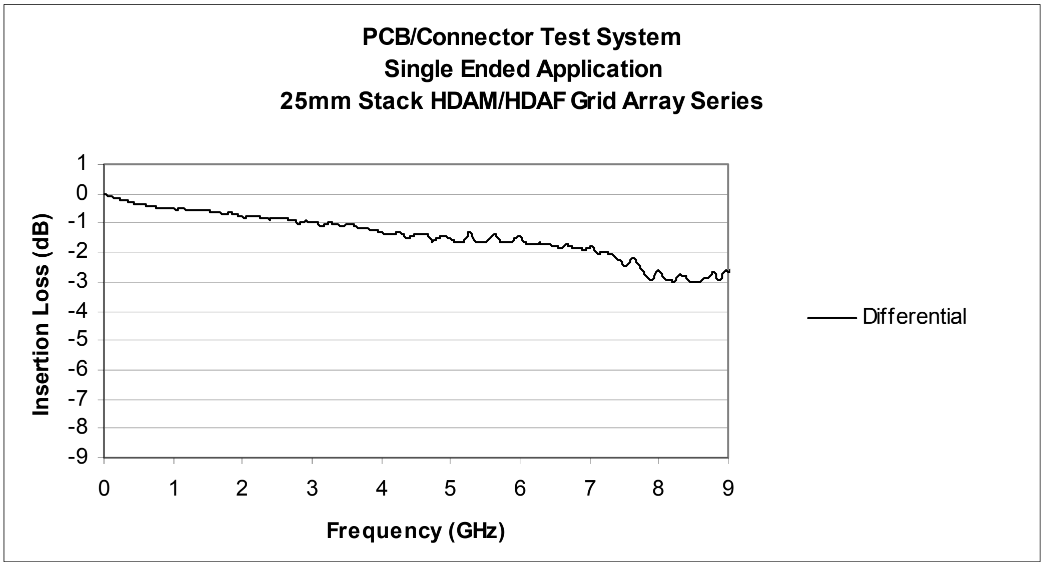
Single-Ended Application – FEXT



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

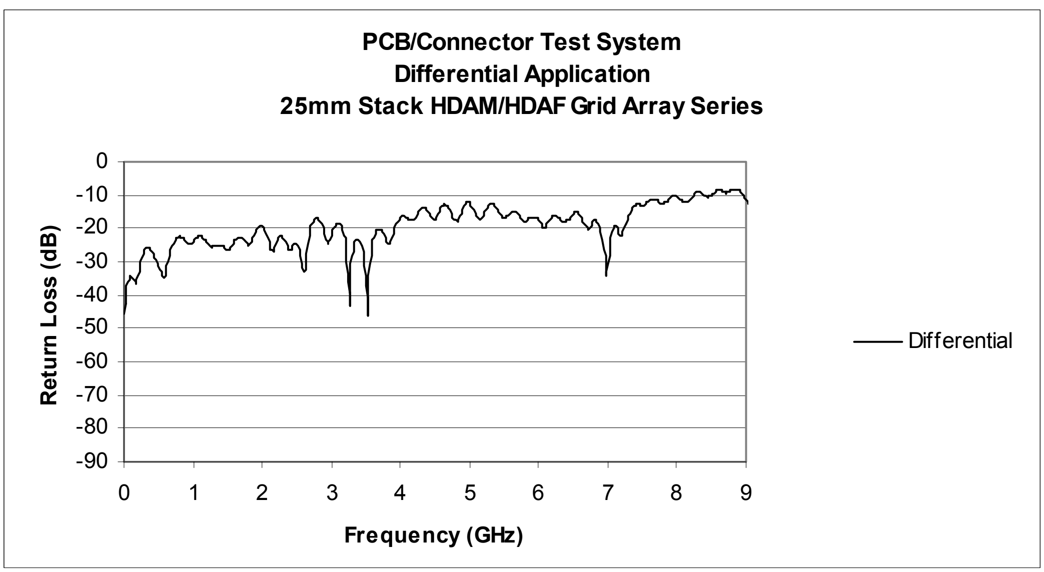
Differential Application – Insertion Loss

Configuration: (Port1 = HDAM_B14-C14; Port2 = HDAF_B14-C14)



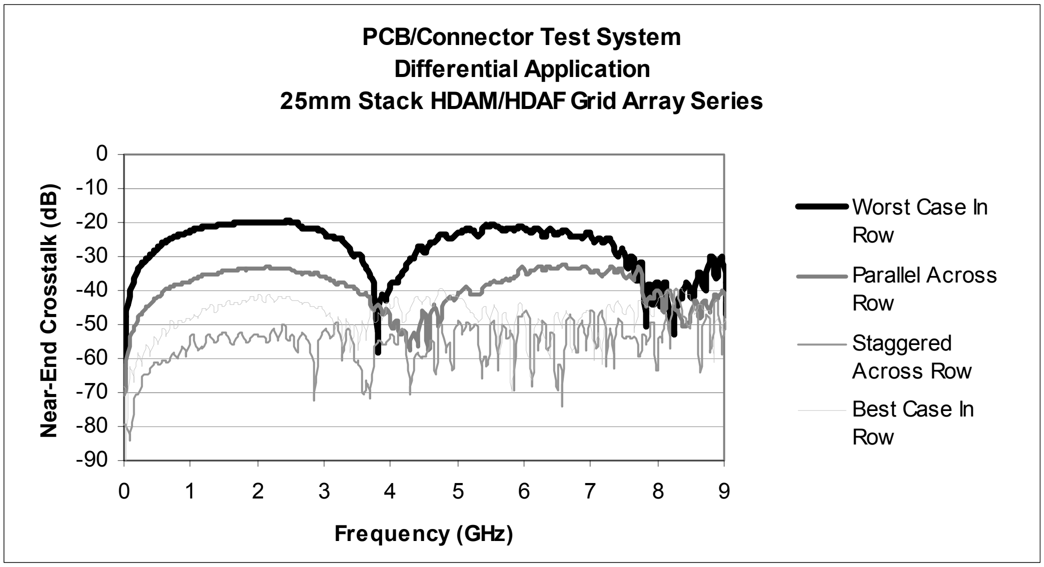
Differential Application – Return Loss

Configuration: (Port1 = HDAM_B14-C14)

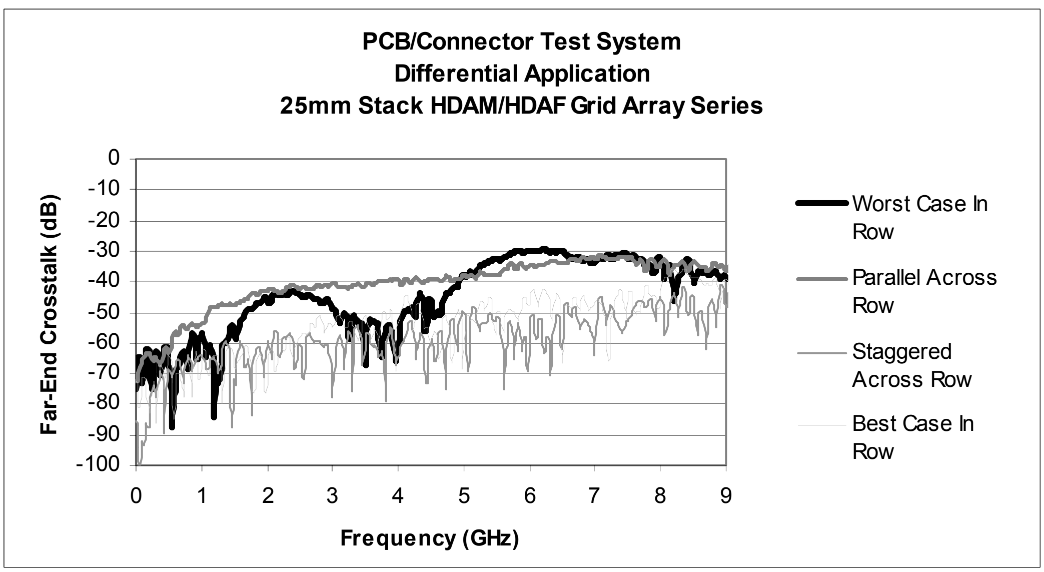


Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Differential Application – NEXT



Differential Application – FEXT



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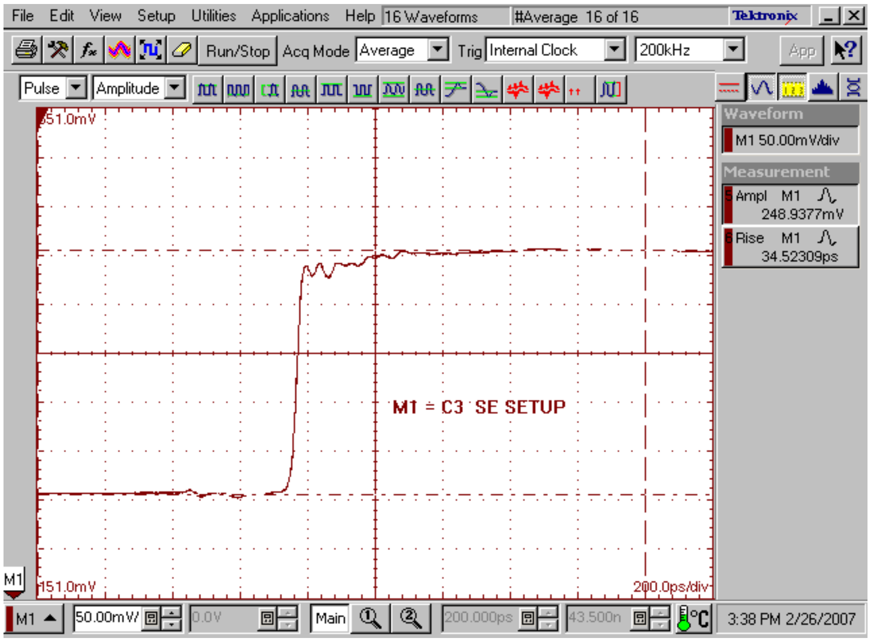
Report Revision: 6/4/2007

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Appendix B – Time Domain Response Graphs

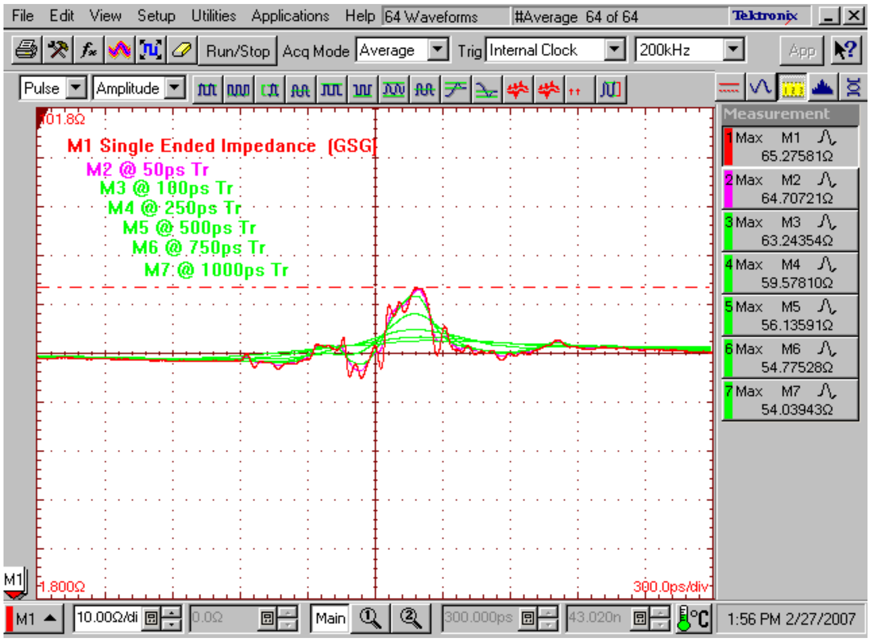
Single-Ended Application – Input Pulse



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

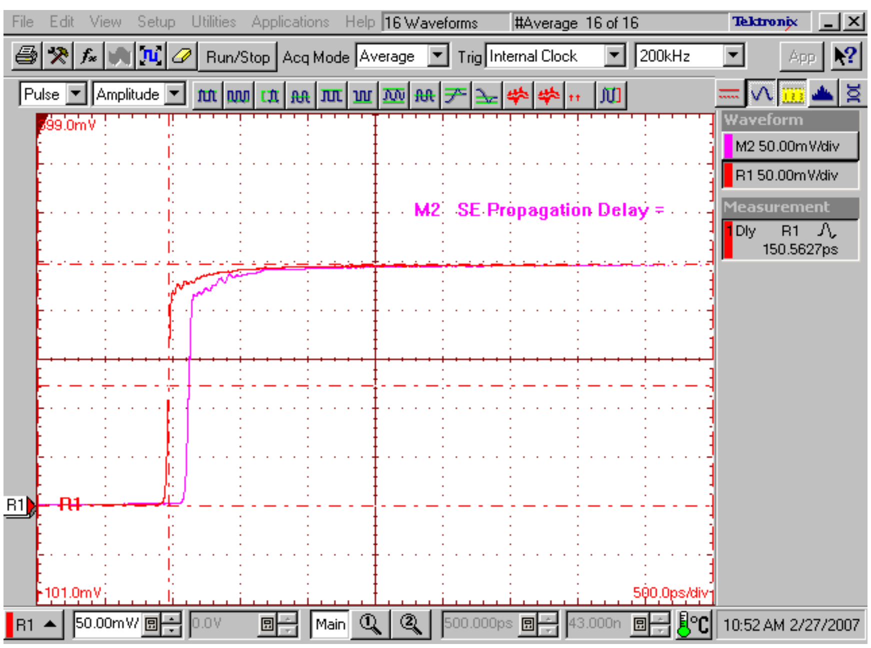
Single-Ended Application – Impedance

Configuration: (Port1 = HDAM_B14)



Single-Ended Application – Propagation Delay

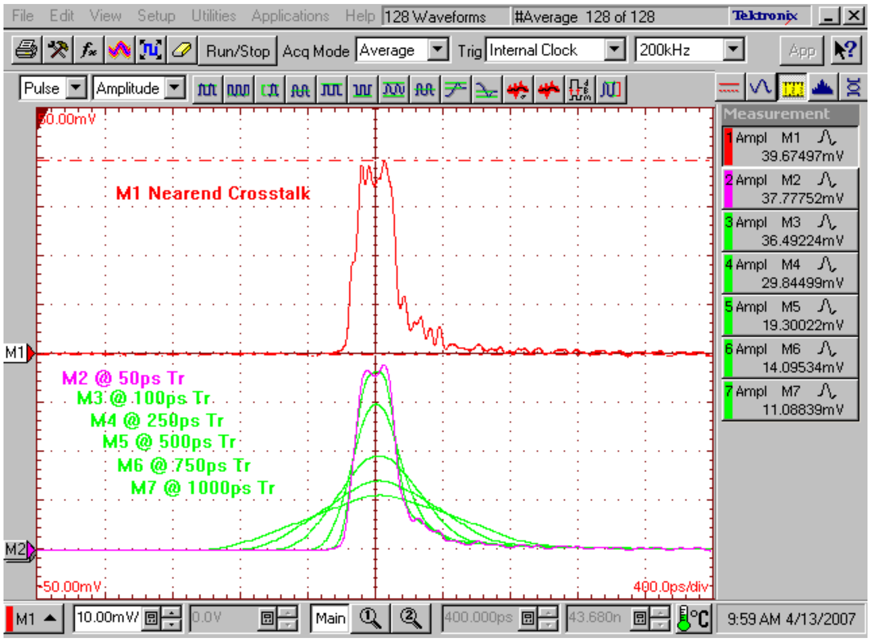
Configuration: (Port1 = HDAM_B14; Port2 = HDAF_B14)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

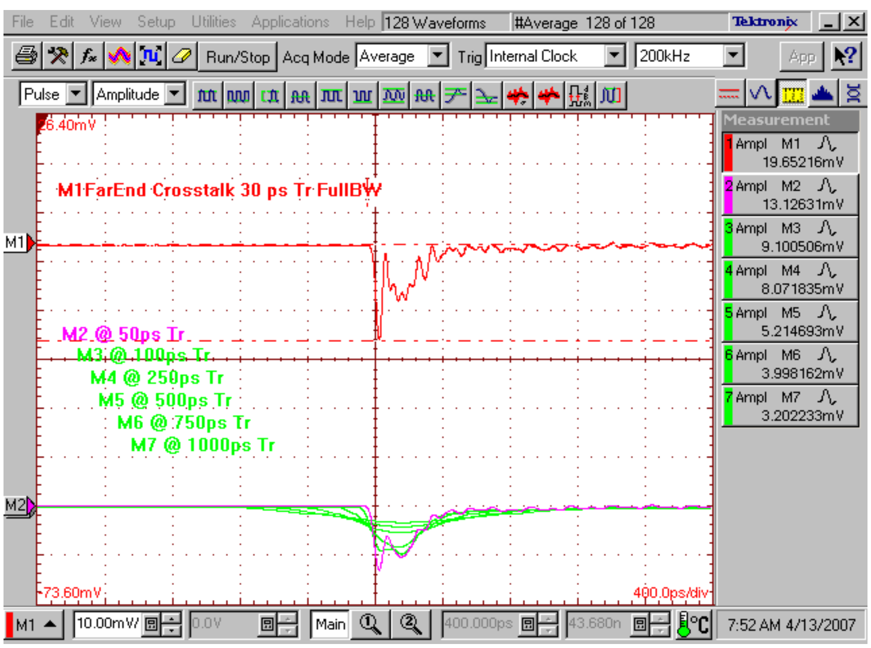
Single-Ended Application – NEXT, "Worst Case SE 2" Configuration

Configuration: (Port1 = HDAM_C3; Port3 = HDAM_D3)



Single-Ended Application – FEXT, "Worst Case SE 2" Configuration

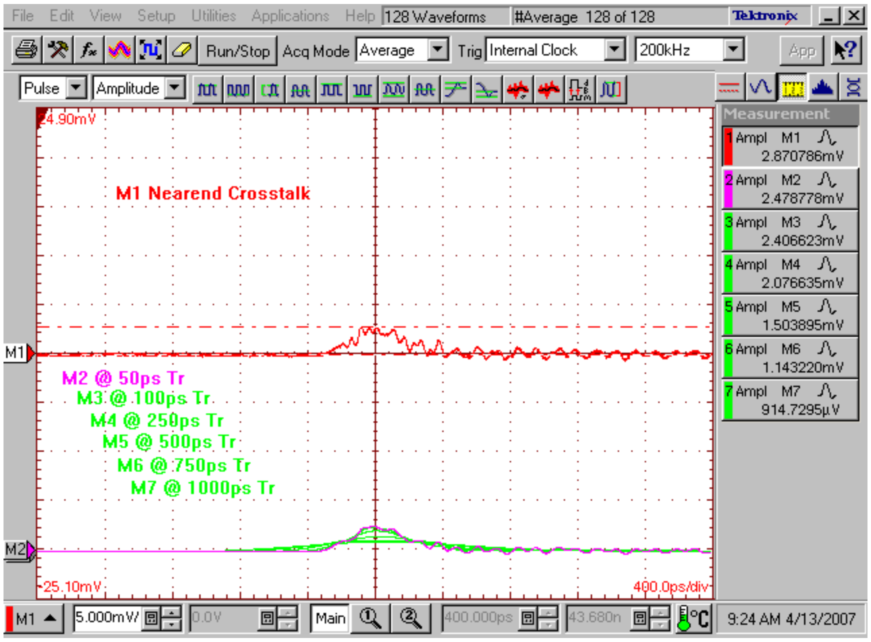
Configuration: (Port1 = HDAM_C3; Port4 = HDAF_D3)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

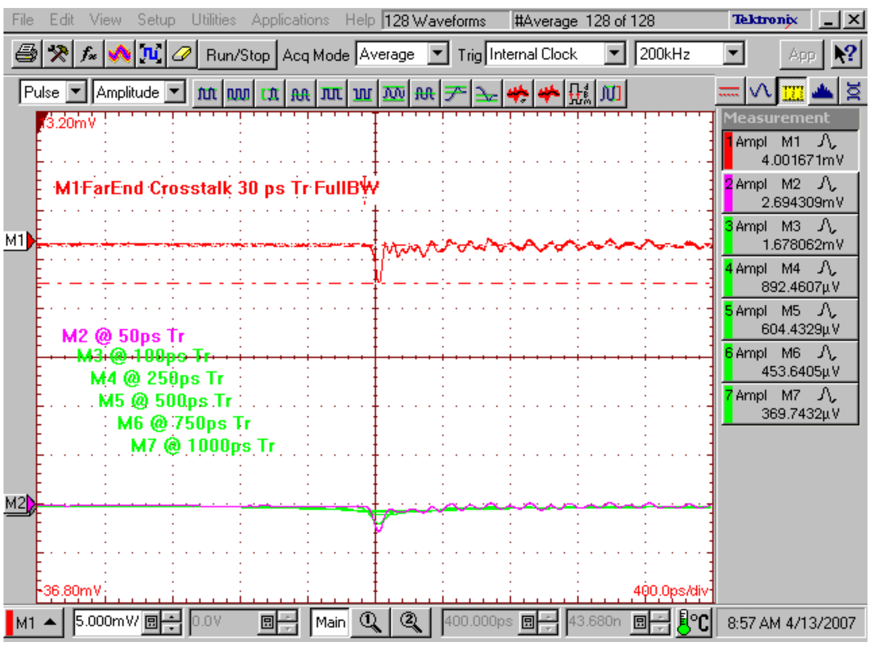
Single-Ended Application – NEXT, "Best Case SE 1" Configuration

Configuration: (Port1 = HDAM_C3; Port3 = HDAM_D14)



Single-Ended Application – FEXT, "Best Case SE 1" Configuration

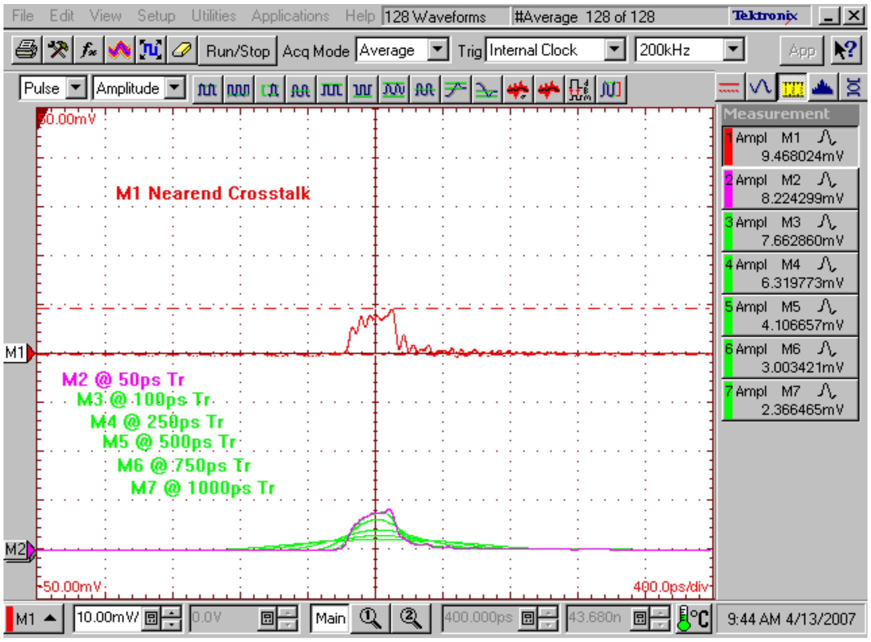
Configuration: (Port1 = HDAM_C3; Port4 = HDAF_D14)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

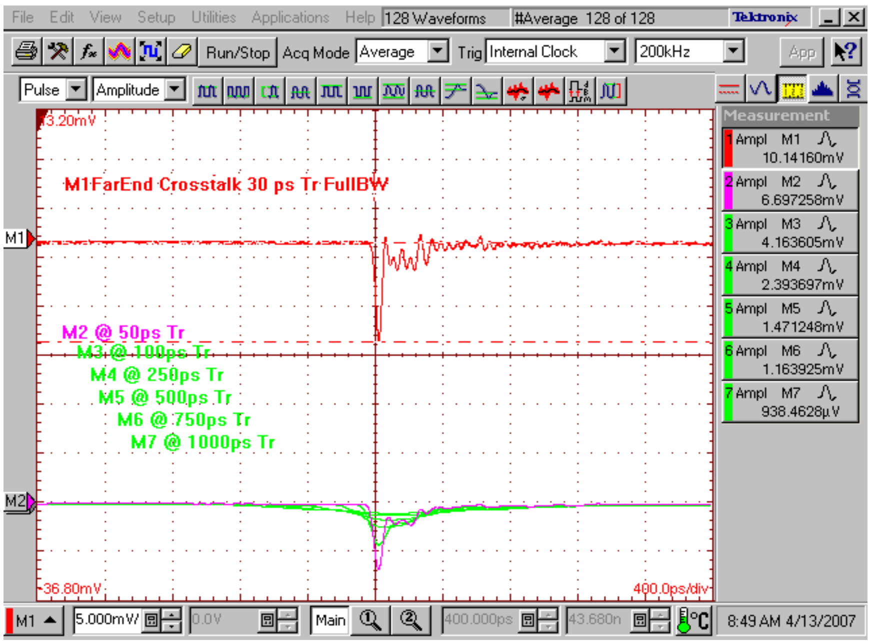
Single-Ended Application – NEXT, "Worst Case SE 4" Configuration

Configuration: (Port1 = HDAM_B14; Port3 = HDAM_B13)



Single-Ended Application – FEXT, "Worst Case SE 4" Configuration

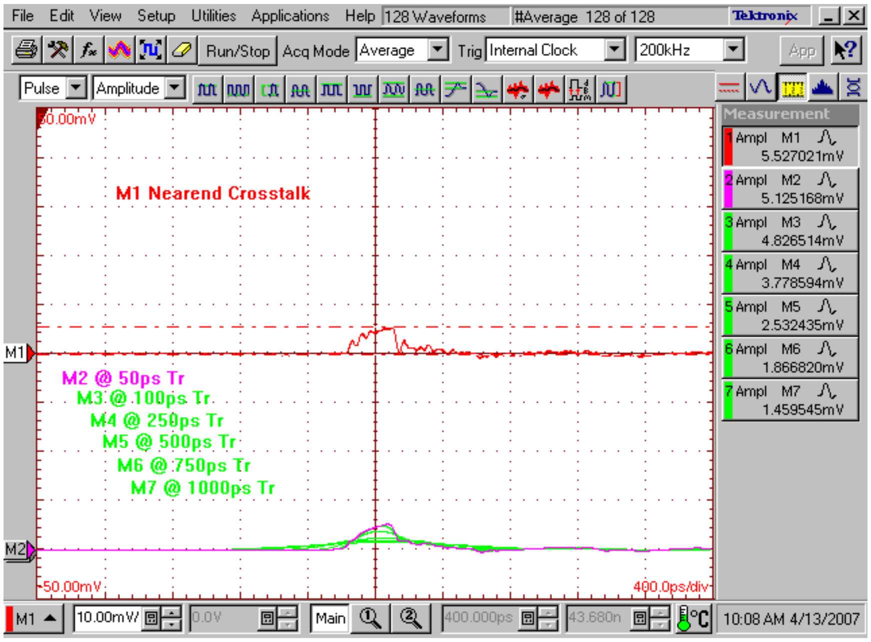
Configuration: (Port1 = HDAM_B14; Port4 = HDAF_B13)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

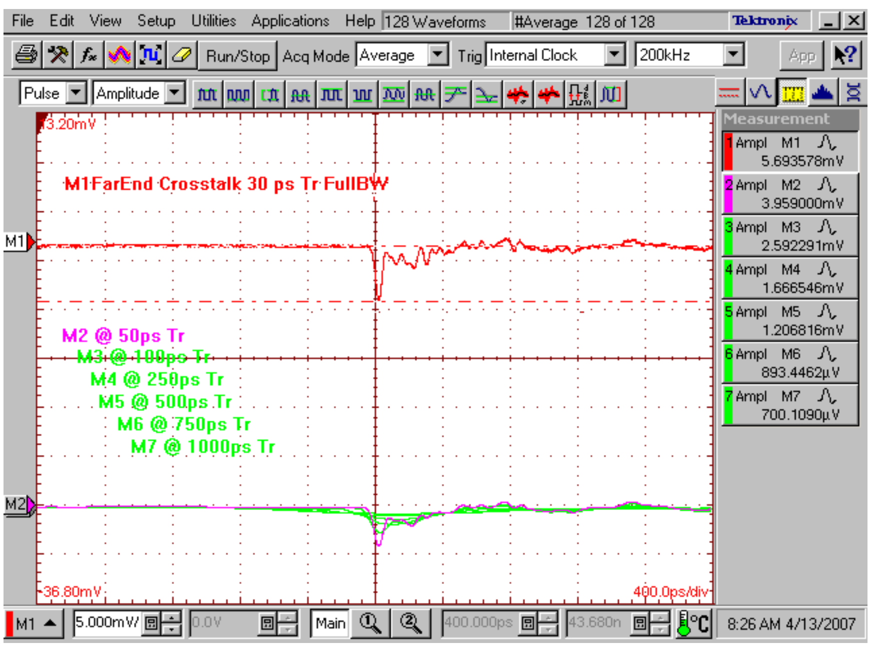
Single-Ended Application – NEXT, "Best Case SE 3" Configuration

Configuration: (Port1 = HDAM_C3; Port3 = HDAM_B2)



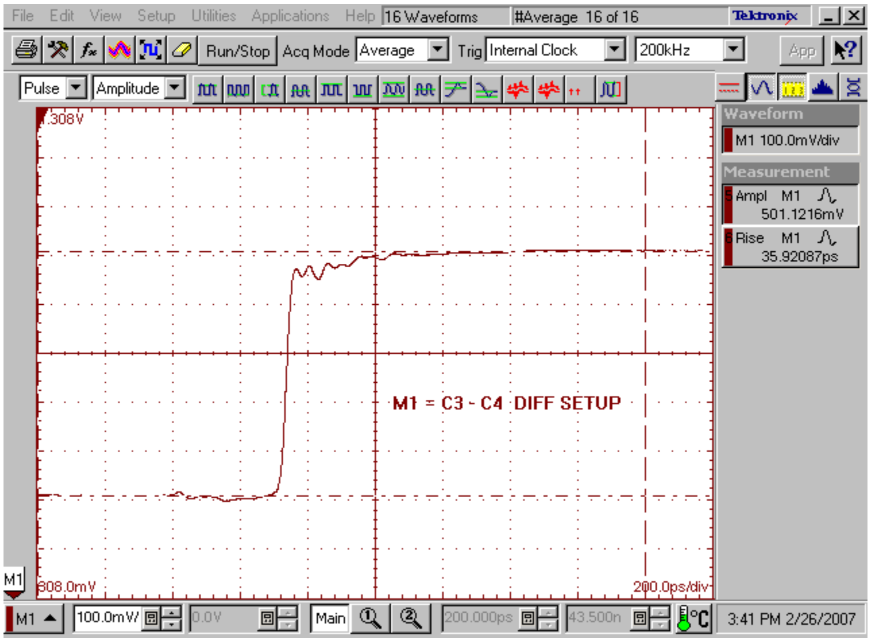
Single-Ended Application – FEXT, "Best Case SE 3" Configuration

Configuration: (Port1 = HDAM_C3; Port4 = HDAF_B2)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

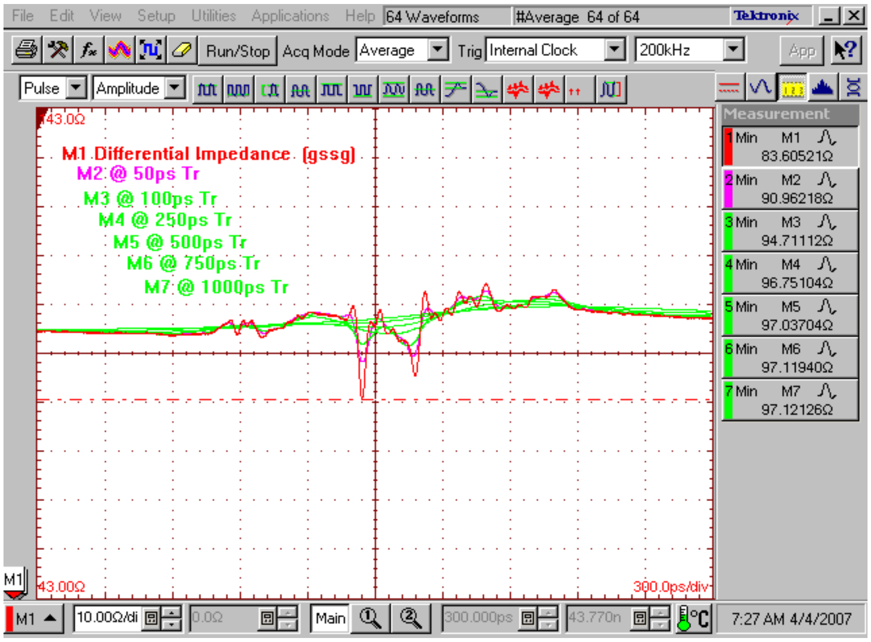
Differential Application – Input Pulse



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

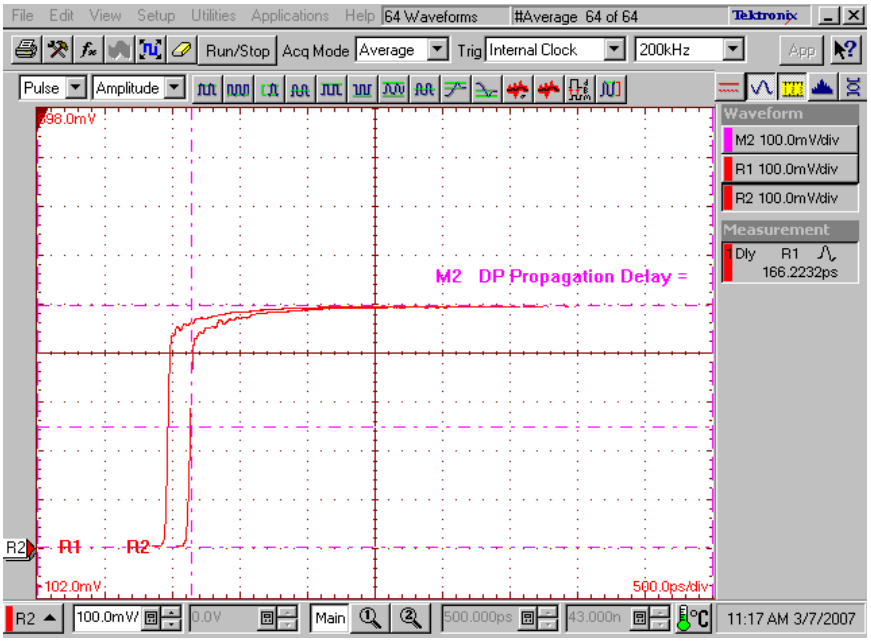
Differential Application – Impedance

Configuration: (Port1 = HDAM_B14-C14)



Differential Application – Propagation Delay

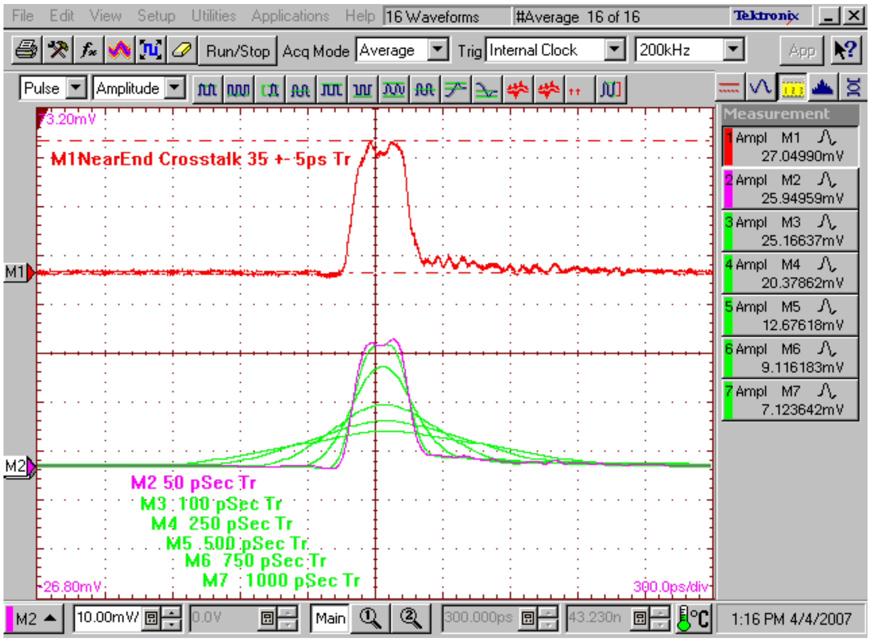
Configuration: (Port1 = HDAM_B14-C14; Port2 = HDAF_B14-C14)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

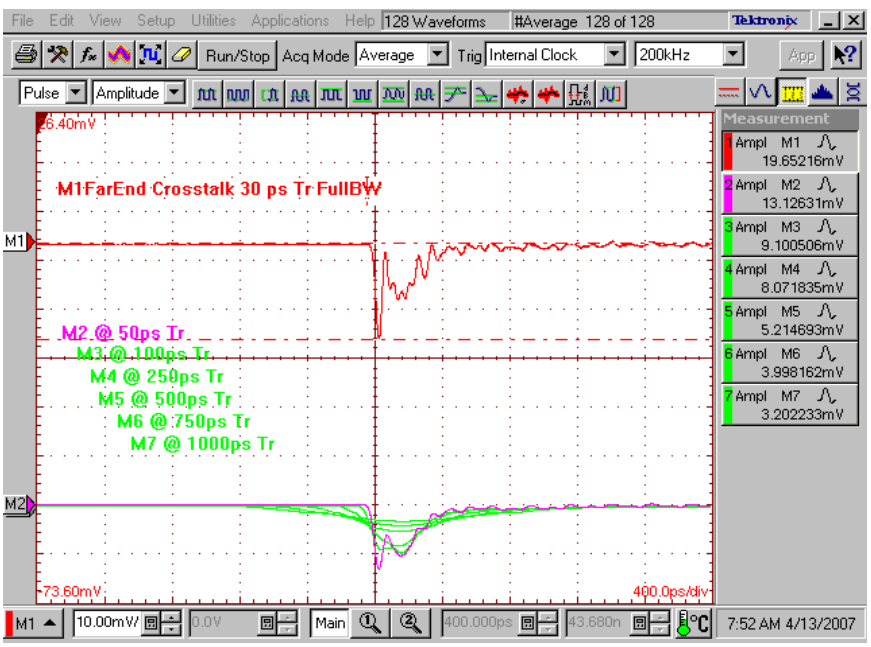
Differential Application – NEXT, "Worst Case DP 2" Configuration

Configuration: (Port1 = HDAM_B3-C3; Port3 = HDAM_D3-E3)



Differential Application – FEXT, "Worst Case DP 2" Configuration

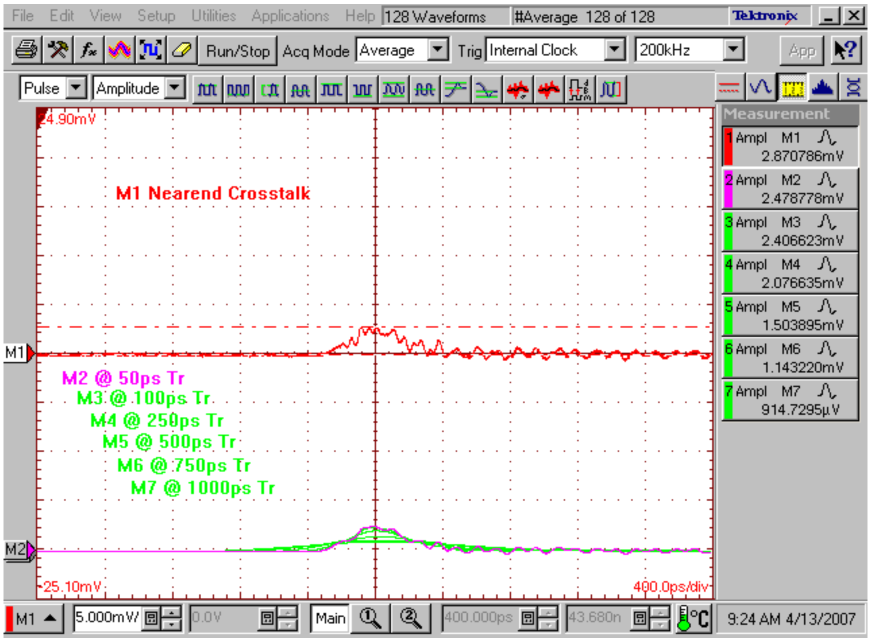
Configuration: (Port1 = HDAM_B3-C3; Port4 = HDAF_D3-E3)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

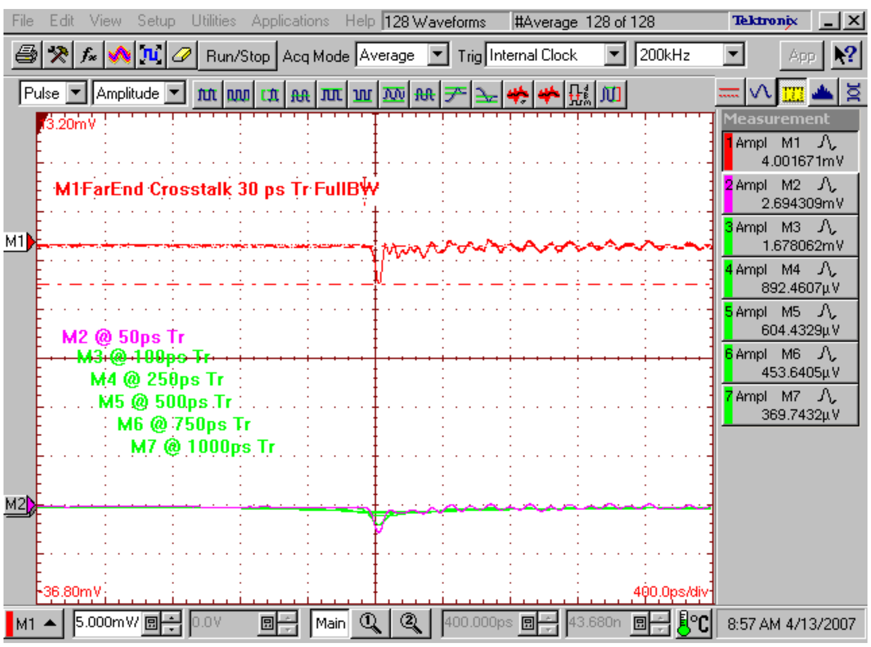
Differential Application – NEXT, "Best Case DP 1" Configuration

Configuration: (Port1 = HDAM_B14-C14; Port3 = HDAM_E14-F14)



Differential Application – FEXT, "Best Case DP 1" Configuration

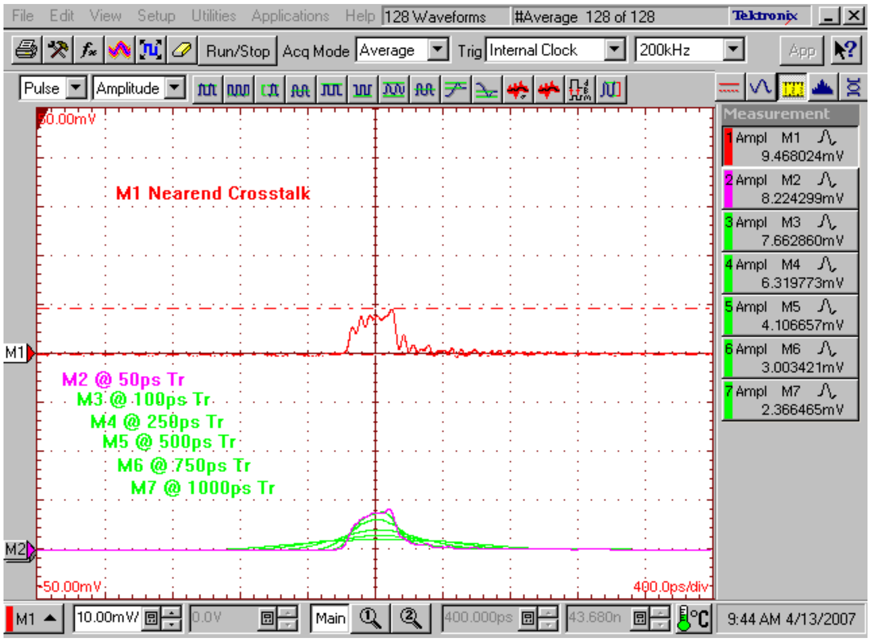
Configuration: (Port1 = HDAM_B14-C14; Port4 = HDAF_E14-F14)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

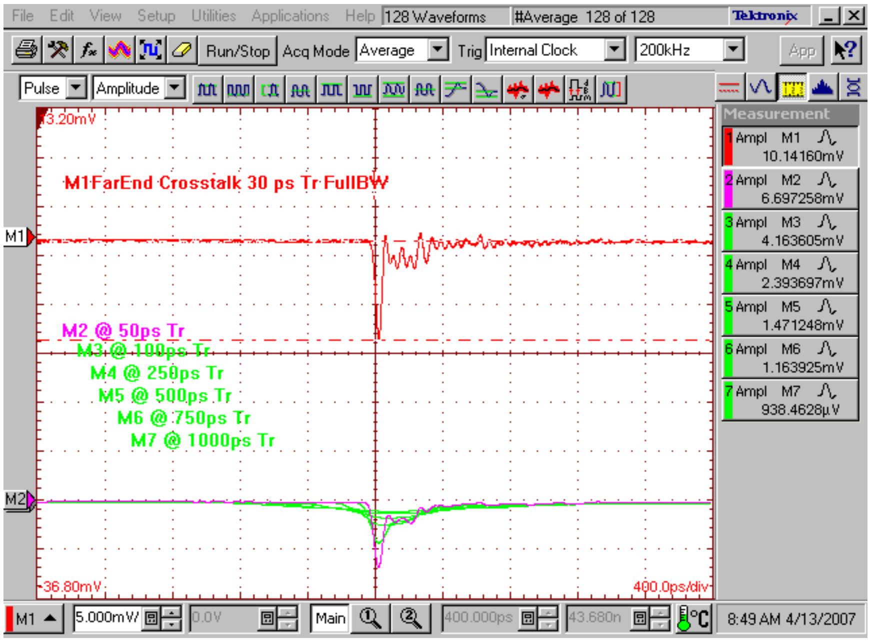
Differential Application – NEXT, "Worst Case DP 3" Configuration

Configuration: (Port1 = HDAM_E8-F8; Port3 = HDAM_E7-F7)



Differential Application – FEXT, "Worst Case DP 3" Configuration

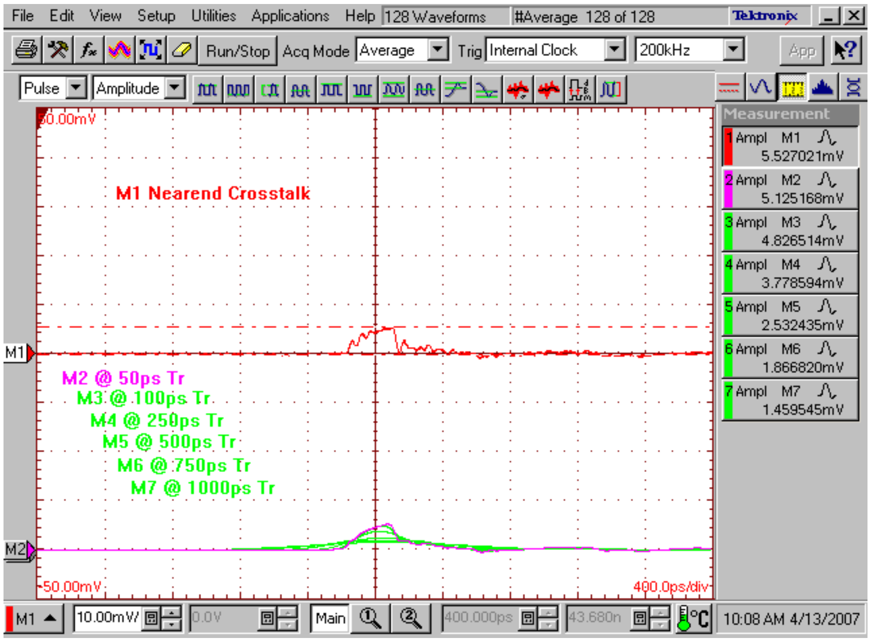
Configuration: (Port1 = HDAM_E8-F8; Port4 = HDAF_E7-F7)



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

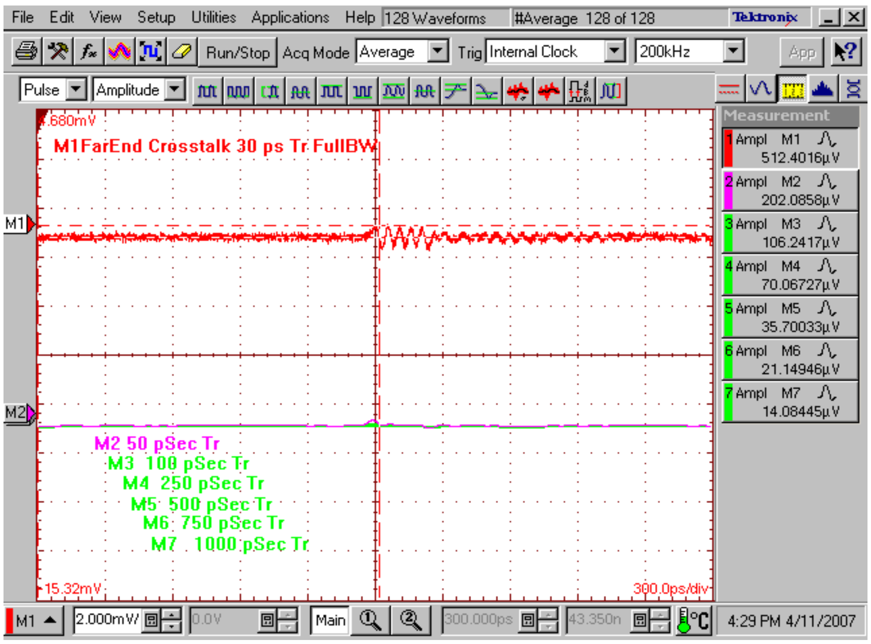
Differential Application – NEXT, "Best Case DP 3" Configuration

Configuration: (Port1 = HDAM_E8-F8; Port3 = HDAM_B7-C7)



Differential Application – FEXT, "Best Case DP 3" Configuration

Configuration: (Port1 = HDAM_E8-F8; Port4 = HDAF_B7-C7)

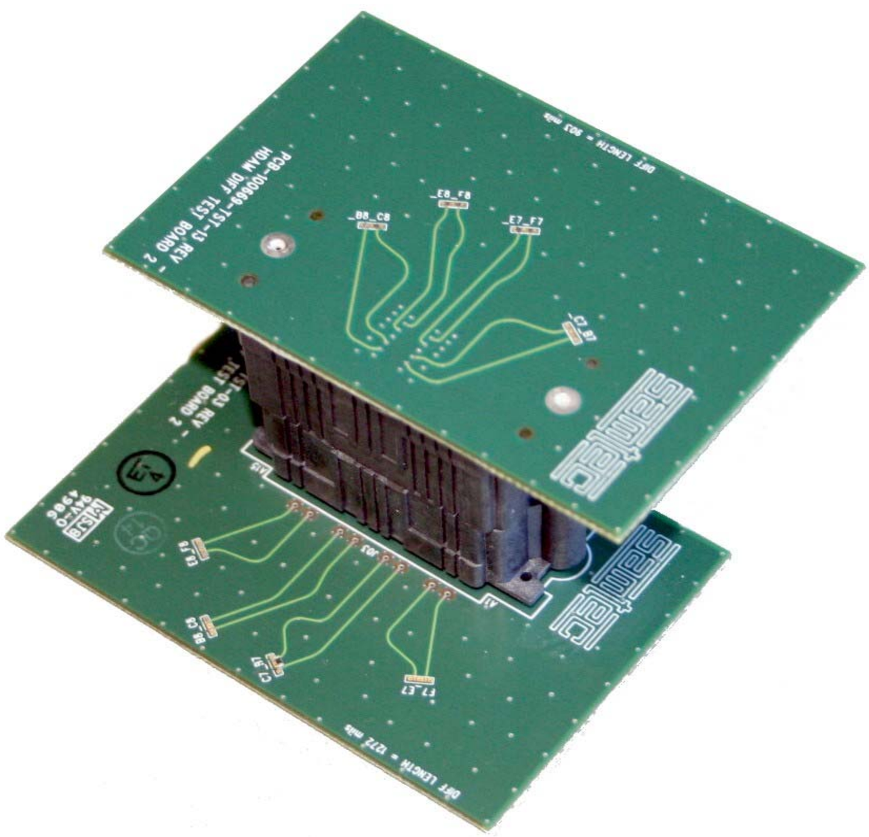


Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Appendix C – Product and Test System Descriptions

Product Description
HDMezz is a high-density array connector designed with open pin fields for differential or single-ended signaling options. The HDAM-15-17.0-S-13-12 /HDAF-15-18.0-S-13-2 mating array design includes 13 signal rows providing 15 signal pins per row. Board-to-Board mating provides a 35mm elevation.

Test System Description
The test fixtures are composed of a 4-layer FR-4 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. The fixture pictured is 1 of 3 signaling card conventions required for a full SI characterization. Configuration conventions and the application details are on the following pages.



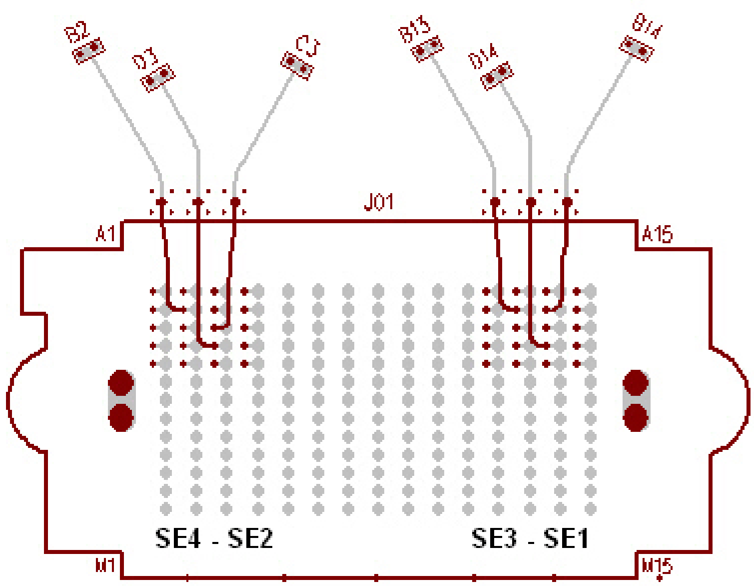
Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Single-Ended Characterization Conditions

Fixture Identity
PCB-100669-TST-11 REV – HDAM SE TEST BOARD
PCB-100669-TST-01 REV – HDAF SE TEST BOARD

SE THRU Parameters - Insertion Loss, Return Loss, Propagation Delay, Impedance
Configuration: GSG
SE 1 HDAM_B14, HDAF_B14

Crosstalk Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT
Configuration: GAVG, 2:1
SE 2 Near-End HDAM_C3, HDAM_D3
Far-End HDAM_C3, HDAF_D3
Configuration: GAGVG, 1:1
SE 1 Near-End HDAM_B14, HDAM_D14
Far-End HDAM_B14, HDAF_D14
Configuration: GAVG/GAVG, 1:1
SE 4 Near-End HDAM_B14, HDAM_B13
Far-End HDAM_B14, HDAF_B13
Configuration: GAGVG/GAGVG, 2:1
SE 3 Near-End HDAM_C3, HDAM_B2
Far-End HDAM_C3, HDAF_B2



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

DP 1 & DP 2 Characterization Conditions

Fixture Identity
PCB-100669-TST-12 REV – HDAM DIFF TEST BOARD 1
PCB-100669-TST-02 REV – HDAF DIFF TEST BOARD 1

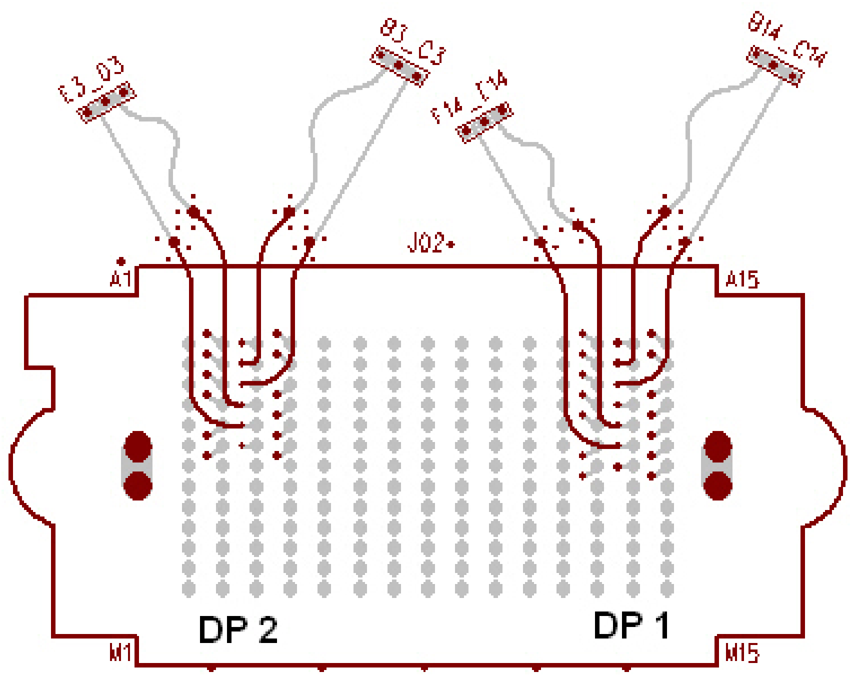
Thru Parameters - Insertion Loss, Return Loss, Propagation Delay, Impedance
Configuration: GSSG
DP 1 HDAM_B14-C14, HDAF_B14-C14

Crosstalk Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT
Configuration: GAAVVG:

DP 2	Near-End	HDAM_B3-C3,	HDAM_D3-E3
	Far-End	HDAM_B3-C3,	HDAF_D3-E3

Configuration: GAAGVVG

DP 1	Near-End	HDAM_B14-C14,	HDAM_E14-F14
	Far-End	HDAM_B14-C14,	HDAF_E14-F14



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

DP 3 Characterization Conditions

Fixture Identity
PCB-100669-TST-13 REV – HDAM DIFF TEST BOARD 2
PCB-100669-TST-03 REV – HDAF DIFF TEST BOARD 2

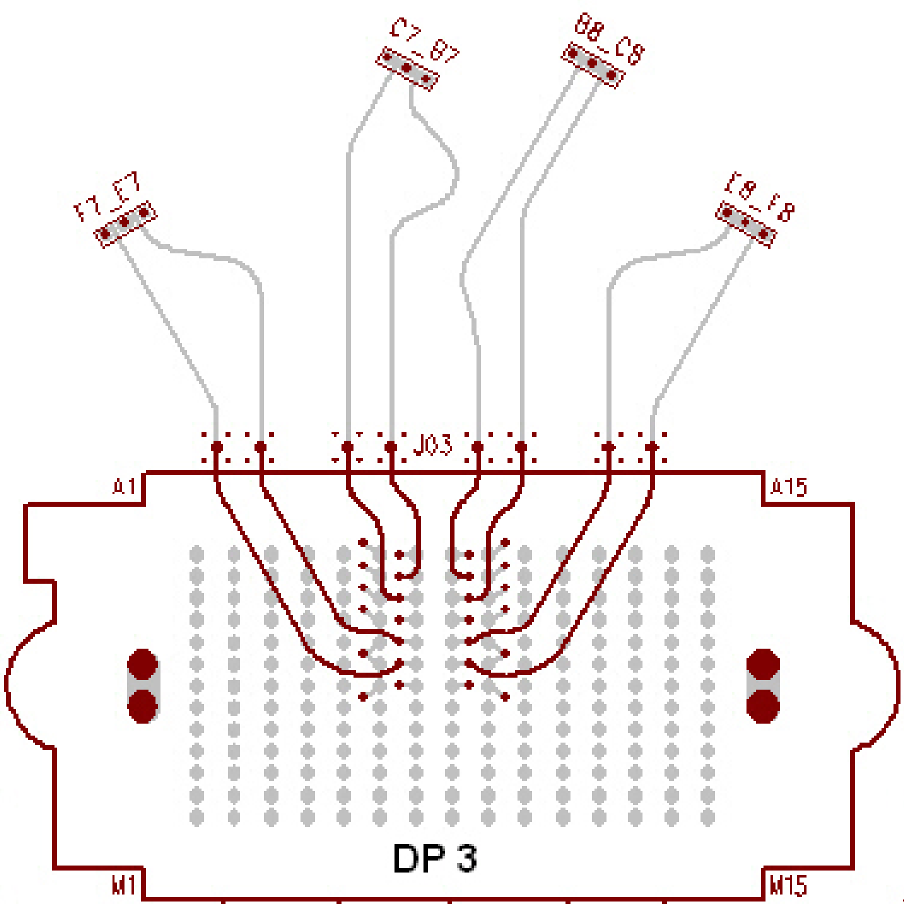
Crosstalk Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT

Configuration: GAAVVG/GAAVVG

DP 3	Near-End	HDAM_E8-F8,	HDAM_E7-F7
	Far-End	HDAM_E8-F8,	HDAF_E7-F7

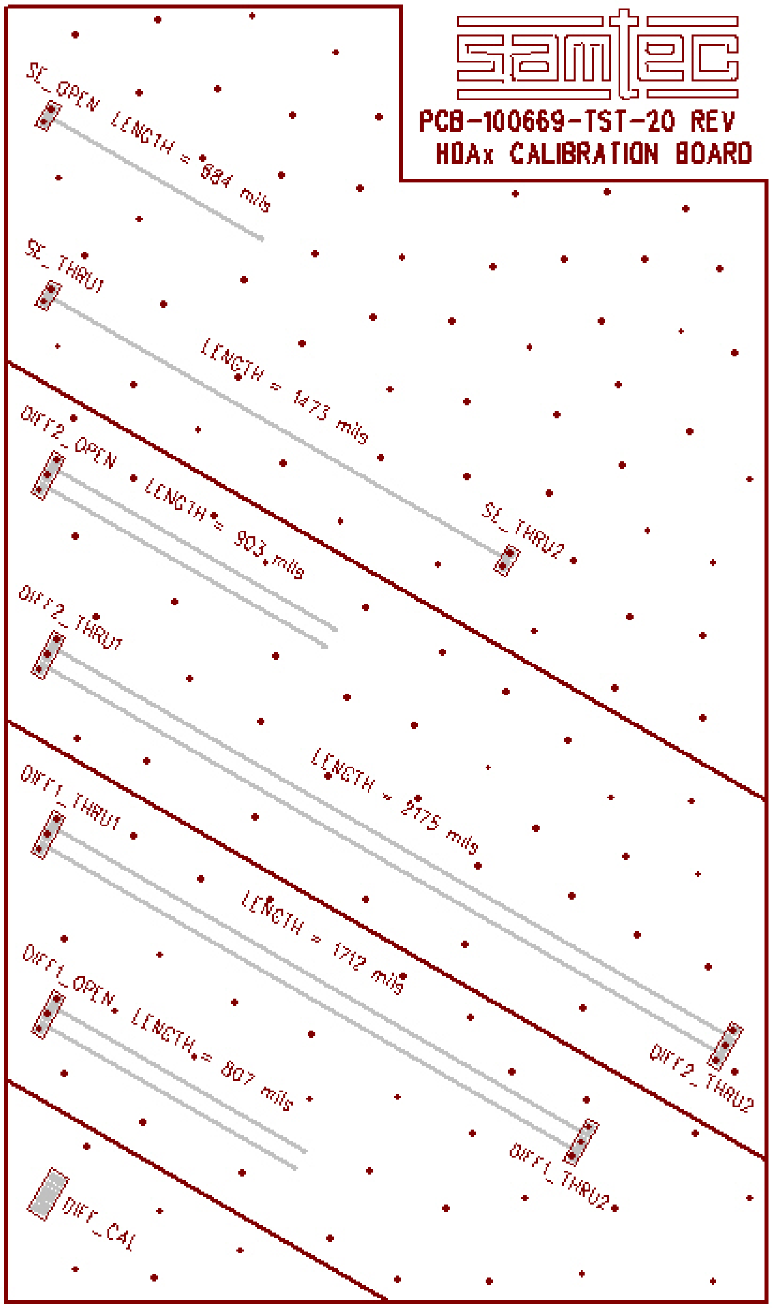
Configuration: GAAGVVG/GAAGVVG

DP 3	Near-End	HDAM_E8-F8,	HDAM_B7-C7
	Far-End	HDAM_E8-F8,	HDAF_B7-C7



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

HDAX Calibration Board Map



Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

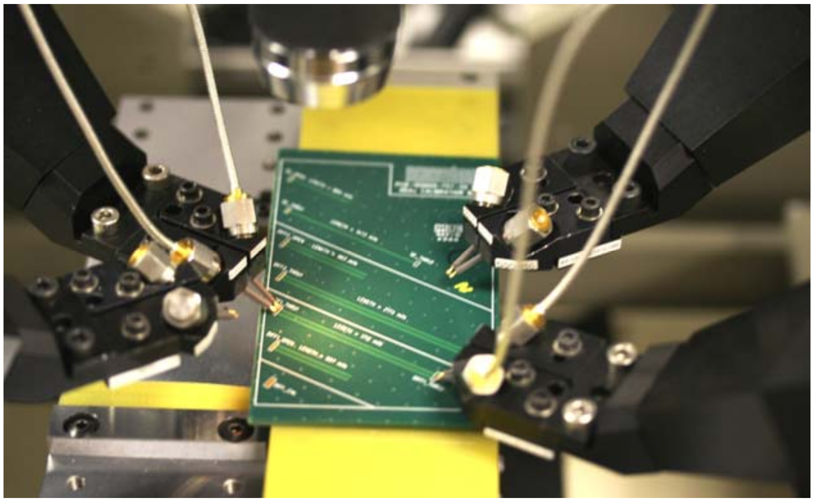
Appendix D – Test and Measurement Setup

The test instrument is the Tektronix CSA8000 Communication Signal Analyzer Mainframe. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. Time domain results are generated using the TDR/Sampling Head capability. S-parameter data is generated from a TDR based software tool called I-Connect Probing is accomplished using a video microscopy system, microprobe positioners, and 40GHz capable probes. The 450 micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a ≥18 dB return loss, and an isolation of 38 dB providing high-bandwidth and low parasitic measurement results. Combined, the above technology provides a stable measurement environment along with the electrical accuracies for obtaining precise calibrations and signal launch capabilities

CSA8000/TDA IConnect Measurements Capability

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Four Position Dual 40 GHz Microprobe Setup



Test Instruments

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
3	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Tektronix 80E03 Dual Channel 20 GHz Sampling Module

Measurement Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
4	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

QTY	Description
4	Pasternack Enterprises 2.9mm Semi-Rigid (.086) 9" Cable Assemblies
2	Tektronix 1 Meter Module Extenders

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Related time and frequency test parameter data recorded for this report were gathered simultaneously.

Sample Preparation

Determine signal launch and monitoring test points by referencing the pin-out maps of interest

Single-ended pinout:	se
Differential parameters:	dp in row
	dp across row
Calibration board	pcb-100669-tst-20

It is a good practice to terminate all non-active signal lines immediately adjacent to the designated active or quiet signal lines under test.

Frequency (S-Parameter) Domain Procedures

Frequency data extraction involves a two step process. The first step determines two SUT time domain waveform relationships utilizing a Tektronix CSA8000 time based instrument. The second step involves the conversion of the time based waveforms into frequency domain response format using the TDA Systems IConnect software tool. TDA Systems labels time related conversion waveforms as the *Step* and *DUT* waveform references. This section establishes the setup procedures for defining the *Step* and *DUT* reference for conversion to frequency s-parameters presented in this report.

CSA8000 Setup

Listed below is the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. These frequency boundaries are determined by the time domain instruments functional settings such as window length, number of points and averaging capability. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process. The single channel pulsed source processes s-parameters in single-ended format. A dual channel differential pulsed source processes s-parameters in differential format.

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss (TDA conversion)

Step Waveform - determine TD waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. The transmission path is completed by inserting a negligible length of transmission standard between the system test probes. Calibration or waveform referencing utilizes 3 pads for each probe touchdown (ie; se thru = 6 pads or diff thru = 12 pads).
Reference cal board, use standard labeled thru_cal.

DUT Waveform - determine waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the transmission THRU_CAL standard and record the measurement.

Return Loss (TDA conversion)

Step Waveform – determine TD waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. Calibration or waveform referencing utilizes 3 pads for each probe touchdown (ie; se reflect = 3 pads or diff reflect = 6 pads).
Reference cal board, use standard labeled thru_cal.

DUT Waveform – determine waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the THRU_CAL reflection standard and record the measurement. In this condition cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Reference se thru, for specified single-ended signal path
Reference diff thru, for specified differential signal path

Near-End Crosstalk (TDA conversion)

Step Waveform – Use Return Loss step waveform.

DUT Waveform - determine waveforms by driving specified signal type and monitoring coupled energy levels at the configurations adjacent near-end signal line(s).

Far-End Crosstalk (TDA conversion)

Step Waveform - Use Insertion Loss step waveform.

DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent far-end signal line(s).

Reference se 1 thru 4 for all single-ended near-end and far-end crosstalk worst or best case configurations.

Reference dp 1 & dp 2 for differential in row near-end and far-end crosstalk worst and best case configurations.

Reference dp 3 for differential across row near-end and far-end crosstalk worst and best case configurations.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Time Domain Procedures

Measurements involving digital type pulses are performed utilizing the Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. For this series of tests, TDR methods are employed for the impedance and propagation delay measurements. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to accurately and fully characterize the SUT.

Impedance(TD)

The signal line(s) of the SUT's signal configuration are energized with a TDR pulse. The far-end of the energized signal lines are terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω termination).

Use specified se thru path for SE impedance profile.
Use specified differential thru path for DIFF impedance profile.

Propagation Delay (TD)

This test reports differential or single ended signal delay as the measured difference of propagation between a combined electrical length of the input/output signal pads and traces (35 ± 5 ps edge rate) and the device under test (DUT) plus a referenced electrical length of the signal pads and signal traces ($PD^{pads/traces}$- $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$). $PD^{pads/traces}$ is the nomenclature representing the electrical length of PCB signal pads & traces equal to physical lengths of PCB pads & traces entering and leaving the device under test (DUT). The PD^{DUT} + $PD^{pads/traces}$ variable is the mated DUT fixture. Both $PD^{pads/traces}$ & $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$ waveform edgerates are measured and recorded at 50 % amplitude of each recorded rising edge. The distance in time between the rising edges is the propagation delay of the device under test (DUT).

Use 1473 mil trace and se thru for single-ended PD measurements.
Use 1712 mil trace and differential thru for differential PD measurements.

Near-End Crosstalk (TD)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the near-end for magnitudes of coupled energy. Adjacent signal lines not undergoing testing are terminated in the test systems characteristic impedance.

Far-End Crosstalk (TD)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the far-end for magnitudes of coupled energy. Adjacent signal lines not undergoing testing are terminated in the test systems characteristic impedance.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Use specified SE 1 & SE 2 configurations for single-ended Worse Case, Best Case, Parallel Across Row and Staggered Across Row near-end and far-end crosstalk measurements.

Use specified DP 1 & DP 2 configurations for differential Worse Case, Best Case, near-end and far-end crosstalk measurements.

Use specified DP 3 crosstalk configurations for differential parallel across row and staggered across row near-end and far-end crosstalk measurements.

Series: HDAM/HDAF Series (HDMezz)
Description: 1.2mm x 2mm grid interconnect system, high density array, 25mm Stack Height

Appendix F – Glossary of Terms

TD – Time Domain
FD – Frequency domain
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
EC6 – Edge Card with a .635mm signal pad pitch
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
LEC6 – Signal Launch Edge Card with a .635 mm signal pad pitch
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
BC – Best Case crosstalk configuration
Z – Impedance (expressed in ohms)