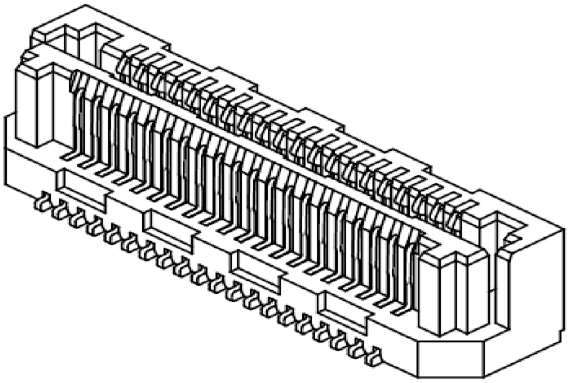
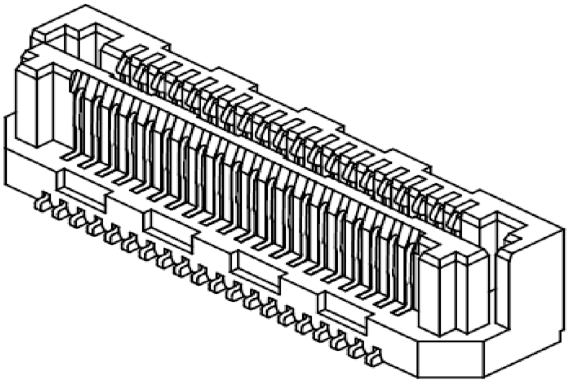
High Speed Characterization Report

LSS-150-02-L-DV-A



Mates with

LSS-150-02-L-DV-A



Description:
Locking Socket & Terminal Strip, 0.635mm Centerline
12MM Stack Height

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 2/21/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Table of Contents

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Connector Overview

Locking Terminal/Socket Strip connectors are hermaphroditic (.0315”) pitch interfaces called the LSS Series and are available in up to 50 contacts per row. LSS Series board-to-board spacing is also available in 6mm (0.2362”), 7mm (0.2756"), 8mm (0.3150"), 9mm (0.3543"), 10mm (0.3937") and 12mm (0.4724") stack heights. The data in this report is applicable only to the 12mm (0.4724") board-to-board spacing.

Connector System Speed Rating

Terminal/Socket LSS Series, 0.635mm (.025”) Centerline, 12mm (0.4724") Board-To-Board Spacing

Signaling	Speed Rating
Single-Ended:	**7.0 GHz / 14 Gbps**
Differential:	**6.5 GHz / 13Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

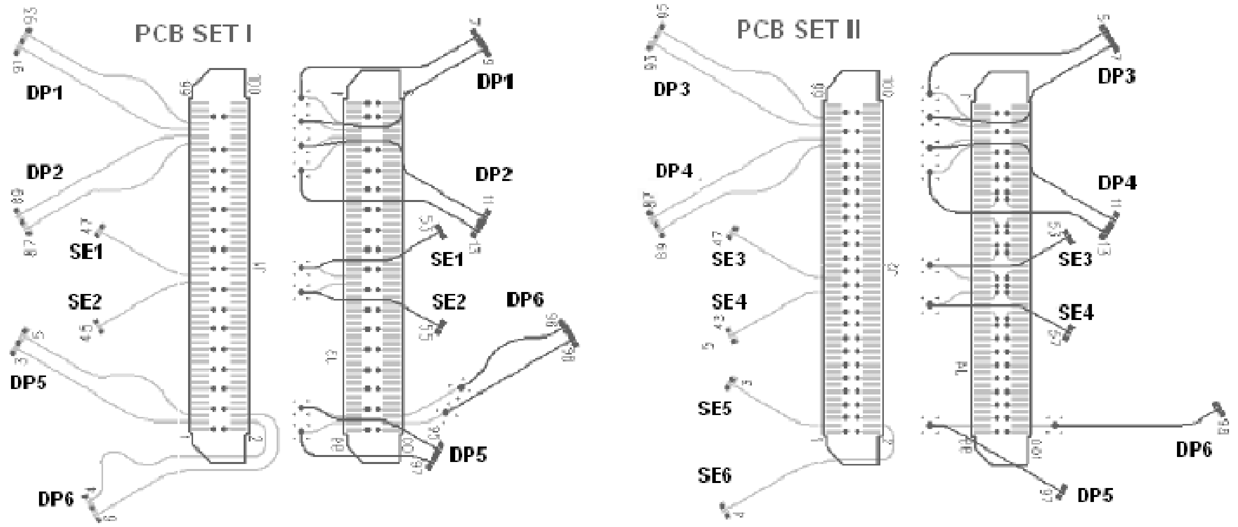
To calculate the Speed Rating, the measured -3 dB point is rounded-up to the nearest half-GHz level. The up rounding corrects for a portion of the test board’s trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

Frequency Domain Data Summary

Table 1 - Single-Ended Signaling System Performance				
Test Parameter	**Drive/Listen**	**Source**	**Victim**	
Insertion Loss	SE3	port 1=LSS_47 port 2=LSS_53	[redacted]	≤ -3dB to 6.9 GHz
Return Loss	SE3	port 1=LSS_47 port 2=LSS_53	[redacted]	≤ -5dB to 6.9 GHz
Near-End Crosstalk	SE2 to SE1	LSS _45	LSS _47	≤ -15dB to 6.9 GHz
	SE4 to SE3	LSS _43	LSS _47	≤ -25dB to 6.9 GHz
	SE6 to SE5	LSS _4	LSS _3	≤ -15dB to 6.9 GHz
Far-End Crosstalk	SE2 to SE1	LSS _45	LSS _53	≤ -20dB to 6.9 GHz
	SE4 to SE3	LSS _43	LSS _53	≤ -32dB to 6.9 GHz
	SE6 to SE5	LSS _4	LSS _97	≤ -3dB to 6.9 GHz

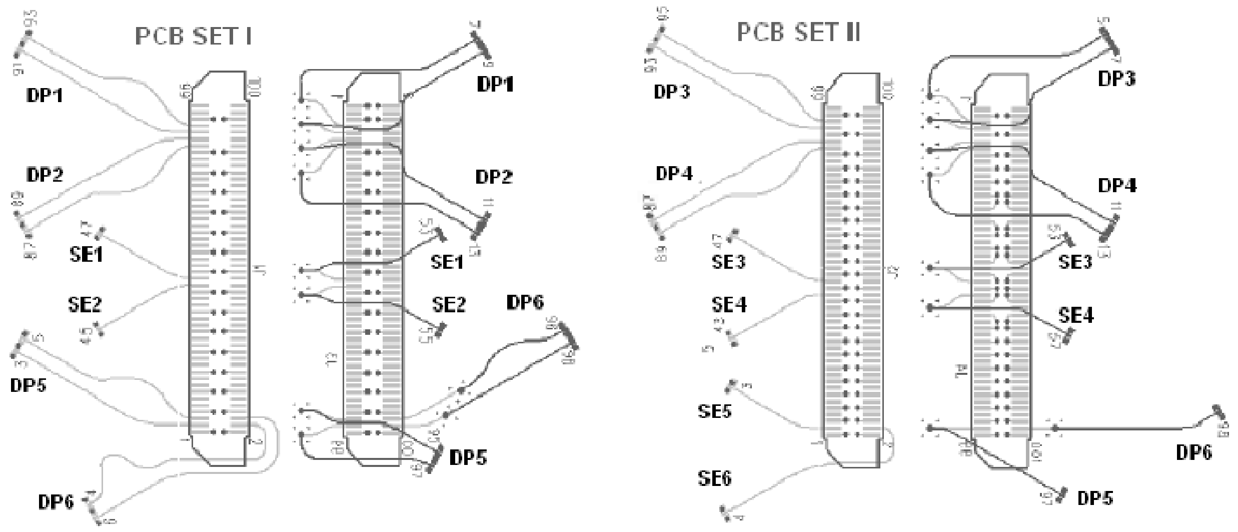
Pin Map (reference Appendix C for full description of test boards)



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

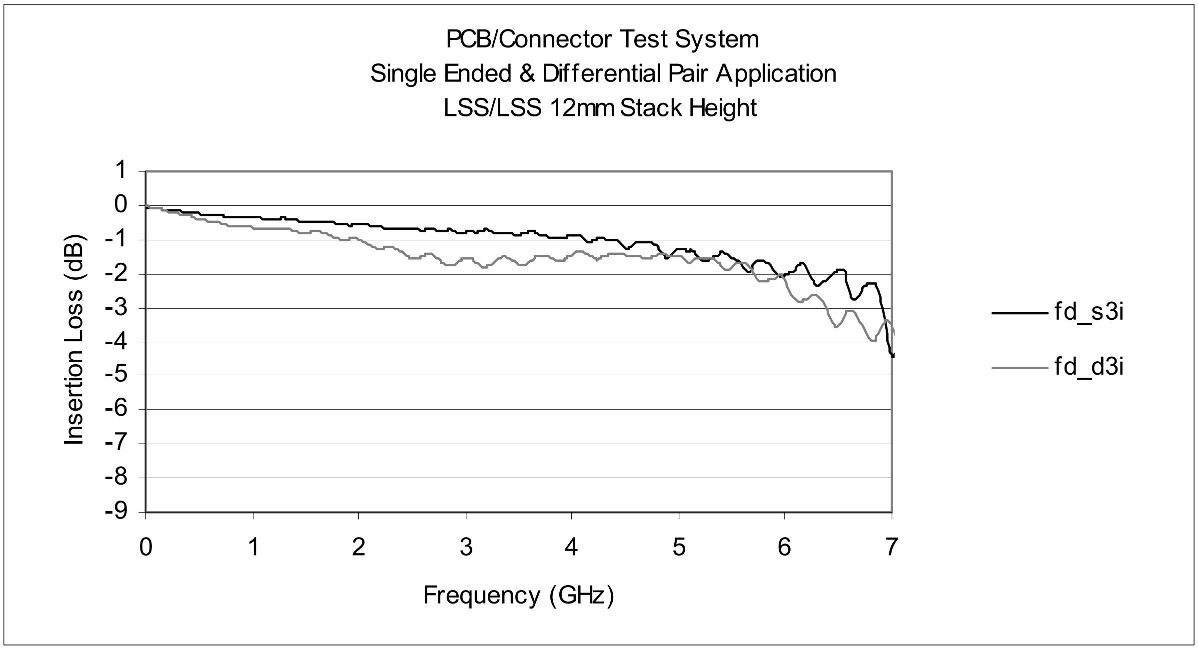
Table 2 - Differential Signaling System Performance				
Test Parameter	**Signal Line(s)**	**Source**	**Victim**	
Insertion Loss	DP3	port 1=LSS_93-95 port 2=LSS_5-7	[redacted]	-3dB @ 6.4 GHz
Return Loss	DP3	port 1=LSS_93-95 port 2=LSS_5-7	[redacted]	≤ -3dB to 6.4 GHz
Near-End Crosstalk	DP2 to DP1	LSS _87-89	LSS _91-93	≤ -18dB to 6.4 GHz
	DP4 to DP3	LSS _87-89	LSS _93-95	≤ -32dB to 6.4 GHz
	DP6 to DP5	LSS _4-6	LSS _3-5	≤ -35dB to 6.4 GHz
Far-End Crosstalk	DP2 to DP1	LSS _87-89	LSS _7-9	≤ -25dB to 6.4 GHz
	DP4 to DP3	LSS _87-89	LSS _5-7	≤ -32dB to 6.4 GHz
	DP6 to DP5	LSS _4-6	LSS _95-97	≤ -35dB to 6.4 GHz

Pin Map (reference Appendix C for full description of test boards)



Bandwidth Chart – Single-Ended & Differential Insertion Loss

Locking Terminal/Socket Strip Connector



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω) – SE3, Signal Line 47-53

Signal Risetime	35±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	57.1	52.3	52.0	51.2	51.1	50.8	50.7
Minimum Impedance	39.8	42.7	45.2	47.9	49.2	49.8	50.1

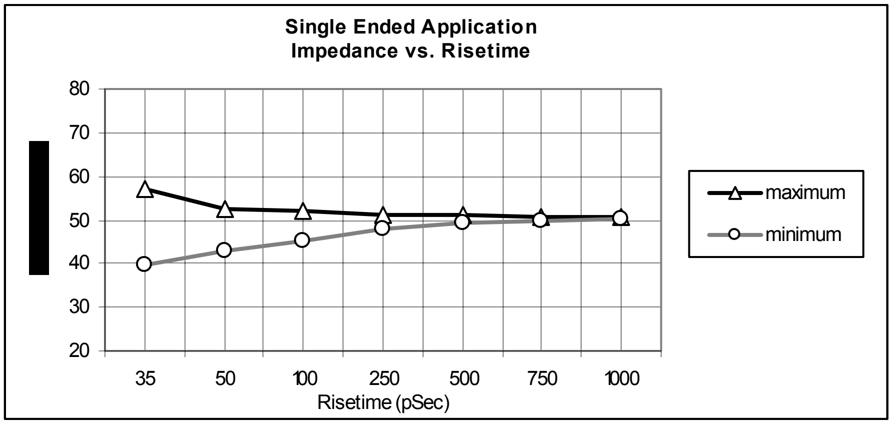


Table 4 - Differential Impedance (Ω) – DP3, Signal Pair 93-95, 5-7

Signal Risetime	35±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	103.1	102.9	100.9	100.4	100.2	100.0	99.9
Minimum Impedance	63.8	67.5	73.4	81.4	88.2	91.3	93.2

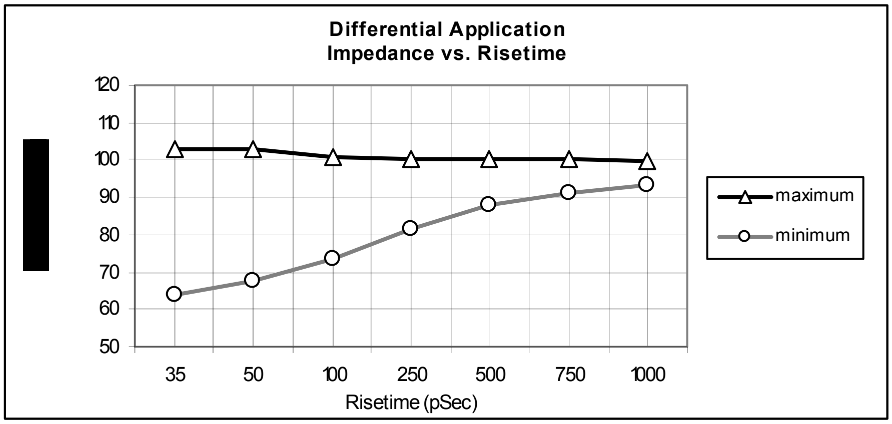
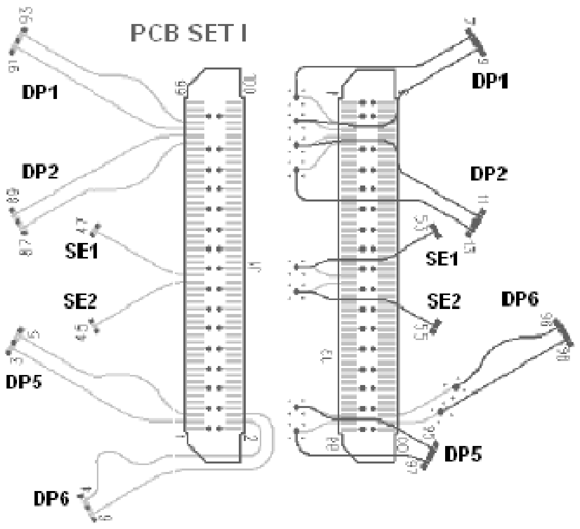
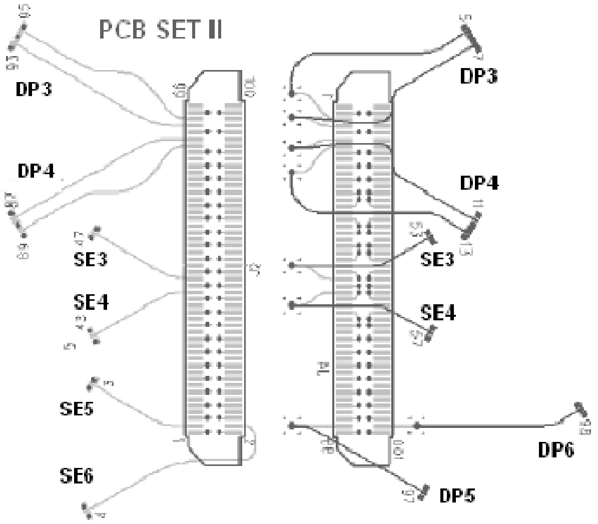


Table 5 - Single-Ended Crosstalk (%)

Input (t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	SE2 to SE1	LSS _45	LSS _47	19.4	17.8	16.6	10.3	6.0	4.2	3.3
	SE4 to SE3	LSS _43	LSS _47	3.3	2.4	1.9	1.2	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _3	1.8	1.6	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	SE2 to SE1	LSS _45	LSS _53	6.3	3.9	2.6	1.2	< 1.0%	< 1.0%	< 1.0%
	SE4 to SE3	LSS _43	LSS _53	4.0	2.3	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _97	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)





Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

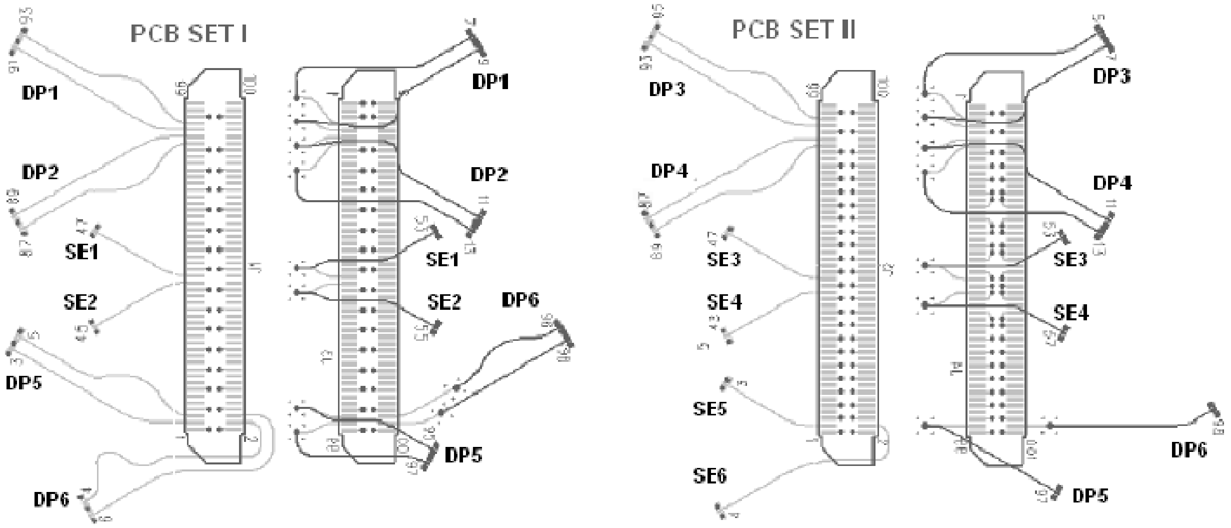
Table 6 - Differential Crosstalk (%)

Input(t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	DP2 to DP1	LSS 87-89	LSS 91-93	5.9	5.4	5.1	3.5	2.1	1.5	1.2
	DP4 to DP3	LSS 87-89	LSS 93-95	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DP2 to DP1	LSS 87-89	LSS 7-9	1.9	1.5	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 5-7	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 95-97	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay

Configuration		Signal Path	(Mated Connector Only)
Single-Ended	SE3	LSS; 47 thru LSS; 53	81ps
Differential	DP3	LSS; 93-95 thru LSS; 5-7	78ps

Pin Map (reference Appendix C for full description of test boards)



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. However, other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors’ true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as “ground”. In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others; connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

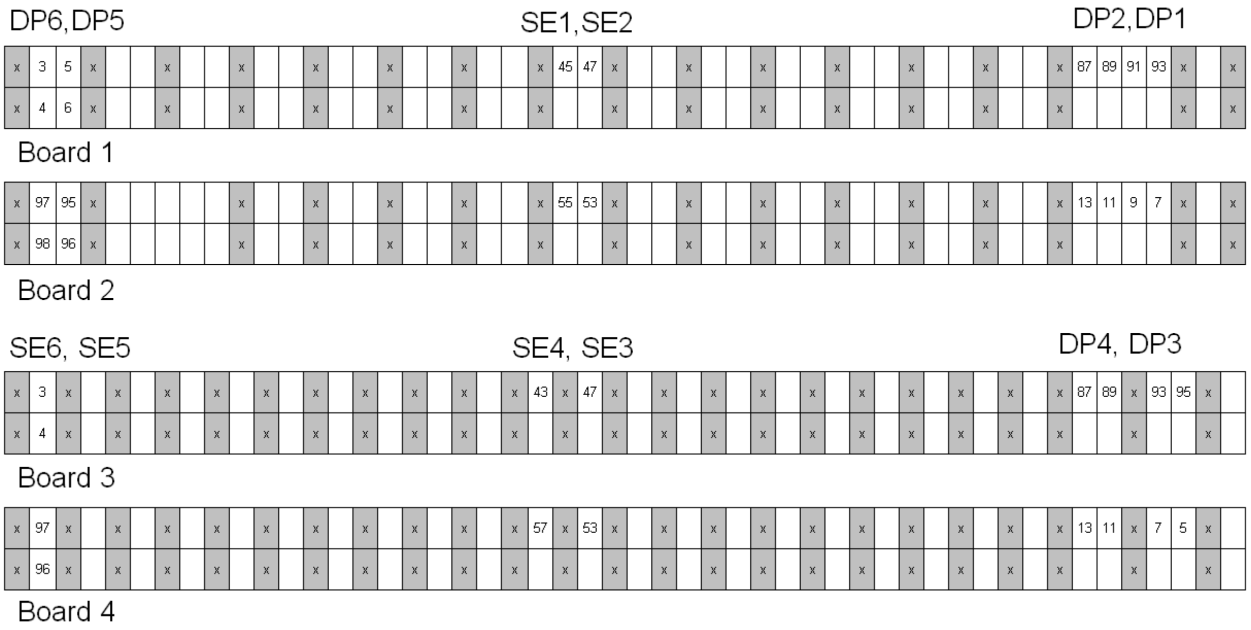
In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So, care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

For this connector, the following array configurations are evaluated:

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

☐ open pin field X grounded pin field

P# signal aggressor or signal victim pins



Single-Ended Impedance:
- Well-referenced line (reference SE2, 1:1),

Single-Ended Crosstalk:
- Well-referenced line; mimics 1:1 S:G ratio (reference SE2, 1:1),
- 2:1 S:G ratio (reference SE1),

Only one single-ended signal was driven for crosstalk measurements.

Differential Impedance:
- Well-referenced line (reference DP2, 1:1)

Differential Crosstalk:
- Well-referenced line; mimics 1:1 S:G ratio (reference DP1)
- Higher Signal Density (reference DP3)
- Full-Row Differential (reference DP1)

Only one differential pair was driven for crosstalk measurements.

*In all cases where a center ground blade is present in the connector it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals, might be encountered, as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect, can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 35 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system’s signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT’s frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 35 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 35 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

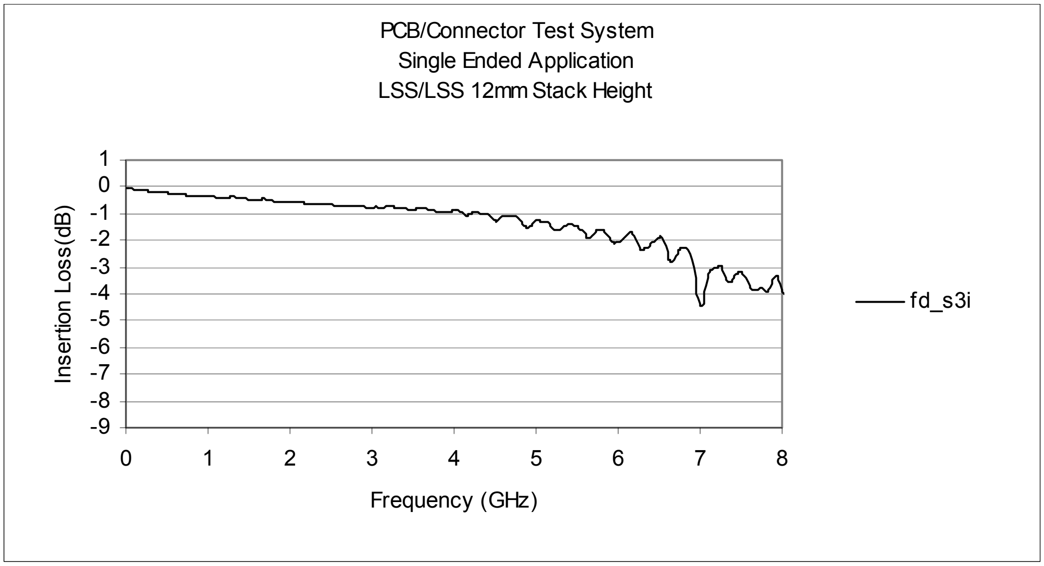
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Appendix A – Frequency Domain Response Graphs

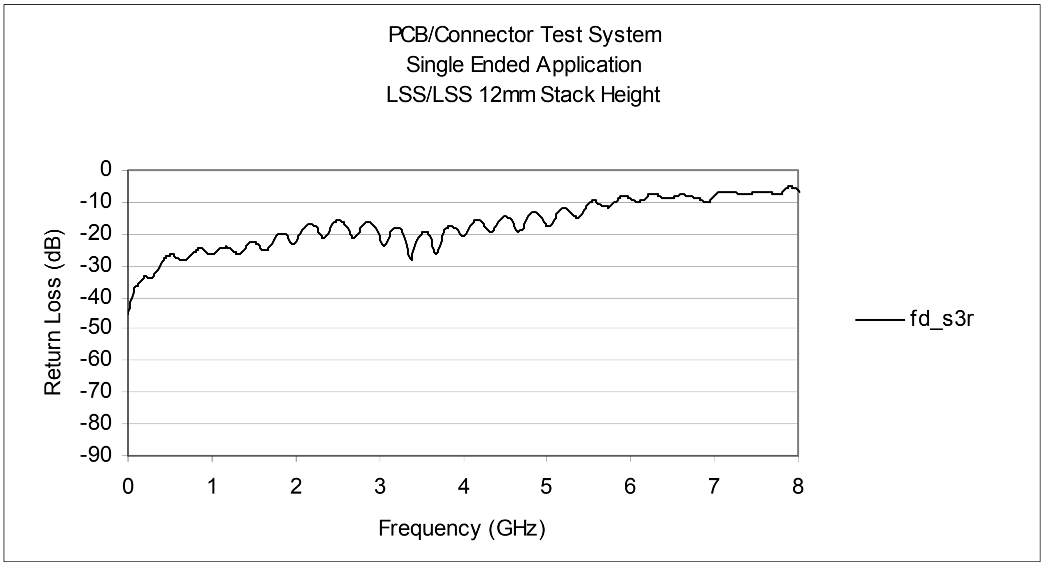
Single-Ended Application – Insertion Loss

Configuration: port 1=LSS_43 port 2=LSS_57



Single-Ended Application – Return Loss

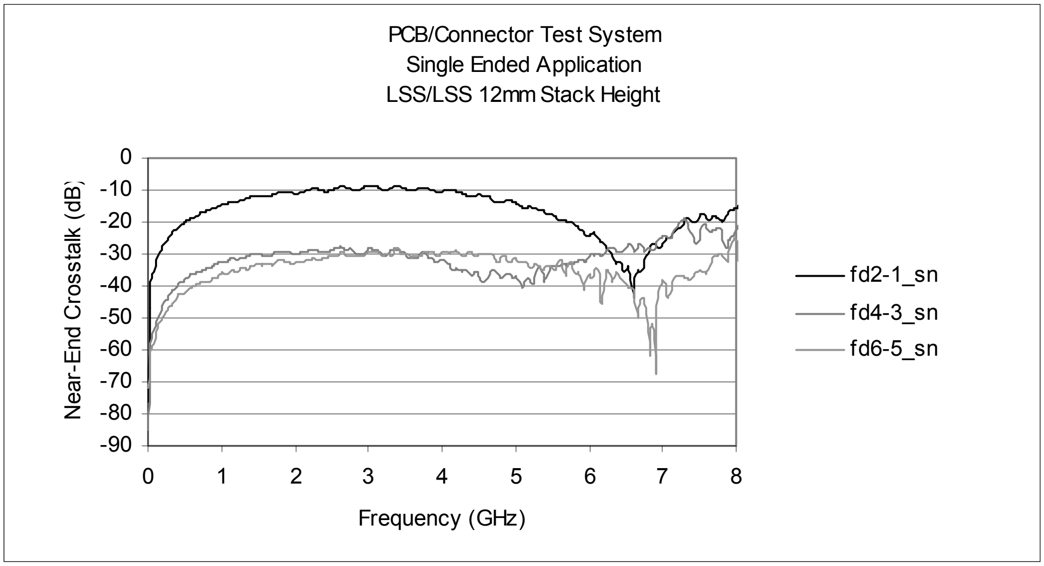
Configuration: port 1=LSS_43 port 2=LSS_57



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

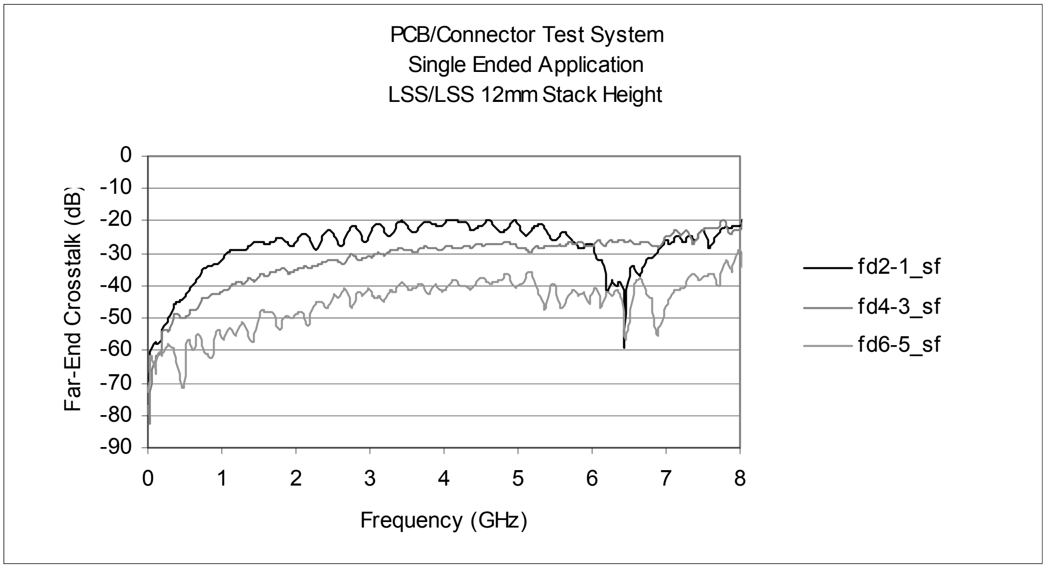
Single-Ended Application – NEXT Configurations

SE2 TO SE1, LSS _45, LSS _47
SE4 TO SE3, LSS _43, LSS _47
SE6 TO SE5, LSS _4, LSS _3



Single-Ended Application – FEXT Configurations

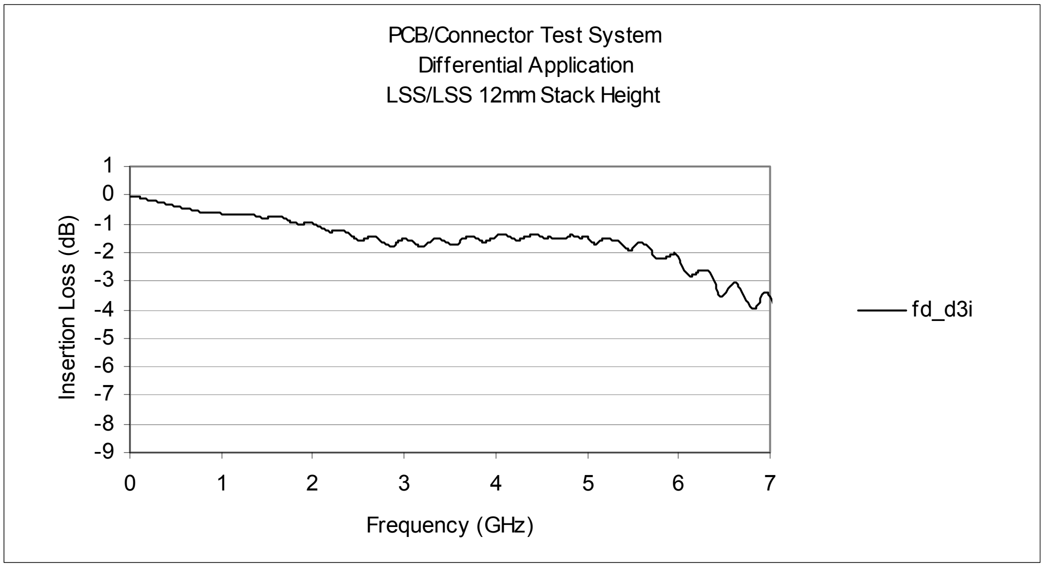
SE2 TO SE1, LSS _45, LSS _53
SE4 TO SE3, LSS _43, LSS _53
SE6 TO SE5, LSS _4, LSS _97



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

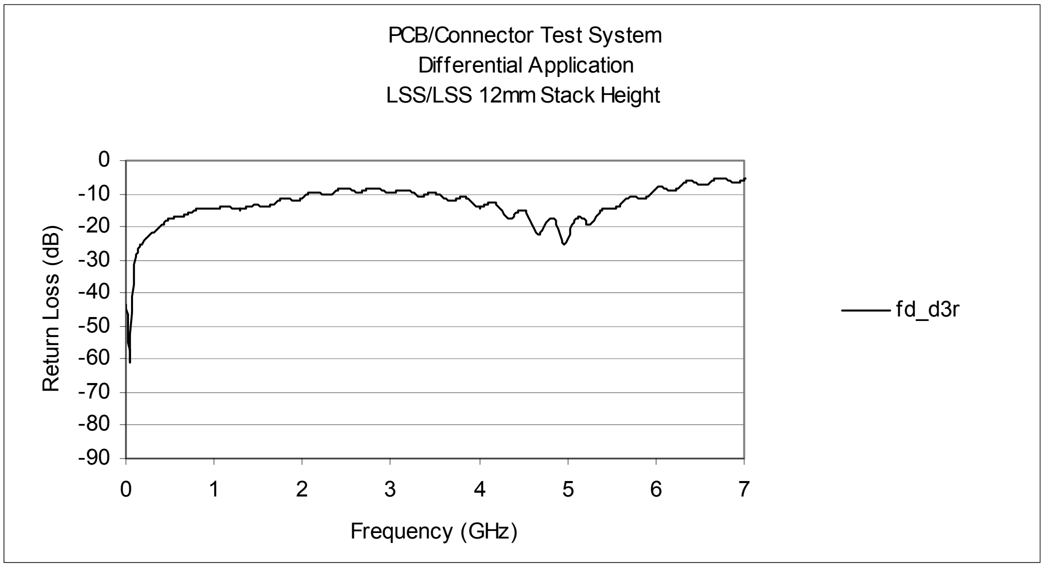
Differential Application – Insertion Loss

Configuration: port 1=LSS_87-89 port 2=LSS_11-13



Differential Application – Return Loss

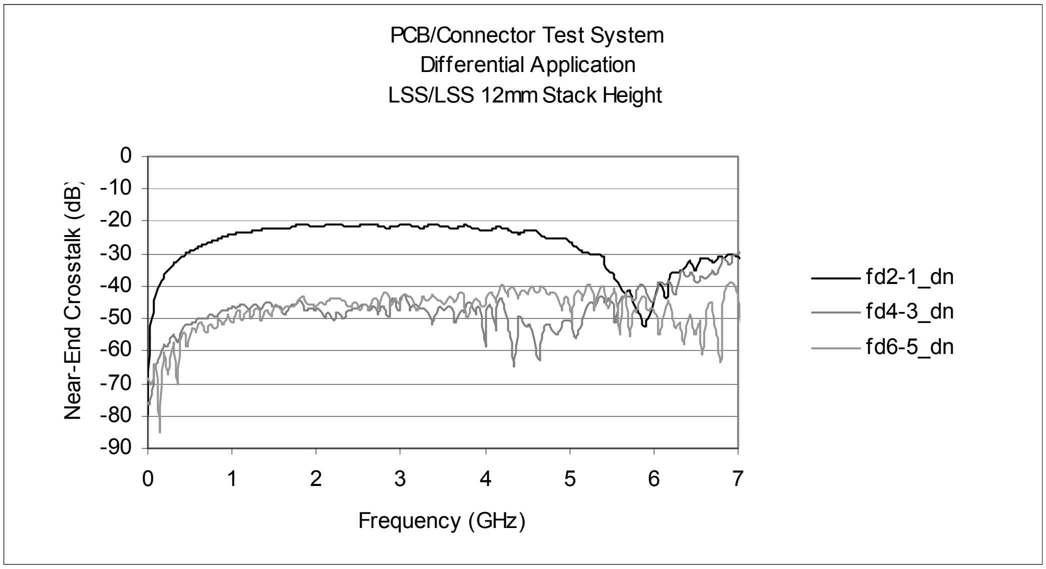
Configuration: port 1=LSS_87-89 port 2=LSS_11-13



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

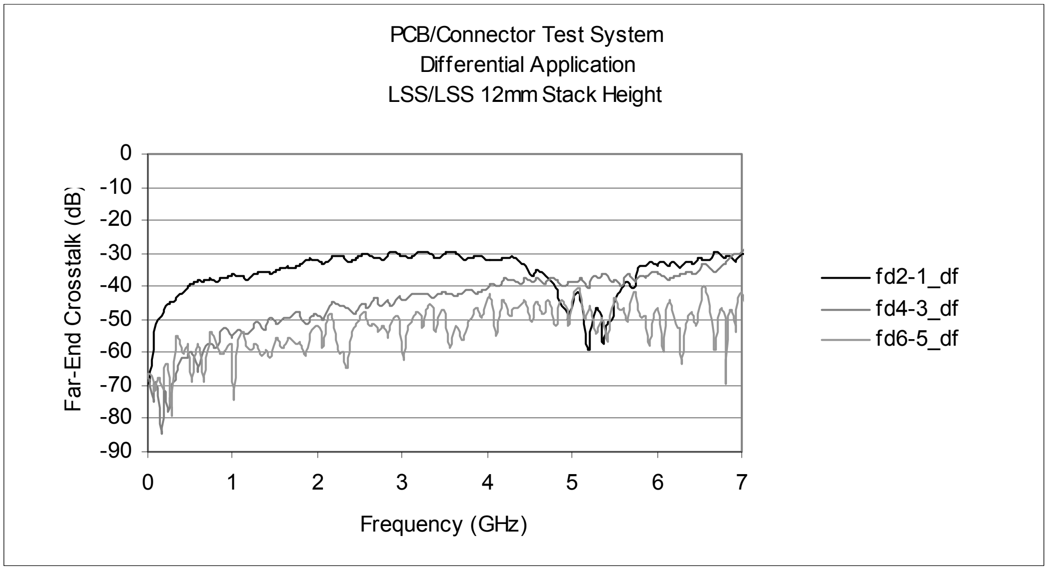
Differential Application – NEXT Configurations

DP2 to DP1, LSS _87-89, LSS _91-93
DP4 to DP3, LSS _87-89, LSS _93-95
DP6 to DP5, LSS _4-6, LSS _3-5



Differential Application – FEXT Configurations

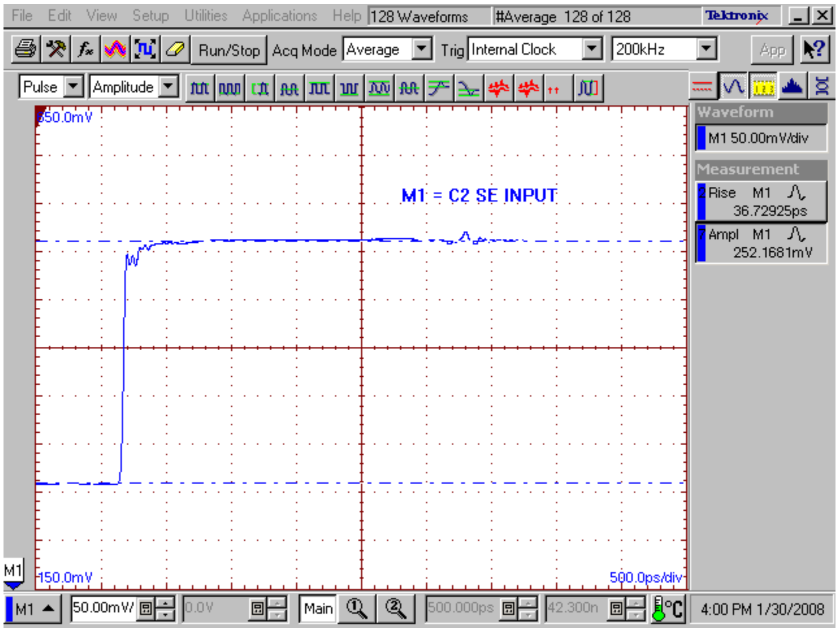
DP2 to DP1, LSS _87-89, LSS _7-9
DP4 to DP3, LSS _87-89, LSS _5-7
DP6 to DP5, LSS _4-6, LSS _95-97



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse

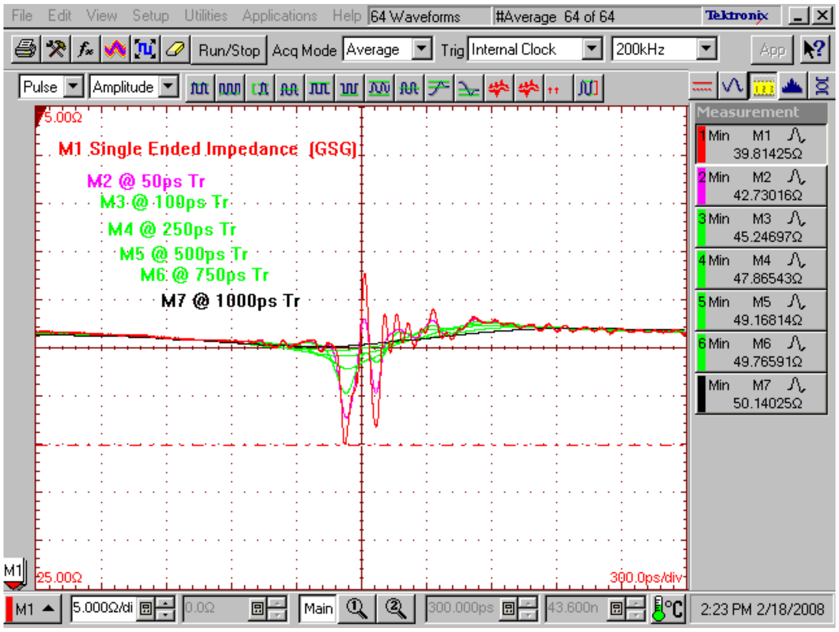


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
200kHz
M1 = C2 SE INPUT
M1 50.00mV/div
Rise M1 36.72925ps
Ampl M1 252.1681mV
M1 50.00mV
0.0V
4:00 PM 1/30/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Single-Ended Application – Impedance

Configuration: port 1=LSS_43 port 2=LSS_57



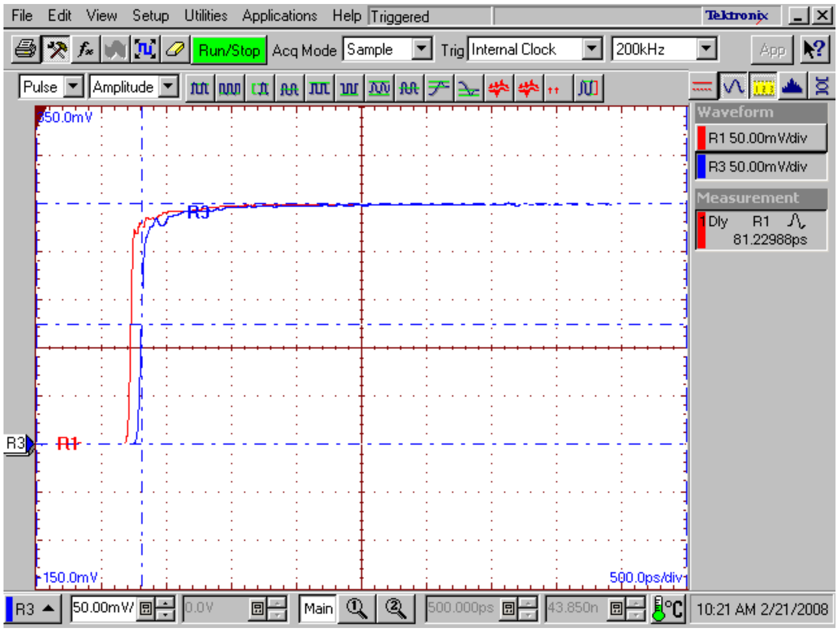
64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz

Min M1 39.81425Ω
Min M2 42.73016Ω
Min M3 45.24697Ω
Min M4 47.86543Ω
Min M5 49.16814Ω
Min M6 49.76591Ω
Min M7 50.14025Ω

M1 5.000Ω/di
2:23 PM 2/18/2008

Single-Ended Application – Propagation Delay

Configuration: port 1=LSS_43 port 2=LSS_57



Triggered
Acq Mode Sample
Trig Internal Clock
200kHz

R1 50.00mV/div
R3 50.00mV/div

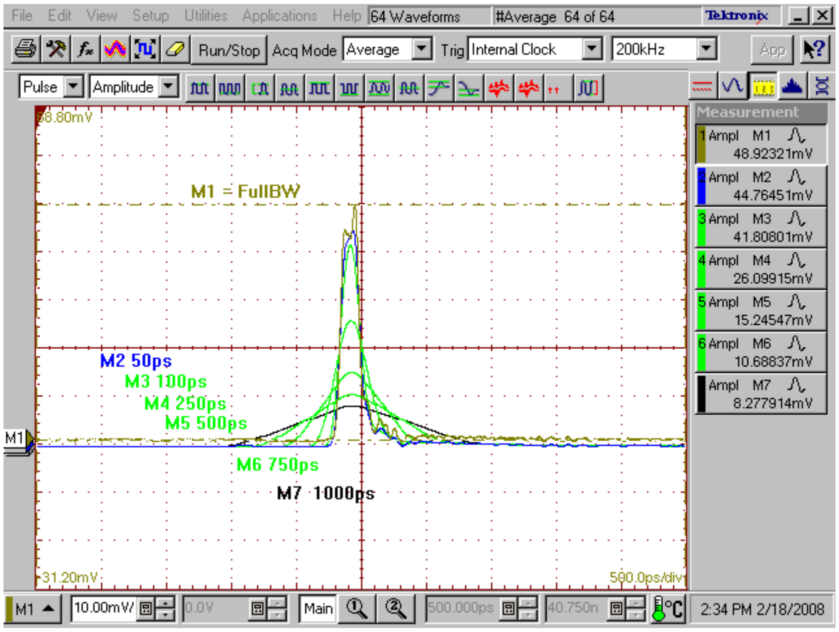
Dly R1 81.22988ps

R3 50.00mV/
10:21 AM 2/21/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Single-Ended Application – NEXT, “SE2 to SE1”

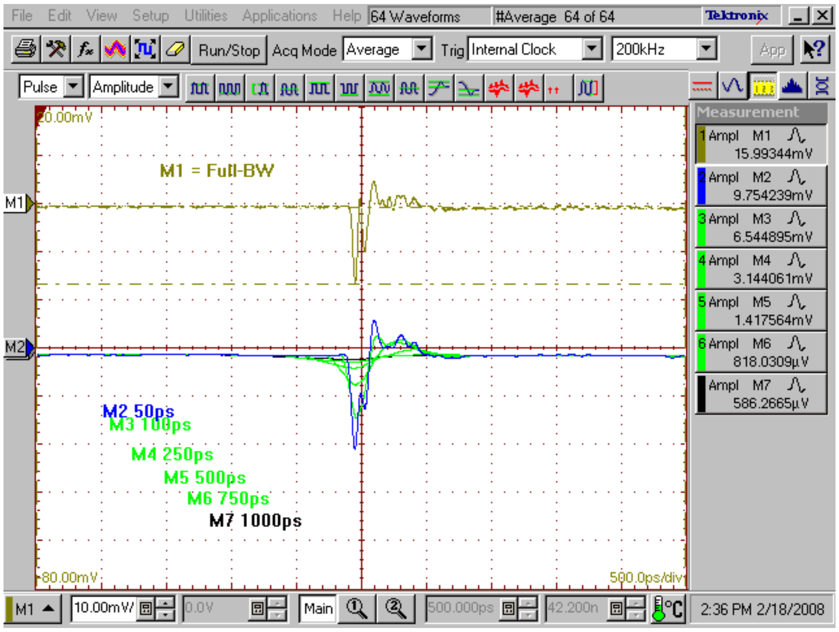
Configuration: (port3 = LSS; 45, Port1 = LSS; 47)



Measurement
1 Ampl M1 48.92321mV
2 Ampl M2 44.76451mV
3 Ampl M3 41.80801mV
4 Ampl M4 26.09915mV
5 Ampl M5 15.24547mV
6 Ampl M6 10.68837mV
7 Ampl M7 8.277914mV

Single-Ended Application – FEXT, “SE2 to SE1”

Configuration: (port3 = LSS; 45, Port2 = LSS; 53)

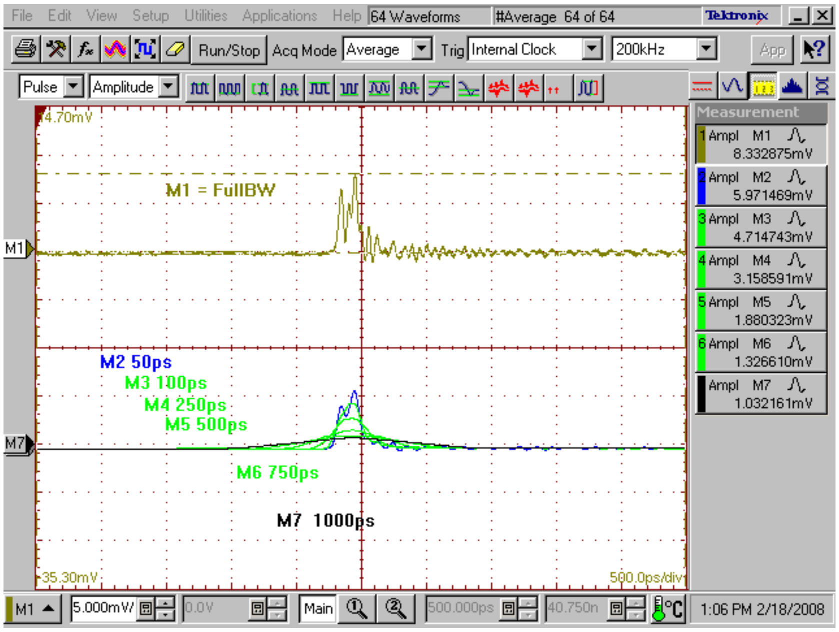


Measurement
1 Ampl M1 15.99344mV
2 Ampl M2 9.754239mV
3 Ampl M3 6.544895mV
4 Ampl M4 3.144061mV
5 Ampl M5 1.417564mV
6 Ampl M6 818.0309µV
7 Ampl M7 586.2665µV

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Single-Ended Application – NEXT, “SE4 to SE3”

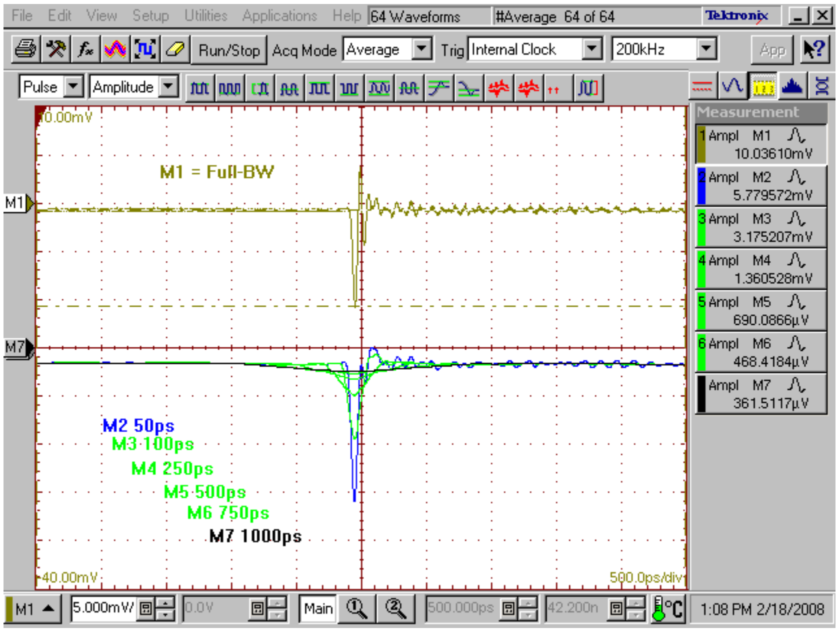
Configuration: (port3 = LSS; 43, Port1 = LSS; 47)



64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz
Ampl M1 8.332875mV
Ampl M2 5.971469mV
Ampl M3 4.714743mV
Ampl M4 3.158591mV
Ampl M5 1.880323mV
Ampl M6 1.326610mV
Ampl M7 1.032161mV
M1 5.000mV/ 0.0V 500.000ps 40.750n
1:06 PM 2/18/2008

Single-Ended Application – FEXT, “SE4 to SE3”

Configuration: (port3 = LSS; 43, Port2 = LSS; 53)

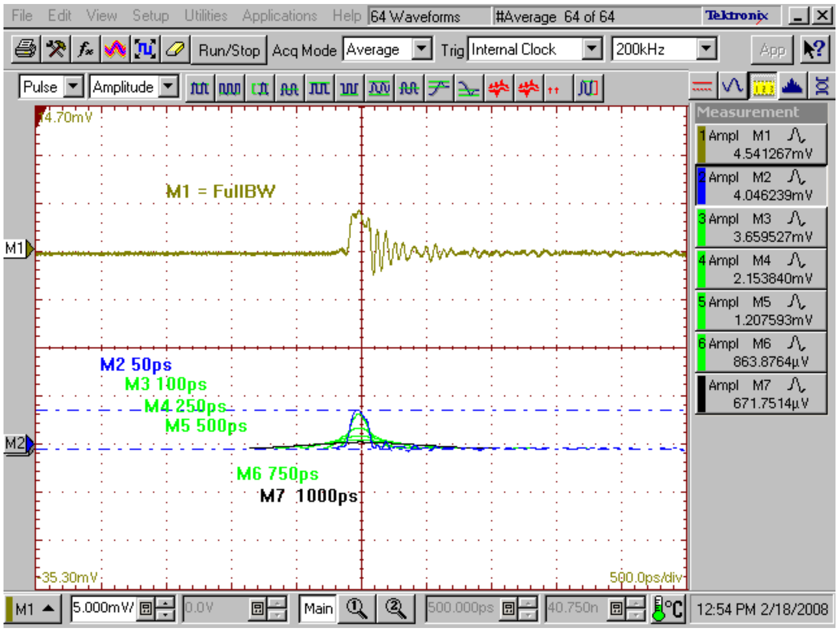


64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz
Ampl M1 10.03610mV
Ampl M2 5.779572mV
Ampl M3 3.175207mV
Ampl M4 1.360528mV
Ampl M5 690.0866µV
Ampl M6 468.4184µV
Ampl M7 361.5117µV
M1 5.000mV/ 0.0V 500.000ps 42.200n
1:08 PM 2/18/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Single-Ended Application – NEXT, “SE6 to SE5”

Configuration: (port3 = LSS; 4, Port1 = LSS; 3)



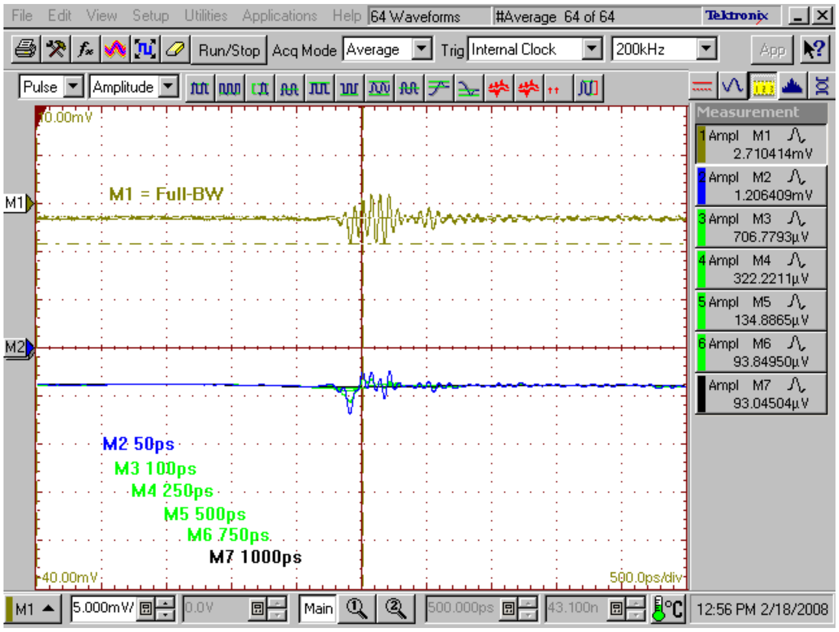
64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz

Measurement
1 Ampl M1 4.541267mV
2 Ampl M2 4.046239mV
3 Ampl M3 3.659527mV
4 Ampl M4 2.153840mV
5 Ampl M5 1.207593mV
6 Ampl M6 863.8764µV
Ampl M7 671.7514µV

5.000mV/ 0.0V 500.000ps 40.750n
12:54 PM 2/18/2008

Single-Ended Application – FEXT, “SE6 to SE5”

Configuration: (port3 = LSS; 4, Port2 = LSS; 97)

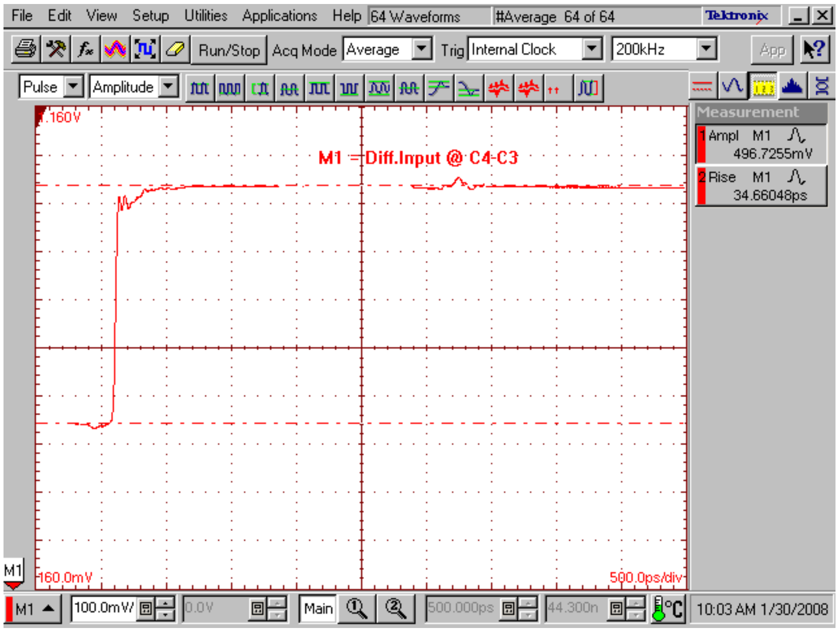


64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz

Measurement
1 Ampl M1 2.710414mV
2 Ampl M2 1.206409mV
3 Ampl M3 706.7793µV
4 Ampl M4 322.2211µV
5 Ampl M5 134.8865µV
6 Ampl M6 93.84950µV
Ampl M7 93.04504µV

5.000mV/ 0.0V 500.000ps 43.100n
12:56 PM 2/18/2008

Differential Application – Input Pulse



64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz

M1 = Diff.Input @ C4-C3

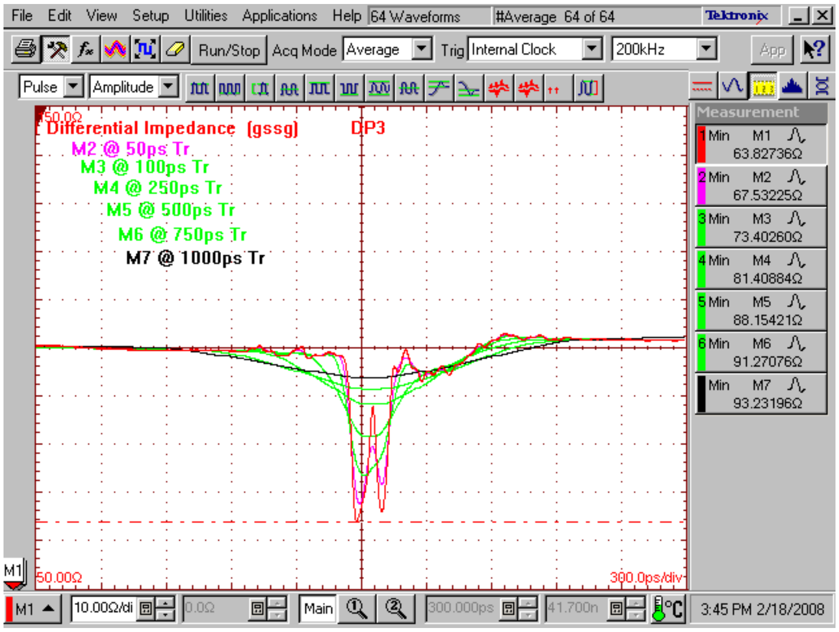
Ampl M1 496.7255mV
Rise M1 34.66048ps

M1 100.0mV/
0.0V
500.000ps
44.300n
10:03 AM 1/30/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Differential Application – Impedance

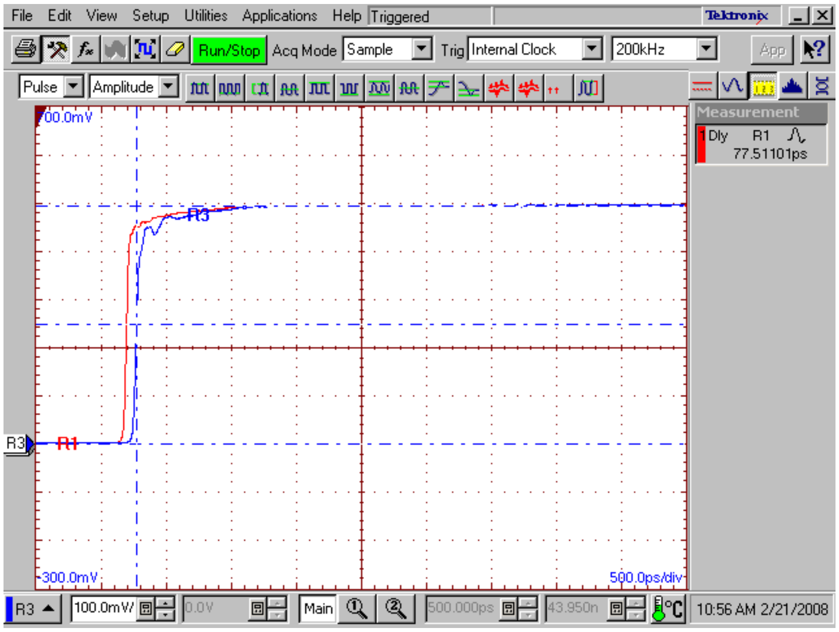
Configuration: port 1=LSS_93-95 port 2=LSS_5-7



Measurement
Min M1 63.82736Ω
Min M2 67.53225Ω
Min M3 73.40260Ω
Min M4 81.40884Ω
Min M5 88.15421Ω
Min M6 91.27076Ω
Min M7 93.23196Ω

Differential Application – Propagation Delay

Configuration: port 1=LSS_93-95 port 2=LSS_5-7

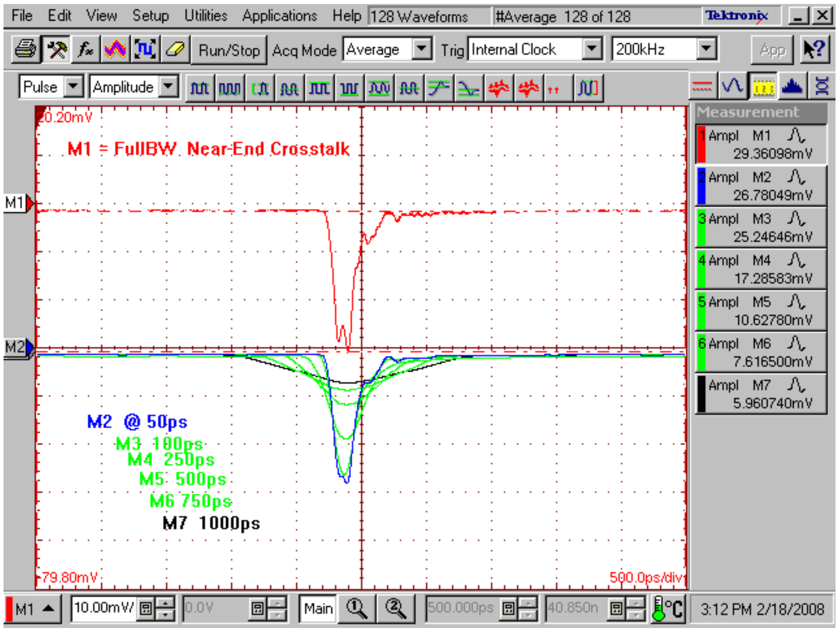


Measurement
Dly R1 77.51101ps

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Differential Application – NEXT, “DP2 to DP1”

Configuration: (port3 = LSS; 87-89, Port1 = LSS; 91-93)



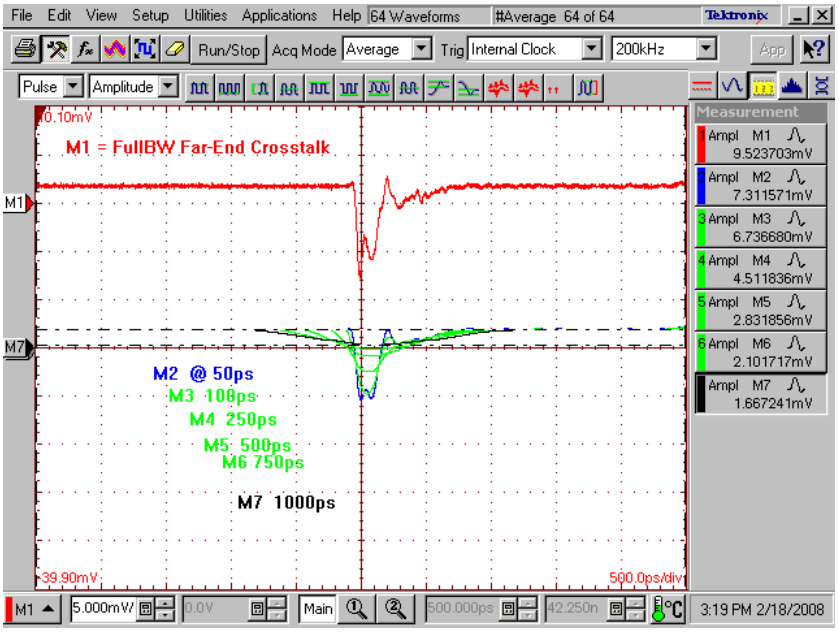
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
200kHz

Measurement
Ampl M1 29.36098mV
Ampl M2 26.78049mV
Ampl M3 25.24646mV
Ampl M4 17.28583mV
Ampl M5 10.62780mV
Ampl M6 7.616500mV
Ampl M7 5.960740mV

M1 10.00mV/ 0.0V 500.000ps 40.850n
3:12 PM 2/18/2008

Differential Application – FEXT, “DP2 to DP1”

Configuration: (port3 = LSS; 87-89, Port2 = LSS; 7-9)



64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz

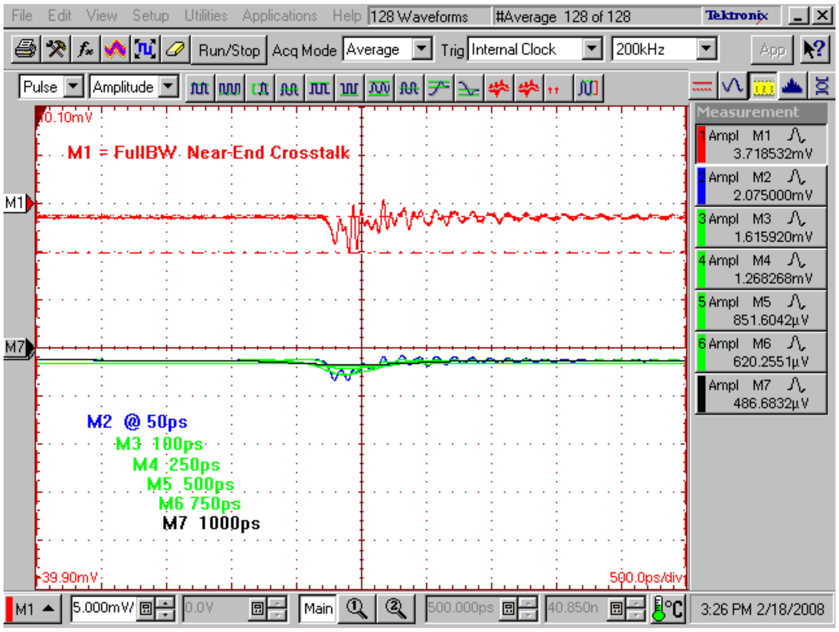
Measurement
Ampl M1 9.523703mV
Ampl M2 7.311571mV
Ampl M3 6.736680mV
Ampl M4 4.511836mV
Ampl M5 2.831856mV
Ampl M6 2.101717mV
Ampl M7 1.667241mV

M1 5.000mV/ 0.0V 500.000ps 42.250n
3:19 PM 2/18/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

Differential Application – NEXT, "DP4 to DP3"

Configuration: (port3 = LSS; 87-89, Port1 = LSS; 93-95)



128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
200kHz
Pulse
Amplitude

M1 = FullBW Near-End Crosstalk
M2 @ 50ps
M3 100ps
M4 250ps
M5 500ps
M6 750ps
M7 1000ps

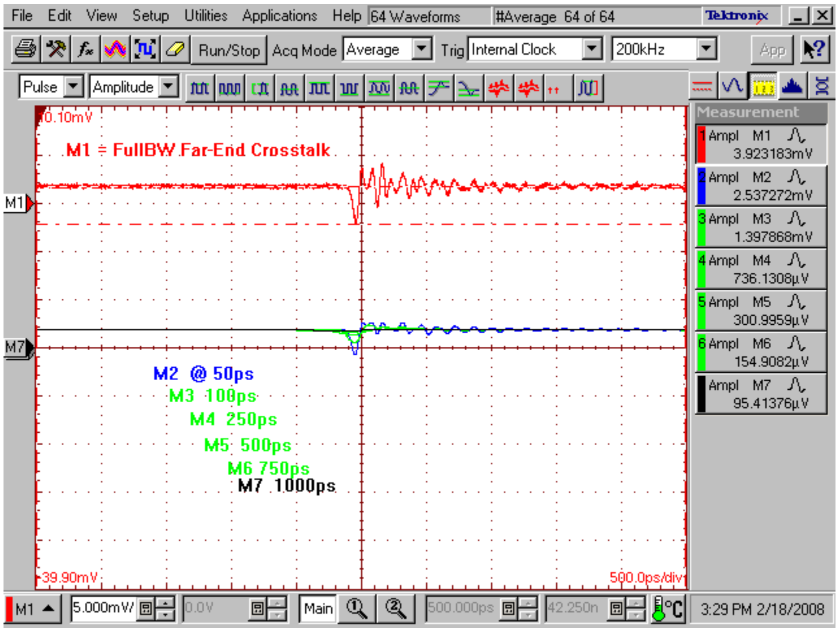
10.10mV
-39.90mV
500.0ps/div

1 Ampl M1 3.718532mV
2 Ampl M2 2.075000mV
3 Ampl M3 1.615920mV
4 Ampl M4 1.268268mV
5 Ampl M5 851.6042µV
6 Ampl M6 620.2551µV
7 Ampl M7 486.6832µV

M1 5.000mV/ 0.0V
500.000ps 40.850n
3:26 PM 2/18/2008

Differential Application – FEXT, "DP4 to DP3"

Configuration: (port3 = LSS; 87-89, Port2 = LSS; 5-7)



64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz
Pulse
Amplitude

M1 = FullBW Far-End Crosstalk
M2 @ 50ps
M3 100ps
M4 250ps
M5 500ps
M6 750ps
M7 1000ps

10.10mV
-39.90mV
500.0ps/div

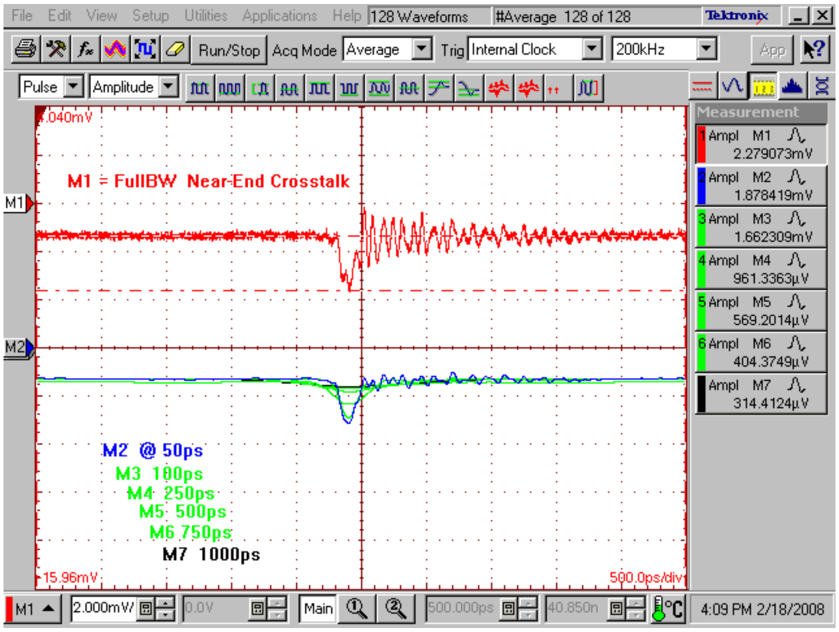
1 Ampl M1 3.923183mV
2 Ampl M2 2.537272mV
3 Ampl M3 1.397868mV
4 Ampl M4 736.1308µV
5 Ampl M5 300.9959µV
6 Ampl M6 154.9082µV
7 Ampl M7 95.41376µV

M1 5.000mV/ 0.0V
500.000ps 42.250n
3:29 PM 2/18/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Differential Application – NEXT, “DP6 to DP5”

Configuration: (port3 = LSS; 4-6, Port1 = LSS; 3-5)



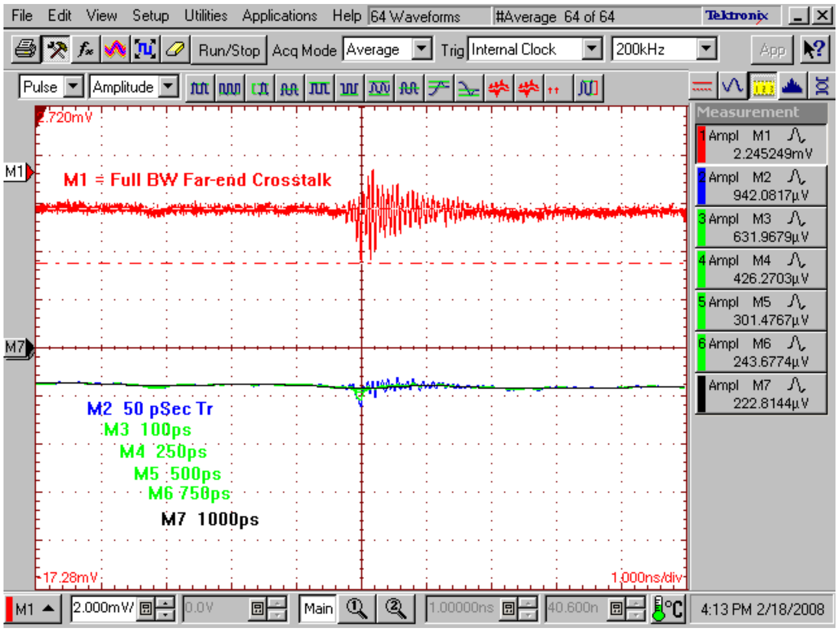
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
200kHz
Amplitude

Ampl M1 2.279073mV
Ampl M2 1.878419mV
Ampl M3 1.662309mV
Ampl M4 961.3363µV
Ampl M5 569.2014µV
Ampl M6 404.3749µV
Ampl M7 314.4124µV

M1 2.000mV/ 0.0V 500.000ps 40.850n
4:09 PM 2/18/2008

Differential Application – FEXT, “DP6 to DP5”

Configuration: (port3 = LSS; 4-6, Port2 = LSS; 95-97)



64 Waveforms
#Average 64 of 64
Acq Mode Average
Trig Internal Clock
200kHz
Amplitude

Ampl M1 2.245249mV
Ampl M2 942.0817µV
Ampl M3 631.9679µV
Ampl M4 426.2703µV
Ampl M5 301.4767µV
Ampl M6 243.6774µV
Ampl M7 222.8144µV

M1 2.000mV/ 0.0V 1.00000ns 40.600n
4:13 PM 2/18/2008

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Appendix C – Product and Test System Descriptions

Product Description

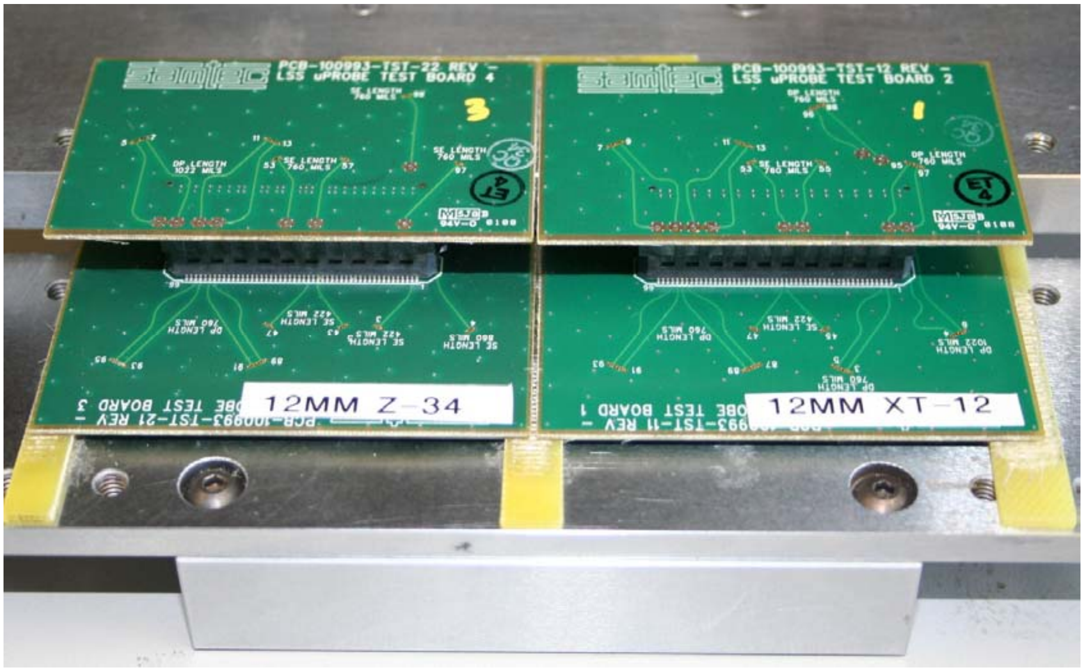
Product samples are the Locking Socket & Terminal Strip LSS Series. Mating connector halves are hermaphroditic and consist of one part number, LSS-150-01-X-DV-A. When mounted to the respective footprint of a PCB a 12mm (0.4724") stack height exists between boards using a -02/-02 combination. The connectors 150 designation indicates the structure consists of two rows of 50 contact terminals mounted into an insulating plastic housing having a PCB surface mount design. Terminals are centerlines on a 0.635mm (0.2362”) pitch.

Test System Description

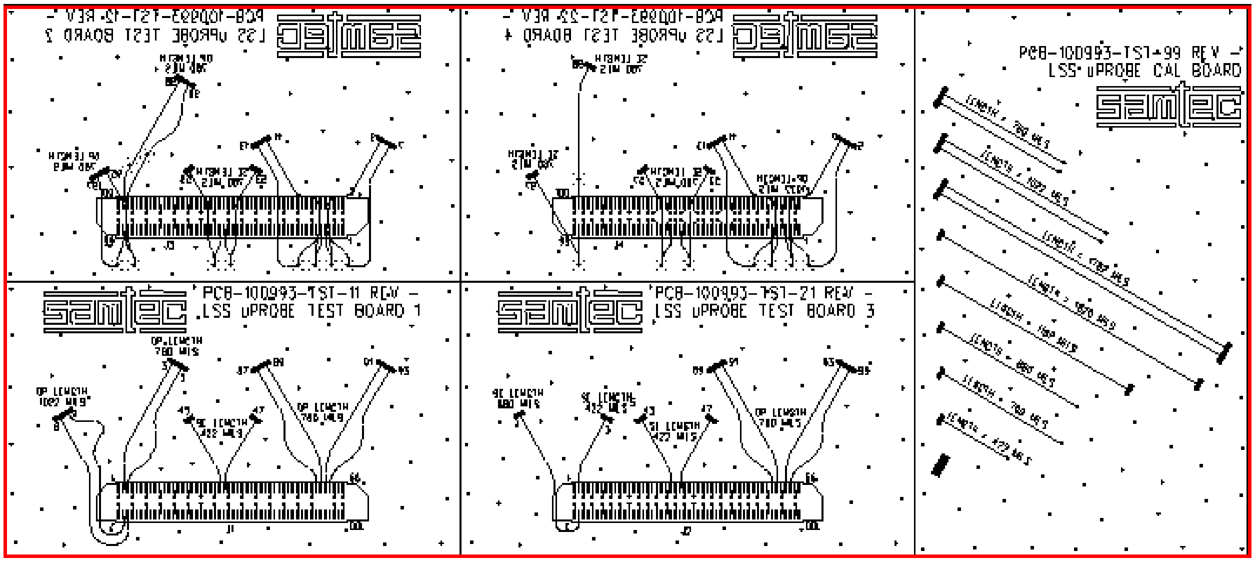
The test fixtures are composed of 4-layer FR-4 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. The test fixtures are specific to the LSS connector series and identified by Samtec P/N PCB-100993-TST-11, P/N PCB-100993-TST-12, P/N PCB-100993-TST-21 and P/N PCB-100993-TST-22. PCB-100993-TST-11 & PCB-100993-TST-12 serve as the signal launch board and terminate to the specified LSS-02 socket connector product. Test fixtures PCB-100993-TST-21 and P/N PCB-100993-TST-22 terminate to the specified LSS-02 terminal connector product. Electrical continuity exists between labeled test points when PCB-100993-TST-11 mates with PCB-100993-TST-21 and PCB-100993-TST-21 mates with PCB-100993-TST-22. Reference plane and calibration standards specific to the LSS-02/LSS-02 are located on the test calibration board LSS, PCB-100993-TST-99. All data and waveforms presented are results from an LSS-02 side signal launch. Pictured on page 27 are mated 12mm test samples and the panel layout for the breakaway printed circuit boards.

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

PCB-100993-TST- Mated 11 & 12, Mated 22 & 23, 12mm Test Fixtures



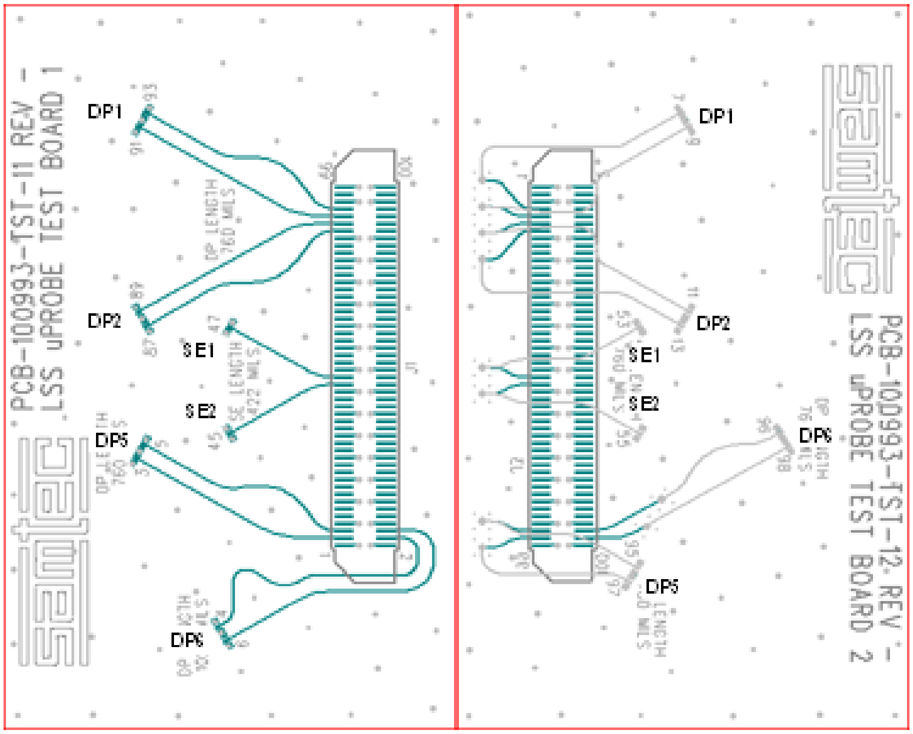
PCB-100993-TST PCB Layout Panel



PCB Fixture Set I

Fixture Identity
PCB-100993-TST-11 Rev – LSS Test Board
PCB-100993-TST-12 – Rev – LSS Test Board
Crosstalk Test Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT,

- DP2 to DP1, Differential, GAAVVG, 2:1 Signal to Ground Ratio,
  Near-End Aggressor: LSS; 87-89, Victim; LSS, 91-93
  Far-End Aggressor: LSS; 87-89, Victim; LSS, 7-9
- SE2 to SE1, Single-Ended, GAVG, 2:1 Signal to Ground Ratio,
  Near-End Aggressor: LSS; 45, Victim; LSS, 47
  Far-End Aggressor: LSS; 45, Victim; LSS, 5
- DP6 to DP5, Differential, GAAG/GVVG, 1:1 Signal to Ground Ratio,
  Near-End Aggressor: LSS; 4-6, Victim; LSS, 3-5
  Far-End Aggressor: LSS; 4-6, Victim; LSS, 95-97



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

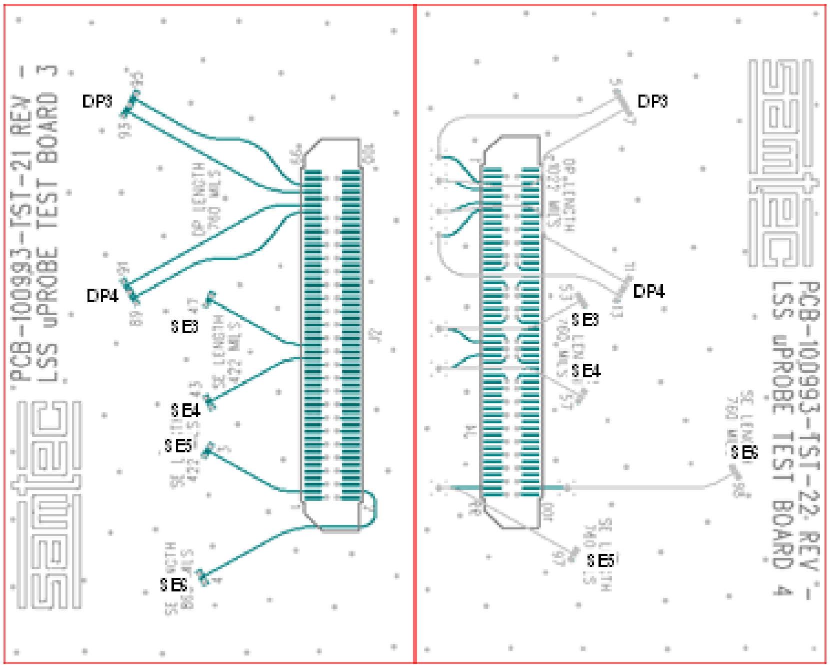
PCB Fixture Set II

Fixture Identity
PCB-100993-TST-21 Rev – LSS Test Board
PCB-100993-TST-22 – Rev – LSS Test Board
Frequency Domain S-Parameters (IL, RL) & Time Domain Test Parameters (Z, PD)

- DP3, Differential, GAAG, Tx: LSS 93-95, Rx: LSS; 5-7
- DP4, Differential, GAAG, Tx: LSS 87-89, Rx: LSS; 11-13 (available upon request)
- SE3, Single-Ended, GAG, Tx: LSS 47, Rx: LSS; 53
- SE4, Single-Ended, GAG, Tx: LSS 43, Rx: LSS; 57 (available upon request)

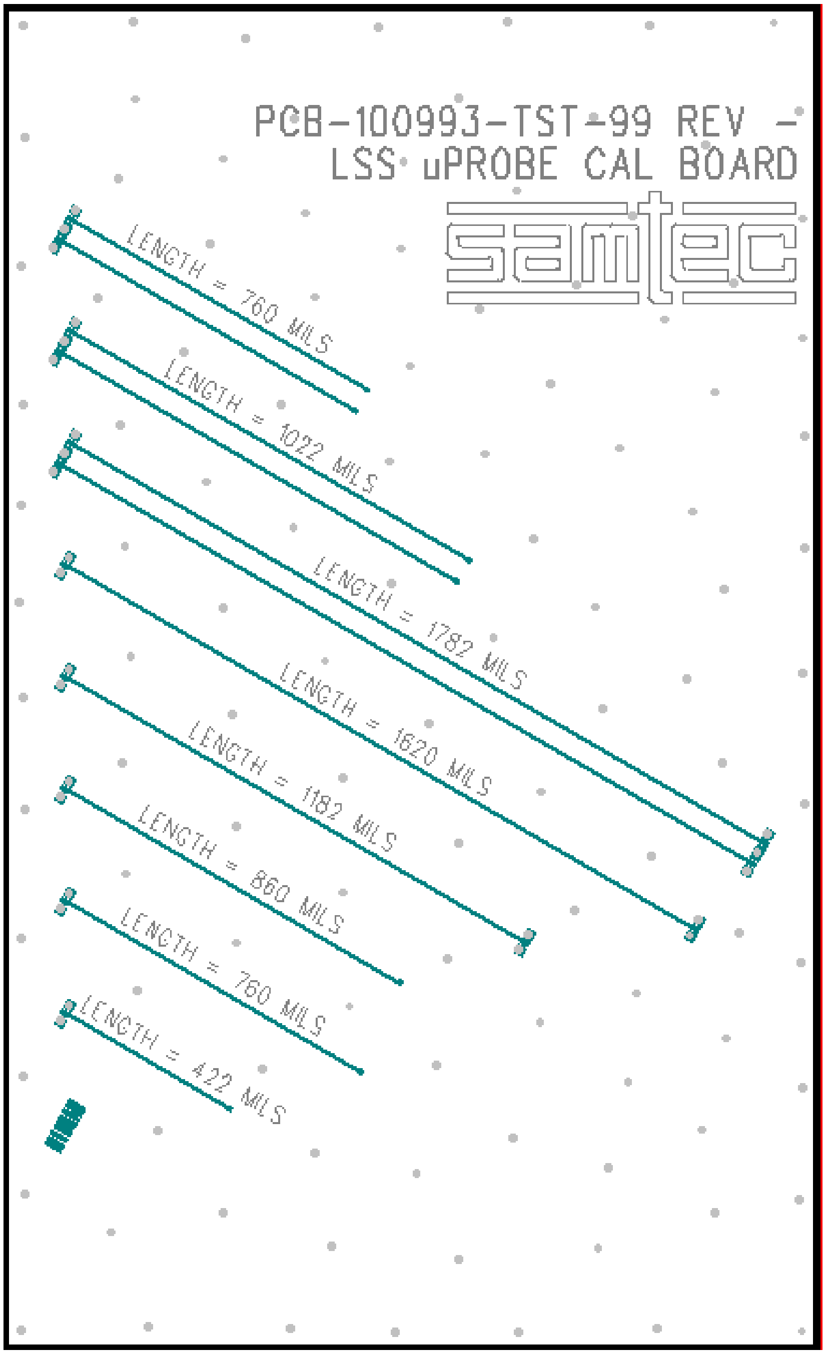
Crosstalk Test Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT,

- DP4 to DP3, Differential, GAAGVVG, 2:1 Signal to Ground Ratio,
  Near-End Aggressor: LSS; 87-89, Victim; LSS, 93-95
  Far-End Aggressor: LSS; 87-89, Victim; LSS, 5-7
- SE4 to SE3, Single-Ended, GAGVG, 1:1 Signal to Ground Ratio,
  Near-End Aggressor: LSS; 43, Victim; LSS, 47
  Far-End Aggressor: LSS; 43, Victim; LSS, 53
- SE6 to SE5, Single-Ended, GAG/GVG, 1:1 Signal to Ground Ratio,
  Near-End Aggressor: LSS; 4, Victim; LSS, 3
  Far-End Aggressor: LSS; 4, Victim; LSS, 97



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

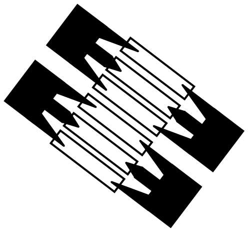
LSS/LSS Calibration Standards



Propagation Delay
Reference Length
Standard Differential,
1782 mils

Propagation Delay
Reference Length
Standard Single-Ended,
1182mils

TDA Step Waveform
Transmission/Reflection
Standard

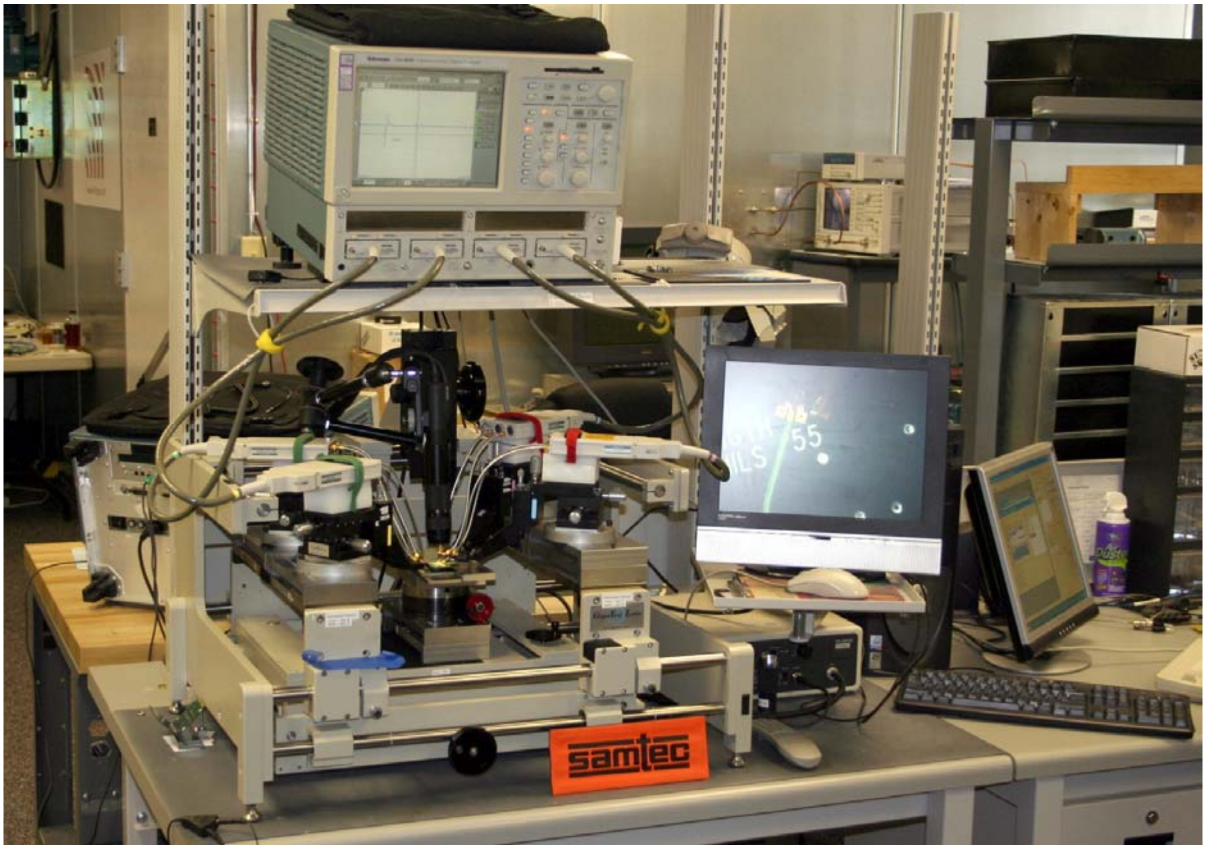


Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Appendix D – Test and Measurement Setup

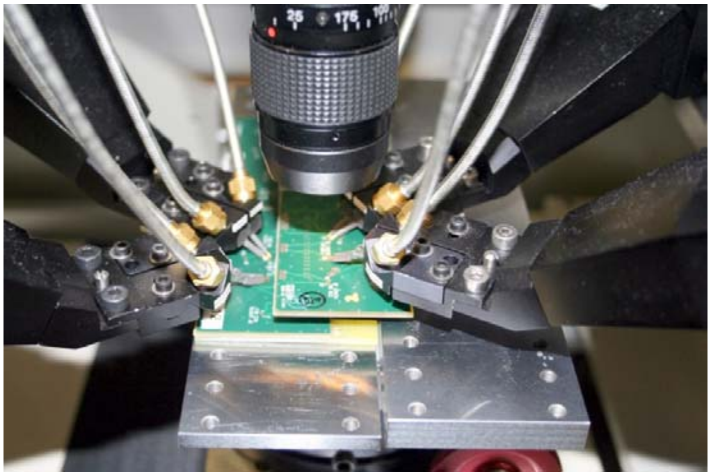
The test instrument is the Tektronix CSA8000 Communication Signal Analyzer Mainframe. Four bays of the CSA8000 use four Tektronix 80E04 TDR/Sampling Heads. Time domain data and graphs are real-time. Post-processed s-parameter data and graphs extend from a TDR based software tool called I-Connect Probing uses a video microscopy system, microprobe positioners, and 40GHz capable probes. Four hundred and fifty micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a ≥18 dB return loss, and an isolation of 38 dB providing high-bandwidth and low parasitic measurement results. Combined, the above technology provides a stable measurement environment along with the electrical accuracies for obtaining precise calibrations and signal launch capabilities

CSA8000/TDA IConnect Measurements Capability



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Four Position Dual 40 GHz Microprobe Setup



Test Instruments

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
4	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Tektronix 80E03 Dual Channel 20 GHz Sampling Module

Measurement Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
4	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

QTY	Description
8	Pasternack Enterprises 2.9mm Semi-Rigid (.086) 9” Cable Assemblies
4	Tektronix 1 Meter Module Extenders

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded.

Sample Preparation

Determine signal launch and monitoring test points by referencing the pin-out maps

Calibration Board, **CAL**
PCB Fixture Sets **I** & **II**

It is a good practice to terminate all non-active signal lines immediately adjacent to the designated active or quiet signal lines under test.

Frequency (S-Parameter) Domain Procedures

Frequency data extraction involves a two-step process. The first step creates the TDR based waveform relationships utilizing a Tektronix CSA8000 time based instrument. The second step involves the conversion of these time-based waveforms into s-parameter format using the TDA Systems IConnect software tool. TDA Systems labels time related conversion waveforms as the *Step* and *DUT* waveform references. This section establishes the setup procedures for defining the *Step* and *DUT* reference for conversion to frequency s-parameters presented in this report.

CSA8000 Setup

Listed below is the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. Functional settings such as window length, number of points and averaging capability determines the instruments frequency boundaries. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process. The single channel pulsed source processes s-parameters in single-ended format. A dual channel differential pulsed source processes s-parameters in differential format.

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss (TDA conversion)

Step Waveform - determine TD waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Complete the transmission path by inserting a negligible length of transmission standard between the system test probes. Calibration or waveform referencing utilizes a six pad cal structure for each of the probe touchdowns (ie; se thru = 3 pads or diff thru = 6 pads). Reference the calibration board **CAL**, and use the 1mm (0.390") length calibration reflect/transmission structure for TDA step waveform characterization.

DUT Waveform - determine TD waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the reflection/transmission standard and record the measurement. The LSS-02/LSS-02 characterization reports one single-ended and one differential insertion loss application. Single-ended and differential line measurement possibilities are SE3, SE4 DP3 and DP4. Reference PCB fixture set **II** for the configured signal path.

Return Loss (TDA conversion)

Step Waveform – determine TD waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. Calibration or waveform referencing utilizes three pads for each probe touchdown (ie; se reflect = 3 pads or diff reflect = 6 pads). Reference **CAL** calibration board and use the 1mm (0.390") length calibration reflect/transmission standard for TDA step waveform characterization.

DUT Waveform – determine waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the reflection/transmission standard and record the measurement. In this condition cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. The LSS-02/LSS-02 characterization reports one single-ended and one differential return loss application. Single-ended and differential line measurement possibilities are SE3 & SE4, and DP3 & DP4. Reference PCB fixture set **II** for the configured signal path.

Near-End Crosstalk (TDA conversion)

Step Waveform – Use Return Loss (RL) step waveform.

DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent near-end signal line. LSS-02/LSS-02 examines three single-ended and three differential near-end XT configurations. Single-ended crosstalk measurements are SE2 to SE1, SE4 to SE3, and SE6 to SE5. Differential crosstalk measurements are DP2 to DP1, DP4 to DP3, and DP6 to DP5. Reference both PCB fixture set **I** and fixture set **II** for crosstalk configurations.

Far-End Crosstalk (TDA conversion)

Step Waveform - Use Insertion Loss (IL) step waveform.

DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent far-end signal line. LSS-02/LSS-02 examines three single-ended and three differential far-end XT configurations. Single-ended crosstalk measurements are SE2 to SE1, SE4 to SE3, and SE6 to SE5. Differential crosstalk measurements are DP2 to DP1, DP4 to DP3, and DP6 to DP5. Reference both PCB fixture set **I** and fixture set **II** for crosstalk configurations.

Time Domain Procedures

Utilize the Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) method for digital type pulse measurements. Impedance and propagation delay characterization utilize TDR measurement methods. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to characterize the SUT.

Impedance(TDR)

Energize the SUT’s signal line(s) with a TDR pulse. The far-end of the energized signal lines are terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω termination) or use quality cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. The LSS-02/LSS-02 characterization reports one single-ended and one differential impedance application. Single-ended and differential line measurement possibilities are SE3, SE4, DP3, and DP4. Reference PCB fixture set **II** for a configured signal path.

Propagation Delay (TDT)

This test reports differential or single ended signal delay as the measured difference of propagation between a combined electrical length of the input/output signal pads and traces (35 ± 5 ps edge rate) and the device under test (DUT) plus a referenced electrical length of the signal pads and signal traces ($PD^{pads/traces} - \mathbf{PD}^{\mathbf{DUT}} + PD^{pads/traces}$). The recorded delay is the signal delay of the connector only. $PD^{pads/traces}$ is the nomenclature representing the electrical length of PCB signal pads & traces equal to physical lengths of PCB pads & traces entering and leaving the device under test (DUT). The $PD^{DUT} + PD^{pads/traces}$ variable is the mated DUT fixture. Measure the risetime of $PD^{pads/traces}$ waveform & $\mathbf{PD}^{\mathbf{DUT}} + PD^{pads/traces}$ waveforms. Record the 50% amplitude of each rising edge. The distance in time between the rising edges is the propagation delay of the device under test (DUT). Single-ended and differential line measurement possibilities are SE3, SE4, DP3, and DP4. Reference the calibration board **CAL** for input/output signal line traces and PCB fixture set **II** for a configured signal path.

Near-End Crosstalk (TDT)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the near-end for magnitudes of coupled energy. Terminate adjacent signal lines not under test in the test systems characteristic impedance LSS-02/LSS-02 examines three single-ended and three differential near-end XT configurations. Single-ended crosstalk measurements are SE2 to SE1, SE4 to SE3, and SE6 to SE5. Differential crosstalk measurements are DP2 to DP1, DP4 to DP3, and DP6 to DP5. Reference both PCB fixture set **I** and fixture set **II** for crosstalk configurations.

Series: Terminal/Socket LSS Series
Description: 0.635mm (.025”) Pitch, 12mm (0.4724") Stack Height

Far-End Crosstalk (TD)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the far-end for magnitudes of coupled energy. Terminate adjacent signal lines not under test into the test systems characteristic impedance. LSS-02/LSS-02 examines three single-ended and three differential far-end XT configurations. Single-ended crosstalk measurements are SE2 to SE1, SE4 to SE3, and SE6 to SE5. Differential crosstalk measurements are DP2 to DP1, DP4 to DP3, and DP6 to DP5. Reference both PCB fixture set **I** and fixture set **II** for crosstalk configurations.

Appendix F – Glossary of Terms

TD – Time Domain
FD – Frequency domain
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
EC6 – Edge Card with a .635mm signal pad pitch
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
LEC6 – Signal Launch Edge Card with a .635 mm signal pad pitch
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
BC – Best Case crosstalk configuration
Z – Impedance (expressed in ohms)
OV – Optimal Vertical
OH – Optimal Horizontal
HDV – High Density Vertical
PPO – Pin Population Option
S – Static (independent of PCB ground)