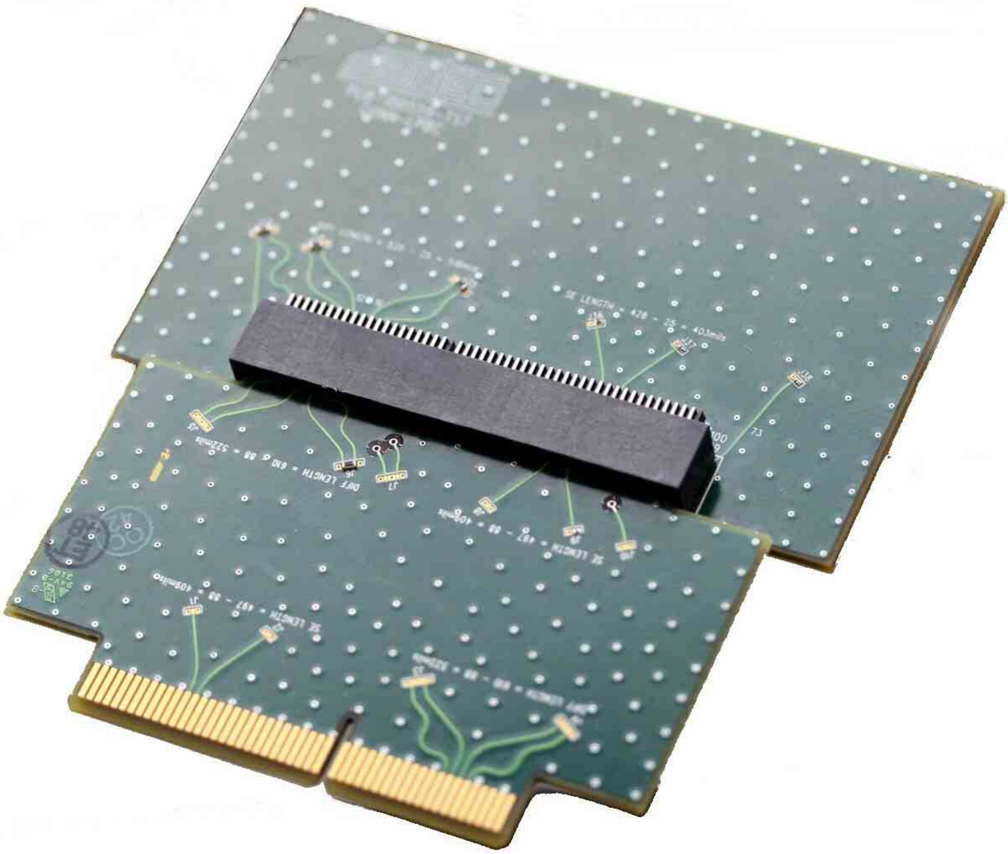
High Speed Characterization Report

MEC1-150-02-L-D-RA1



Description:

Mini Edge-Card Socket
Right Angle Surface Mount, 1.0mm (.03937”) Pitch

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047

Report Revision: 10/3/2006

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

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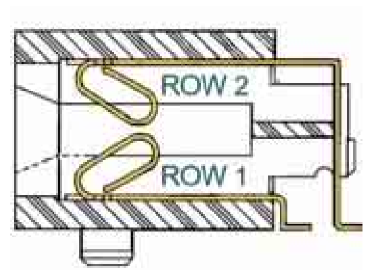
Connector Overview

Mini Edge-Card 1.0mm (.03937") pitch socket connectors (MEC1 Series) are double row structures with up to 70 contacts per row. The MEC1 connector is available in a vertical, right angle or edge body mount style designed for use with 1.60mm edge-card thicknesses. Applications can include board-to-board or cable-to-board. The electrical characteristics reported are specific to a MEC1 right angle mount socket connector mated with a 1.0mm pitch, 1.60mm (.062") thickness test specific edge-card.

Connector System Speed Rating

MEC1 Series, 1.0mm (.03937") Pitch Socket, Right Angle Body Style

Signaling	Speed Rating
Row 1 (Inner), Single-Ended:	**4.5 GHz / 9 Gbps**
Row 1 (Inner), Differential:	**5.5 GHz / 11 Gbps**
Row 2 (Outer), Single-Ended:	**3.0 GHz / 6 Gbps**
Row 2 (Outer), Differential:	**4.0 GHz / 8 Gbps**



The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board's trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/ 15 Gbps.

Series: MEC1- RA1 Series
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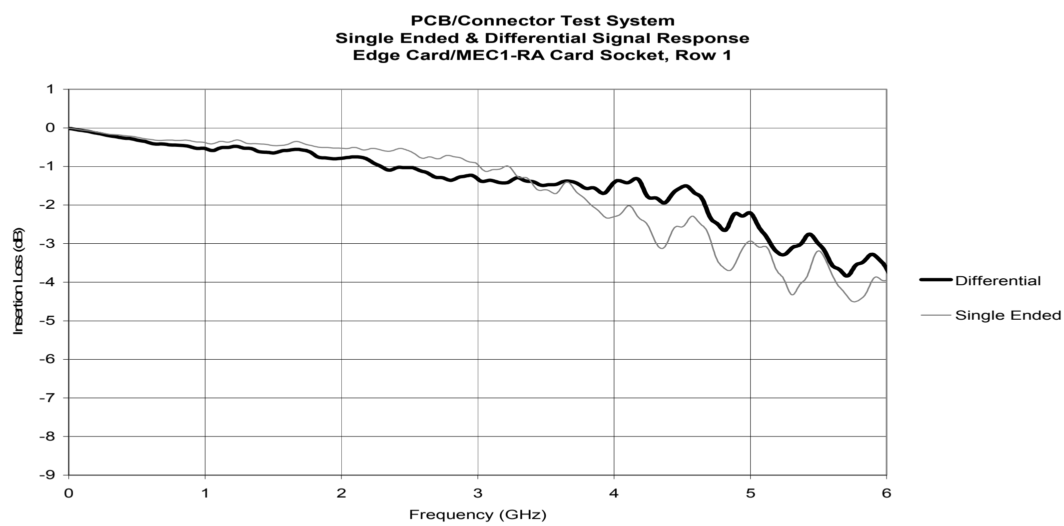
Frequency Domain Data Summary *(Row 1 - Inner)*

Table 1 - Single-Ended Connector System Performance		
Test Parameter	**Configuration**	
Insertion Loss	GSG	-3dB @ 4.32 GHz
Return Loss	GSG	≤ -5dB to 4.32 GHz
Near-End Crosstalk	GAQG	≤ - 5dB to 4.32 GHz
	GAGQG	≤ -18dB to 4.32 GHz
	Xrow, GAG to GQG	≤ -28dB to 4.32 GHz
Far-End Crosstalk	GAQG	≤ -10dB to 4.32 GHz
	GAGQG	≤ -15dB to 4.32 GHz
	Xrow, GAG to GQG	≤ -28dB to 4.32 GHz

Table 2 - Differential Connector System Bandwidth		
Test Parameter	**Configuration**	
Insertion Loss	GSSG	-3dB @ 5.16 GHz
Return Loss	GSSG	≤ -5dB to 5.16 GHz
Near-End Crosstalk	GAAQQG	≤ -20dB to 5.16 GHz
	GAAGQQG	≤ -35dB to 5.16 GHz
	Xrow, GAASSG to GQQG	≤ -44dB to 5.16 GHz
Far-End Crosstalk	GAAQQG	≤ -25dB to 5.16 GHz
	GAAGQQG	≤ -38dB to 5.16 GHz
	Xrow, GAASS to GQQG	≤ -44dB to 5.16 GHz



Series: MEC1- RA1 Series
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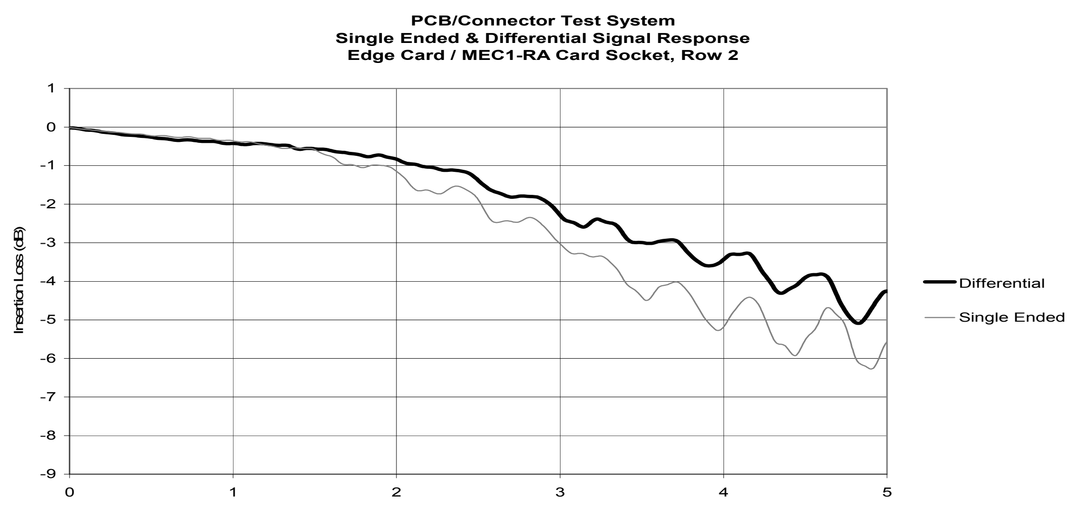
Frequency Domain Data Summary *(Row 2 - Outer)*

Table 3 - Single-Ended Connector System Performance		
Test Parameter	**Configuration**	
Insertion Loss	GSG	-3dB @ 3.00 GHz
Return Loss	GSG	≤ -3dB to 3.00 GHz
Near-End Crosstalk	GAQG	≤ -5dB to 3.00 GHz
	GAGQG	≤ -22dB to 3.00 GHz
	Xrow, GAG to GQG	≤ -30dB to 3.00 GHz
Far-End Crosstalk	GAQG	≤ -12dB to 3.00 GHz
	GAGQG	≤ -22dB to 3.00 GHz
	Xrow, GAG to GQG	≤ -32dB to 3.00 GHz

Table 4 - Differential Connector System Bandwidth		
Test Parameter	**Configuration**	
Insertion Loss	GSSG	-3dB @ 3.52 GHz
Return Loss	GSSG	≤ -3dB to 3.52 GHz
Near-End Crosstalk	GAAQQG	≤ -18dB to 3.52 GHz
	GAAGQQG	≤ -35dB to 3.52 GHz
	Xrow, GAASSG to GQQG	≤ -32dB to 3.52 GHz
Far-End Crosstalk	GAAQQG	≤ -25dB to 3.52 GHz
	GAAGQQG	≤ -35dB to 3.52 GHz
	Xrow, GAASS to GQQG	≤ -44dB to 3.52 GHz



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Time Domain Data Summary *(Row 1 - Inner)*

Table 5 - Single-Ended Impedance (Ω)							
Signal Risetime	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	56.8	54.8	53.0	52.0	51.7	51.6	51.5
Minimum Impedance	28.5	34.5	41.6	47.1	48.1	48.7	49.2

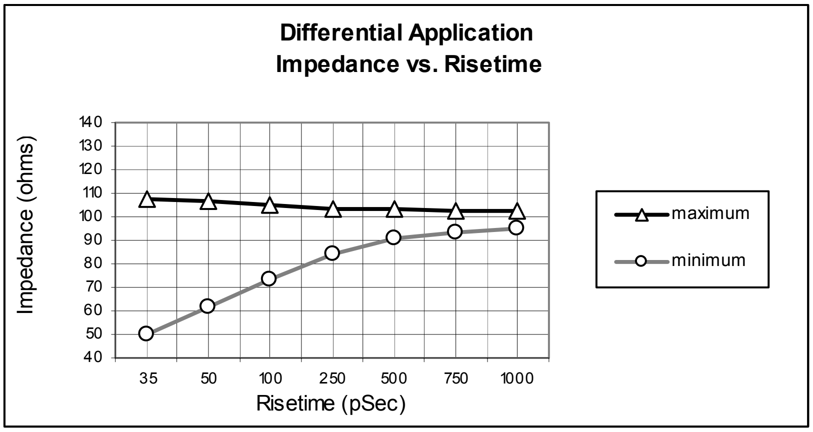

Table 6 - Differential Impedance (Ω)							
Signal Risetime	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	107.2	106.3	105.2	103.4	102.9	102.7	102.7
Minimum Impedance	50.0	61.4	73.6	84.6	90.5	93.3	95.1

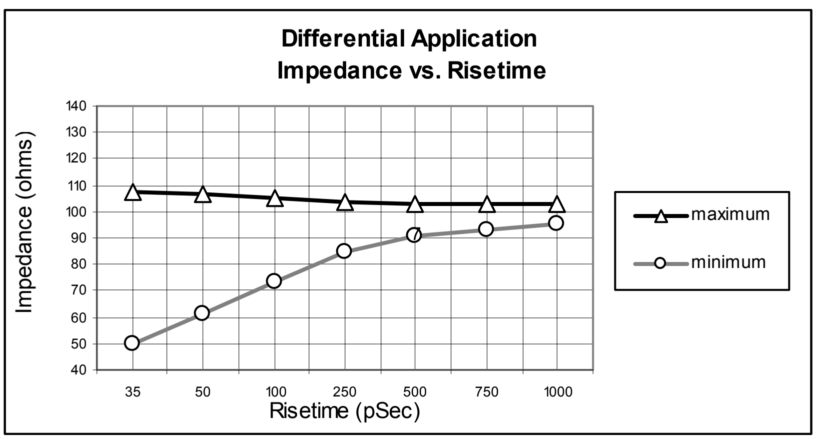

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Table 7 - Single-Ended Crosstalk (%)

Input (t_r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAQG	13.7	12.3	10.8	6.5	3.6	2.5	1.9
	GAGQG	3.1	2.6	2.4	1.4	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{se}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	GAQG	7.6	6.1	4.3	1.8	< 1.0%	< 1.0%	< 1.0%
	GAGQG	3.8	3.1	2.2	1.0	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{se}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 8 - Differential Crosstalk (%)

Input (t_r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAAQQSS	3.7	3.3	2.8	1.6	< 1.0%	< 1.0%	< 1.0%
	GAAGQQG	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{diff}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	GAAQQSS	1.6	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	GAAGQQG	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{diff}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 9 - Propagation Delay (Mated Connector)

Single-Ended, Row 1	99ps
Differential, Row 1	93ps

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Time Domain Data Summary *(Row 2 - Outer)*

Table 10 - Single-Ended Impedance (Ω)							
Signal Risetime	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	77.5	75.0	70.3	59.5	54.9	53.6	53.0
Minimum Impedance	27.4	33.4	40.9	48.8	49.9	50.0	50.0

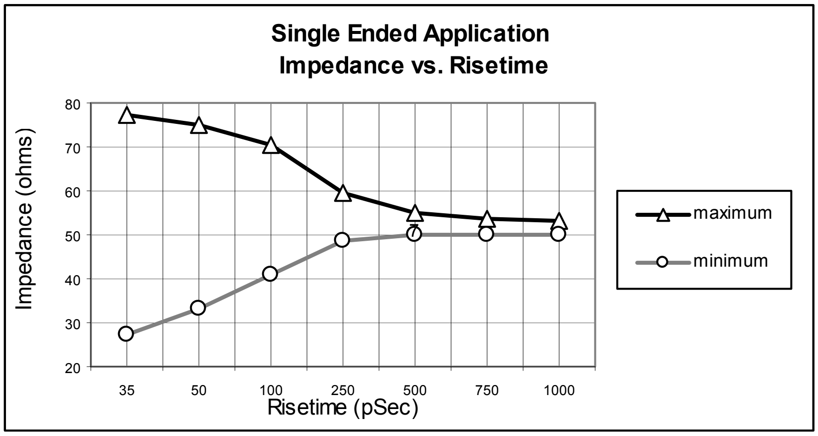

Table 11 - Differential Impedance (Ω)							
Signal Risetime	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	120.4	118.1	111.6	103.9	103.3	103.0	102.8
Minimum Impedance	48.8	59.9	73.1	89.9	95.0	96.7	97.9

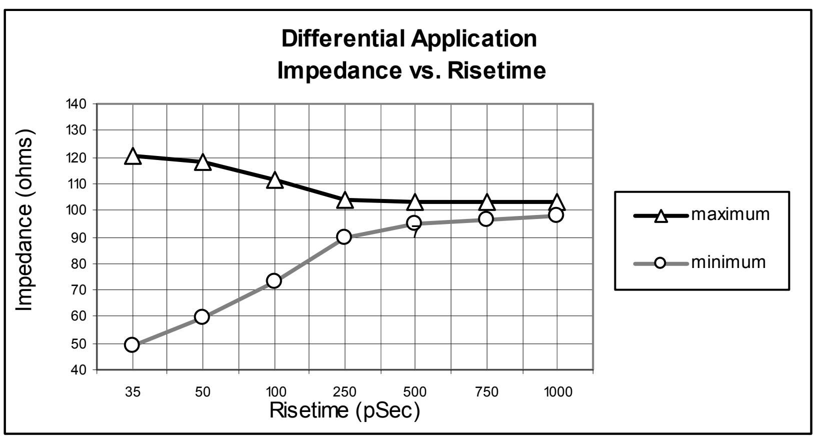

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Table 12 - Single-Ended Crosstalk (%)

Input (t_r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAQG	14.3	13.4	12.8	9.4	5.8	4.1	3.2
	GAGQG	4.1	3.3	2.5	1.7	1.0	< 1.0%	< 1.0%
	$Xrow^{se}$	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	GAQG	8.7	7.5	6.7	4.3	2.6	1.8	1.4
	GAGQG	3.5	2.7	1.8	1.1	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{se}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 13 - Differential Crosstalk (%)

Input (t_r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAAQQSS	4.5	4.0	3.7	2.6	1.5	1.1	< 1.0%
	GAAGQQG	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{diff}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	GAAQQSS	1.4	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	GAAGQQG	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	$Xrow^{diff}$	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 14 - Propagation Delay (Mated Connector)

Single-Ended, Row 2	116ps
Differential, Row 2	108ps

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Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from the test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors’ true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as “ground”. In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others; connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

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For this connector, the following configurations were evaluated:

Single-Ended Impedance:
- GSG (ground-signal-ground)

Single-Ended Crosstalk:
- Electrical "worst case": GAQG (ground-active-quiet-ground)
- Electrical "best case": GAGQG (ground-active-ground-quiet-ground)
- Across row: $Xrow^{se}$ (from one row of terminals to the other row or across the ground blade when applicable)

Differential Impedance:
- GSSG (Ground-positive signal-negative signal-ground)

Differential Crosstalk:
- Electrical "worst case": GAAQQG (ground-active-active-quiet-quiet-ground)
- Electrical "best case": GAAGQQG (ground-active-active-ground-quiet-quiet-ground)
- Across row: $Xrow^{diff}$ (from one row of terminals to the other row or across the ground blade when applicable) (ground-active-active-static-static-ground) across the row of terminals to (ground-quiet-quiet-ground)

In all cases where a center ground blade is present in the connector it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

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Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of an interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, rise times were measured at 10%-90% signal levels.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system’s signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT’s frequency domain data are provided in the frequency domain test procedures in Appendix G of this report.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix G of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 30 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 30 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

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Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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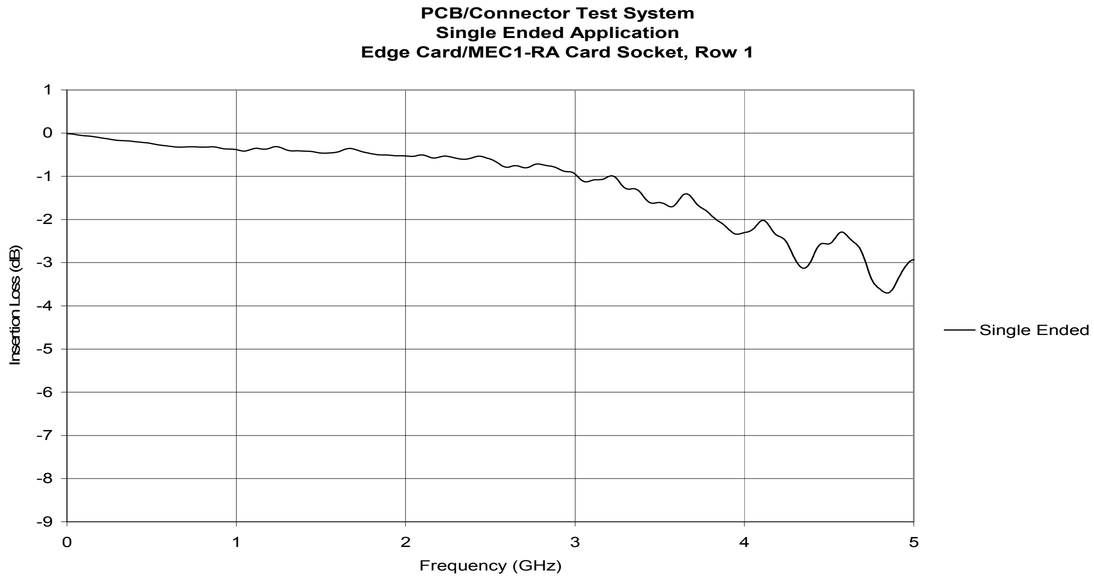
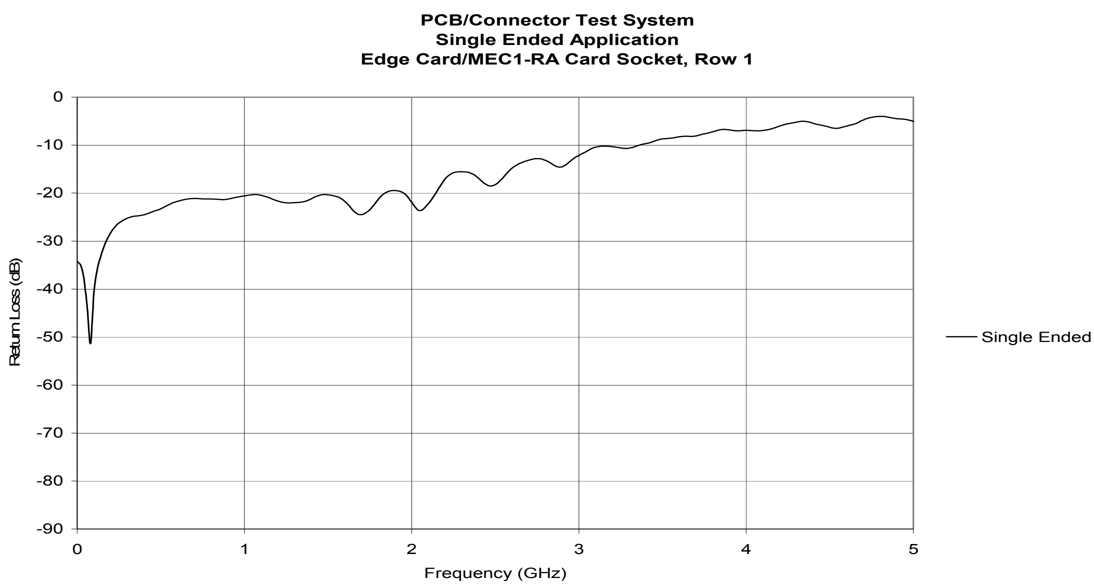
Appendix A – Frequency Domain Response Graphs *(Row 1 - Inner)*

Single-Ended Application – Insertion Loss



Single-Ended Application – Return Loss



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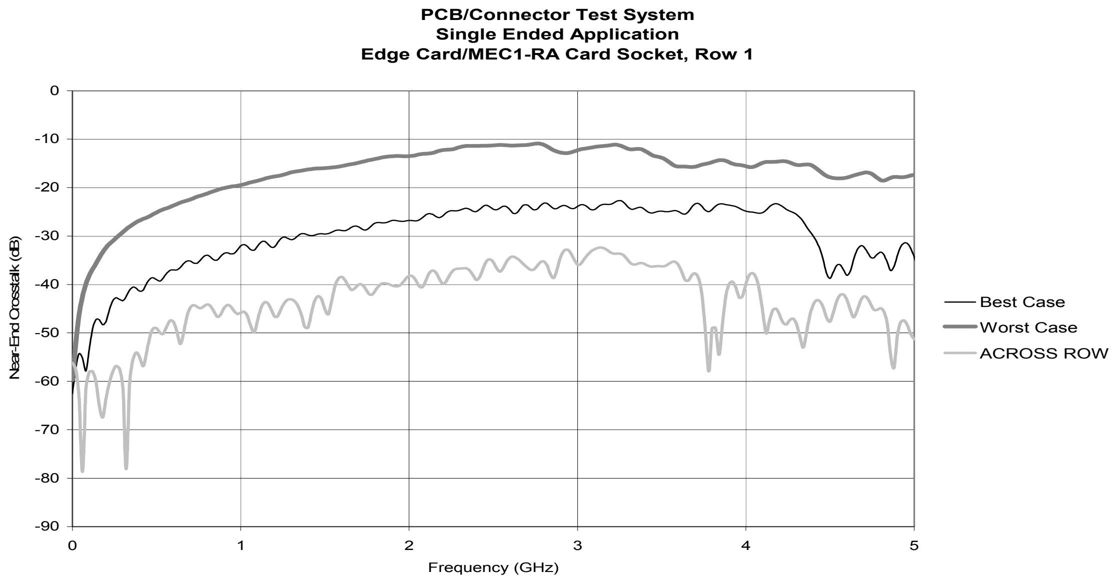
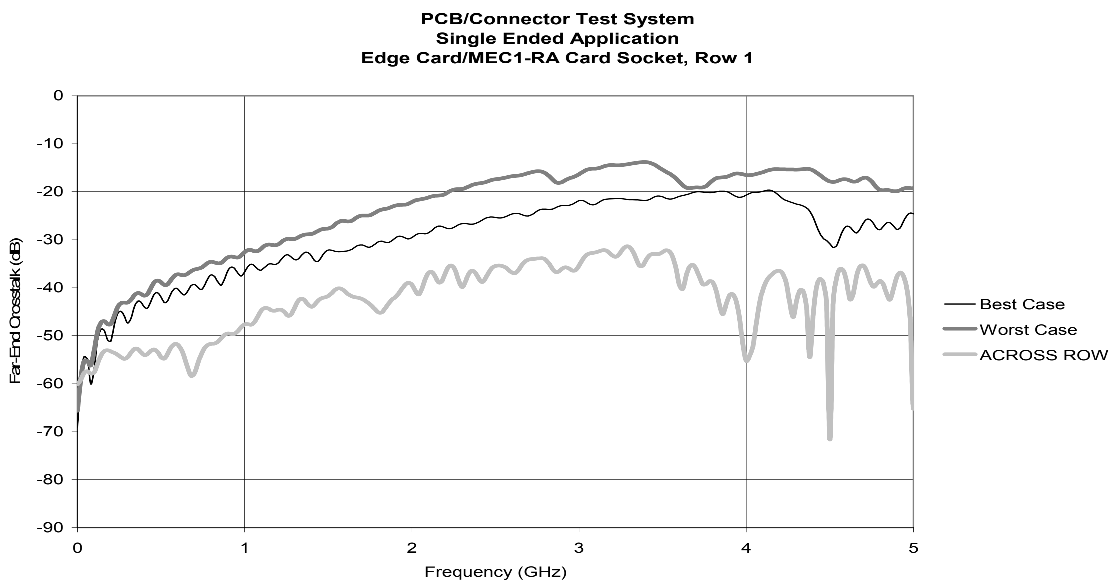
Single-Ended Application – NEXT



Single-Ended Application – FEXT



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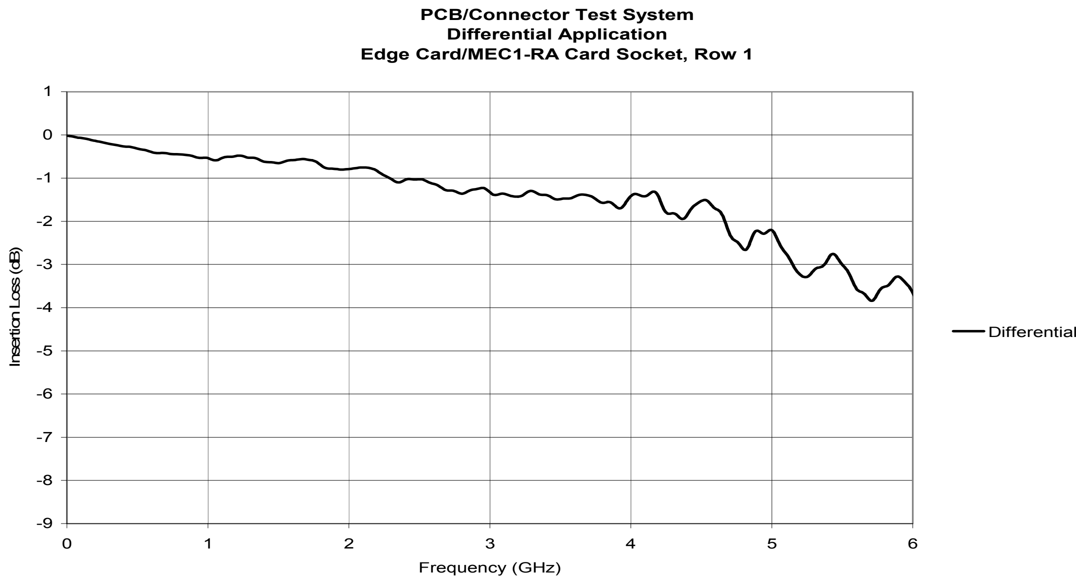
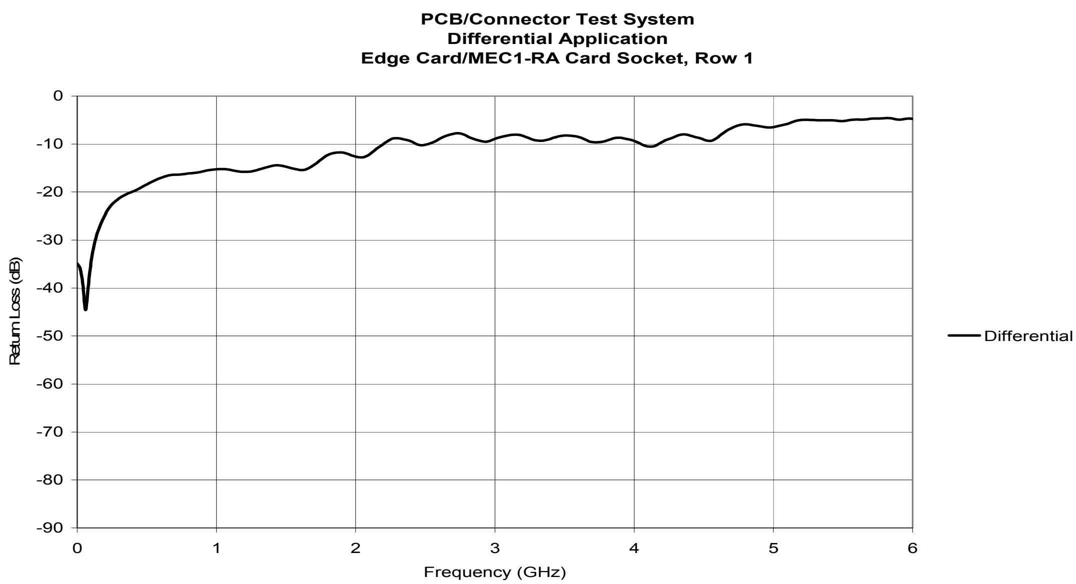
Differential Application – Insertion Loss



Differential Application – Return Loss



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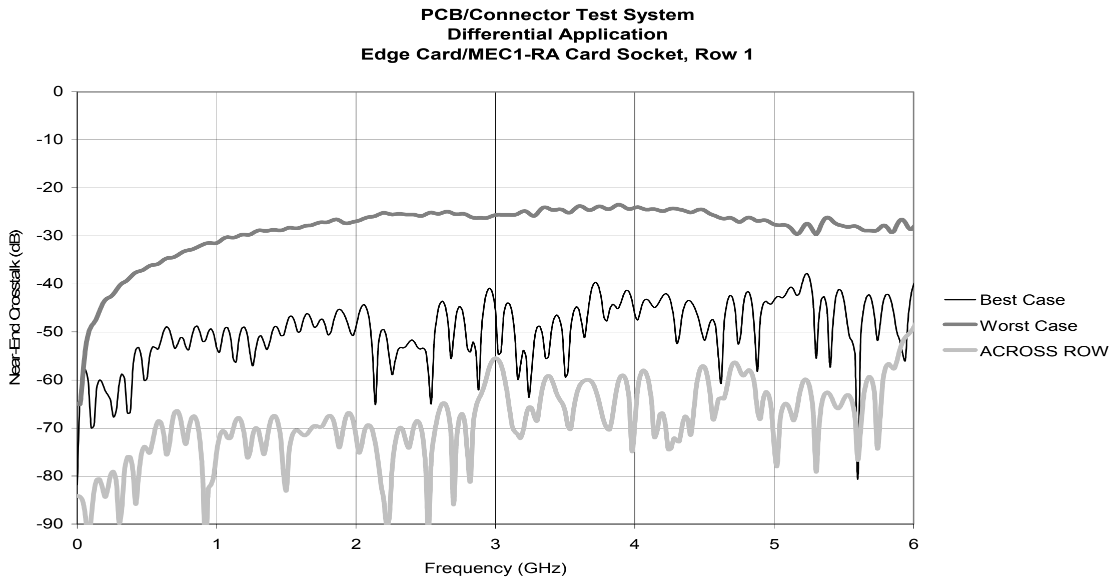
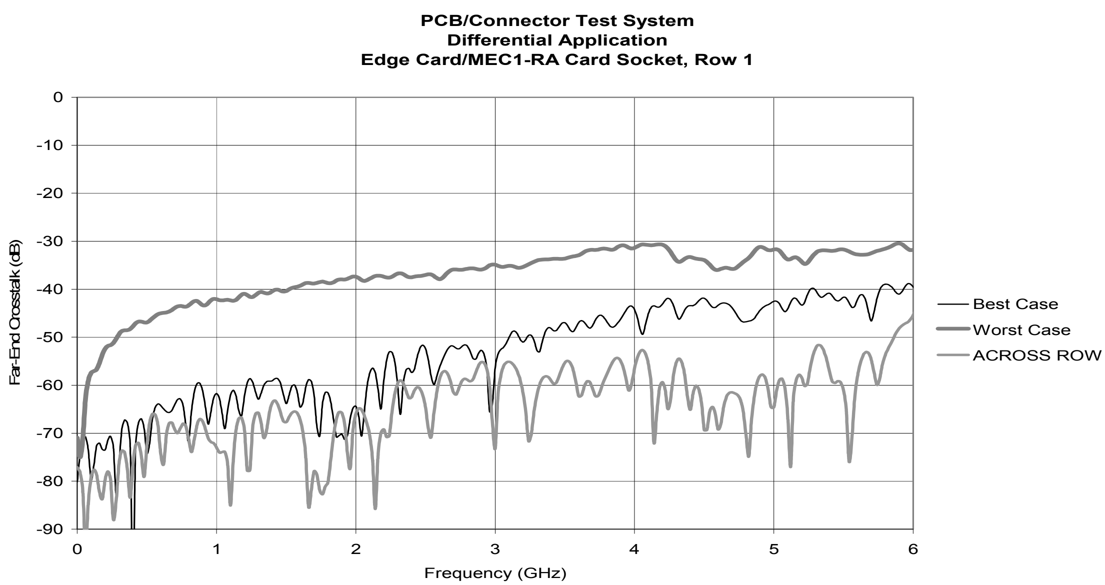
Differential Application – NEXT



Differential Application – FEXT



Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

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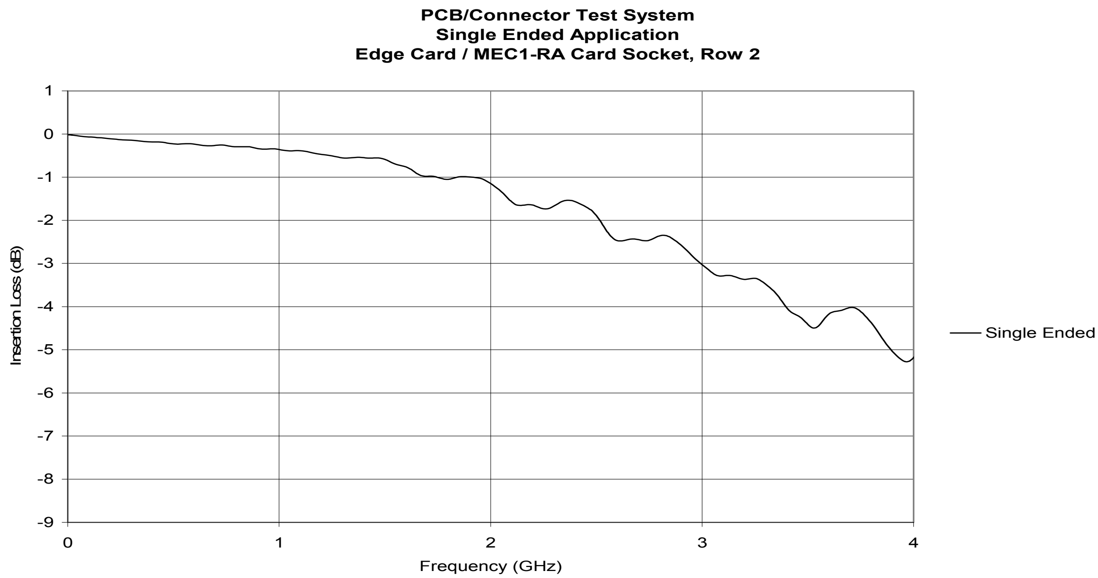
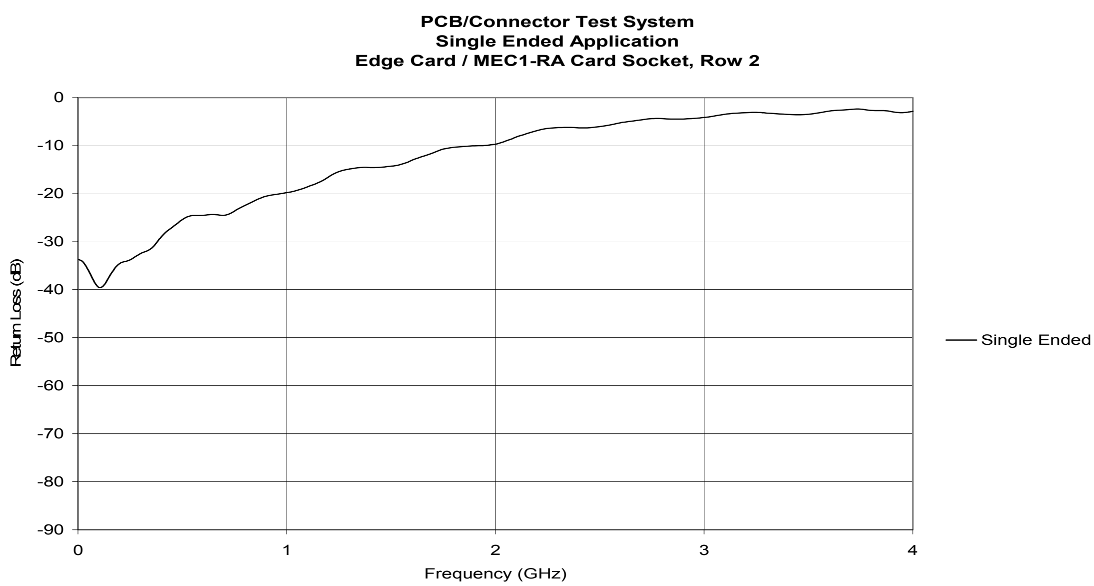
Appendix B – Frequency Domain Response Graphs *(Row 2 - Outer)*

Single-Ended Application – Insertion Loss



Single-Ended Application – Return Loss



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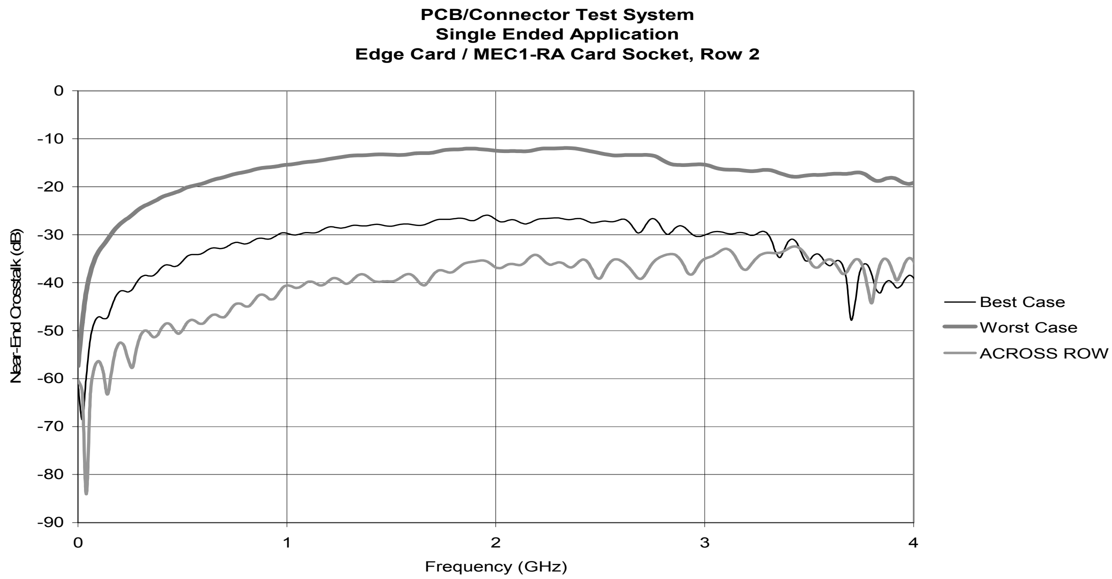
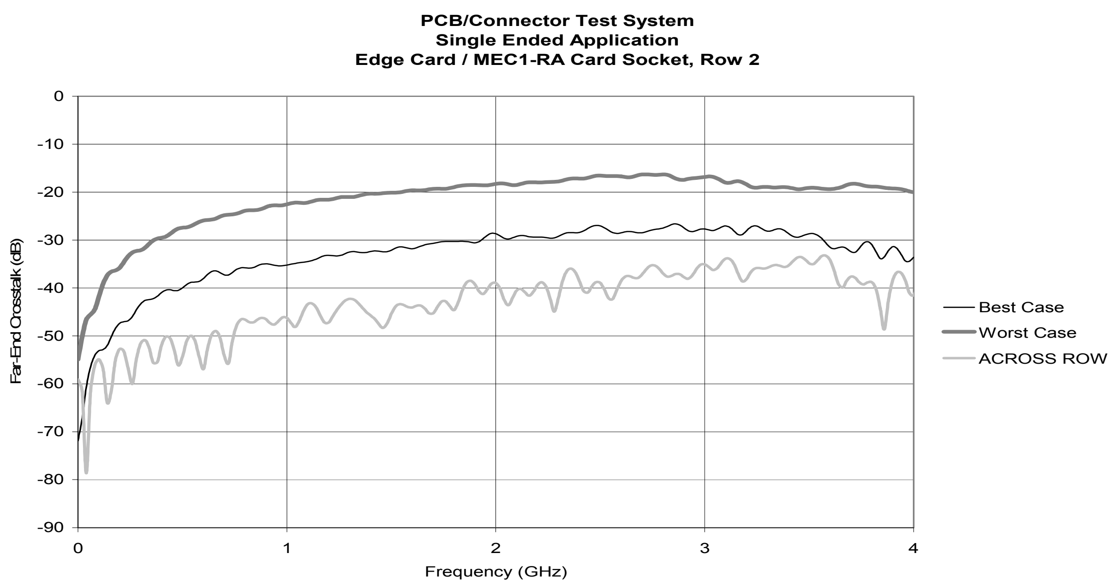
Single-Ended Application – NEXT

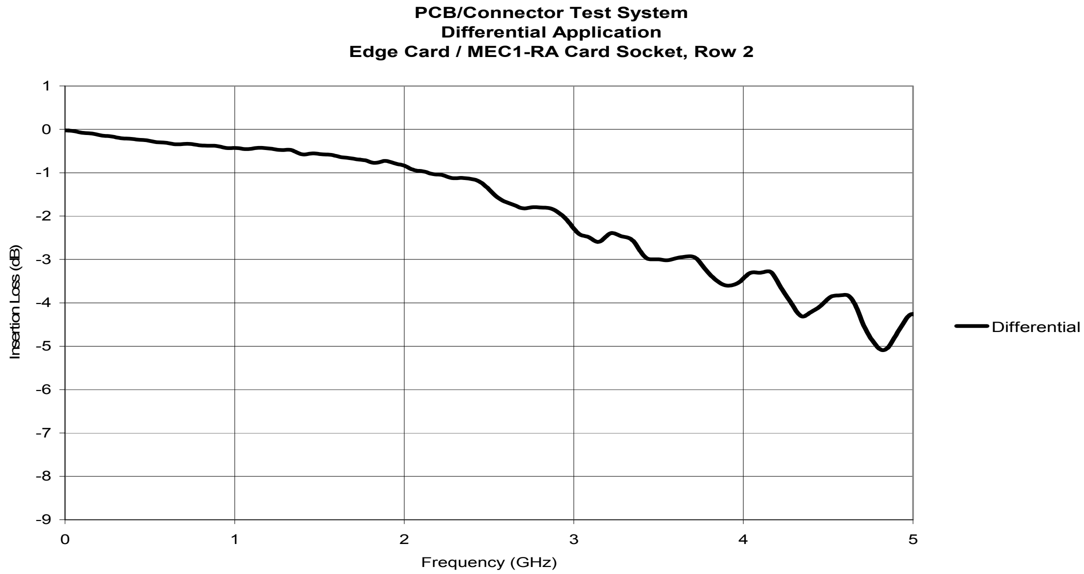


Single-Ended Application – FEXT

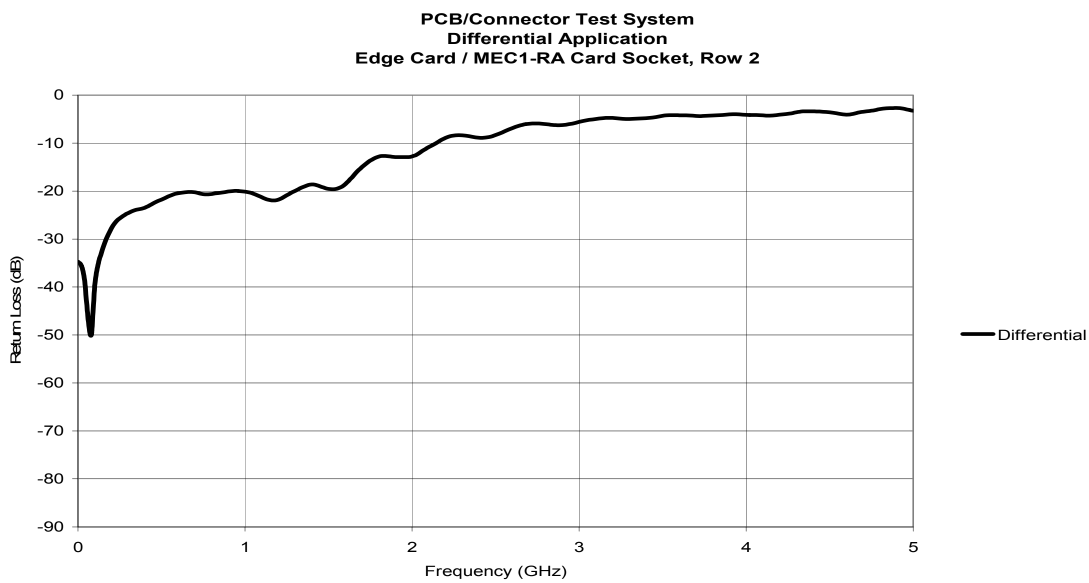


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Differential Application – Insertion Loss

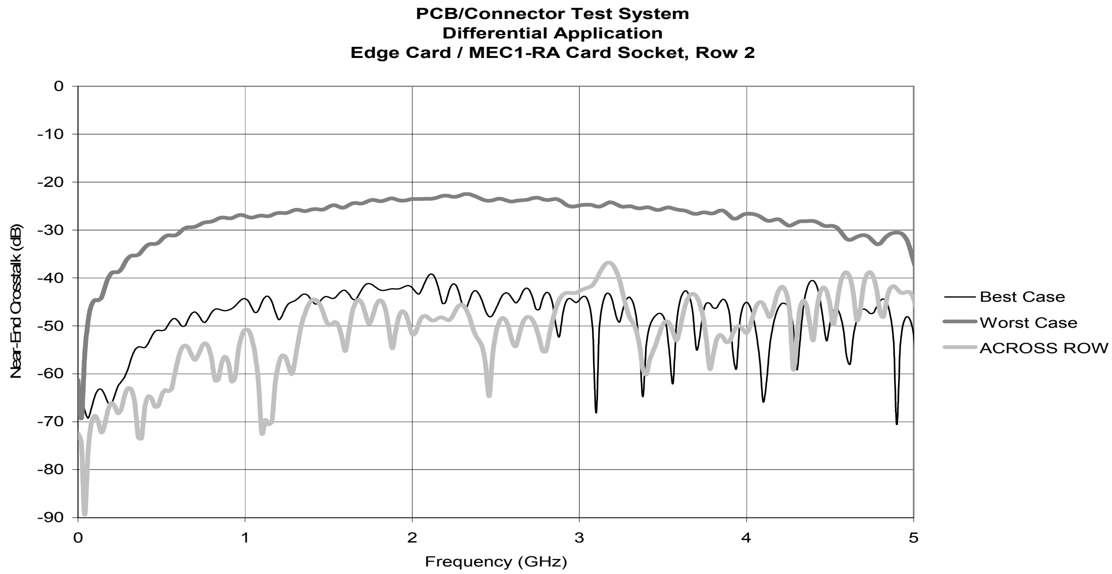


Differential Application – Return Loss

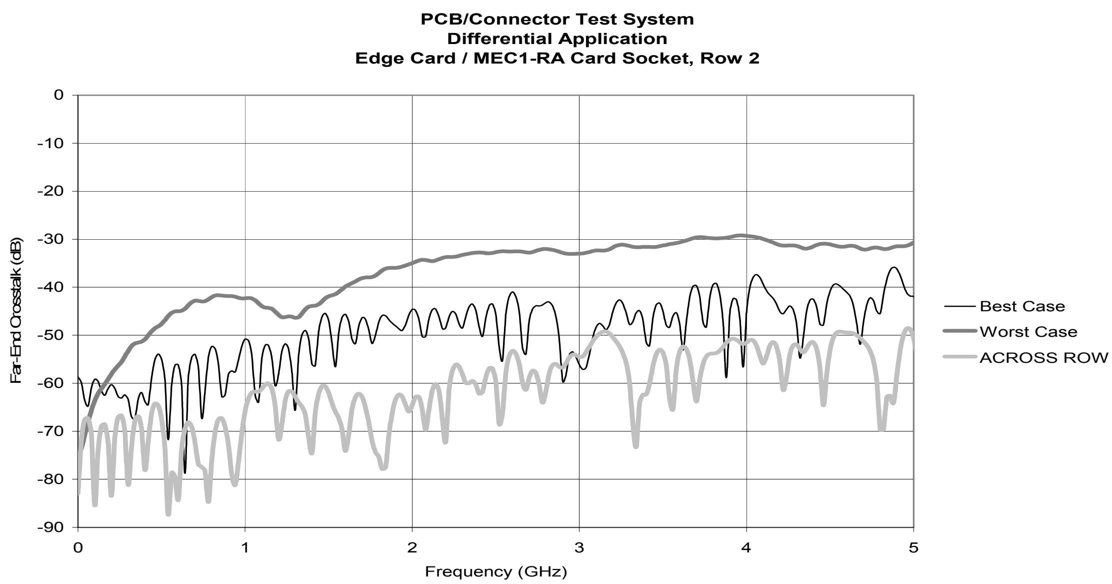


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Differential Application – NEXT



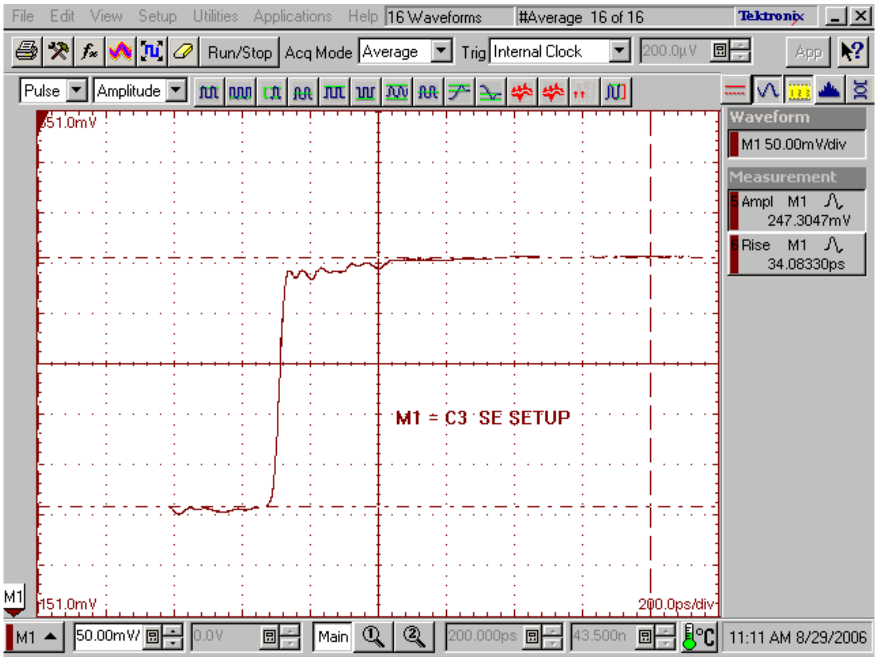
Differential Application – FEXT



Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

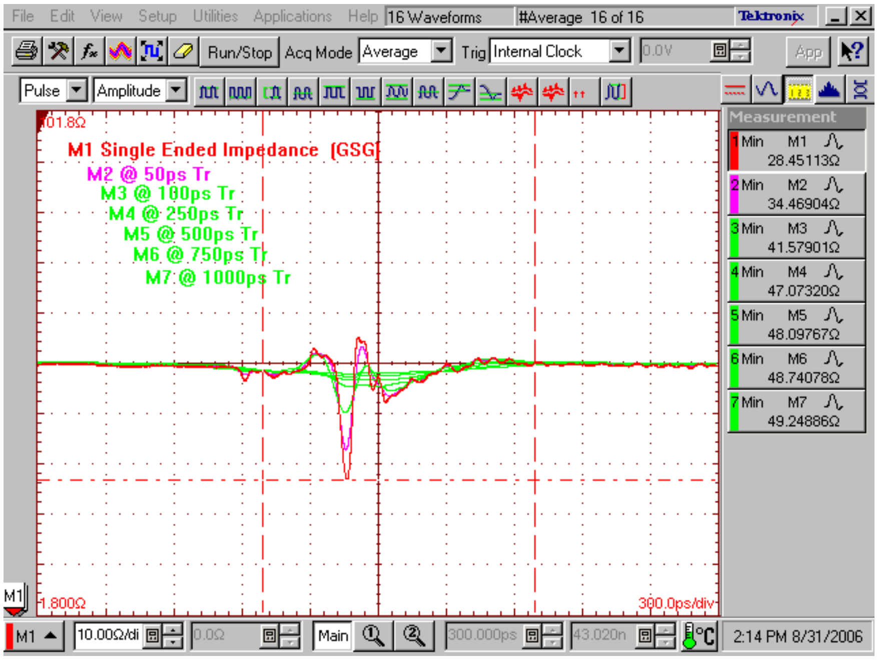
Appendix C – Time Domain Response Graphs *(Row 1 - Inner)*

Single-Ended Application – Input Pulse

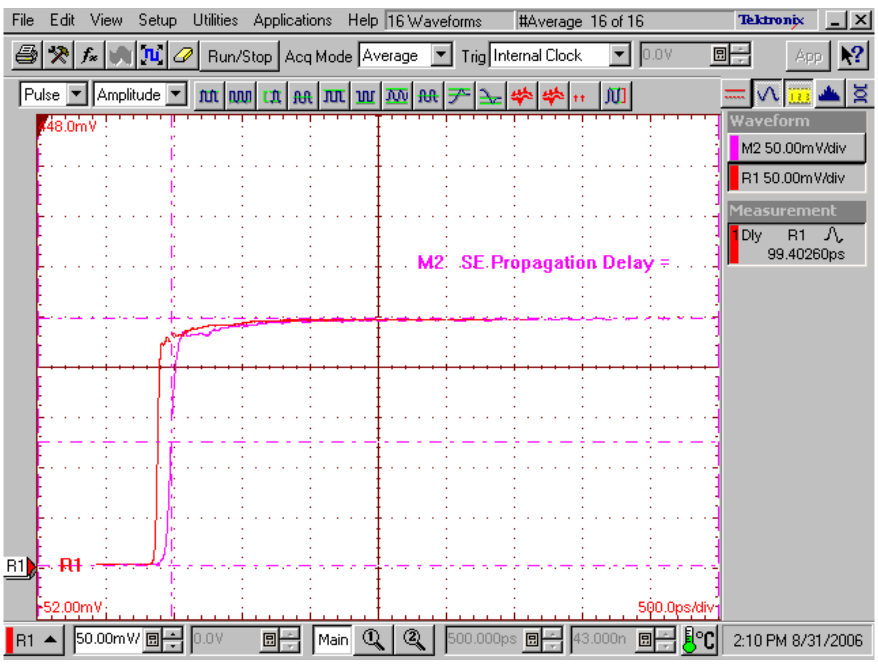


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – Impedance

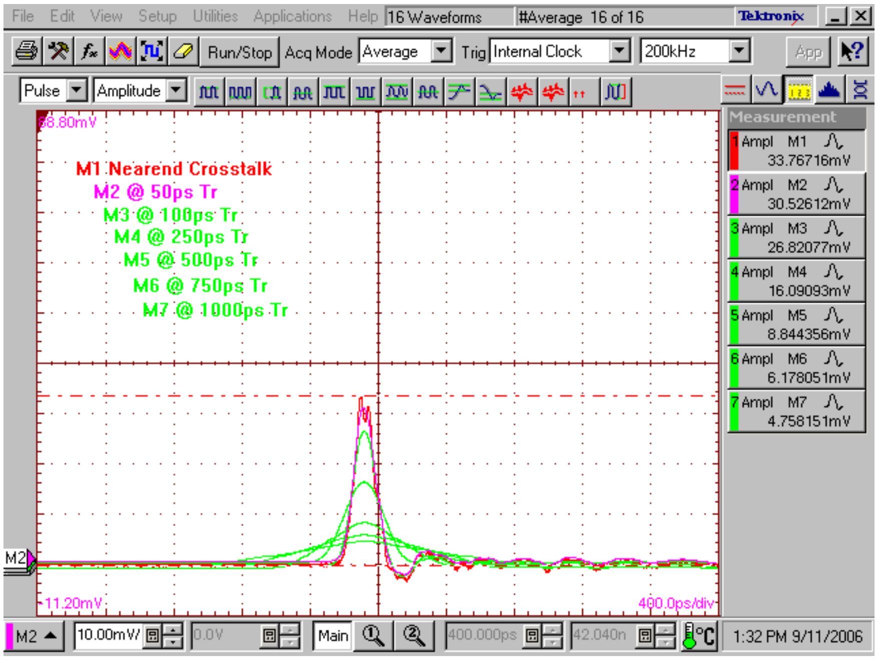


Single-Ended Application – Propagation Delay

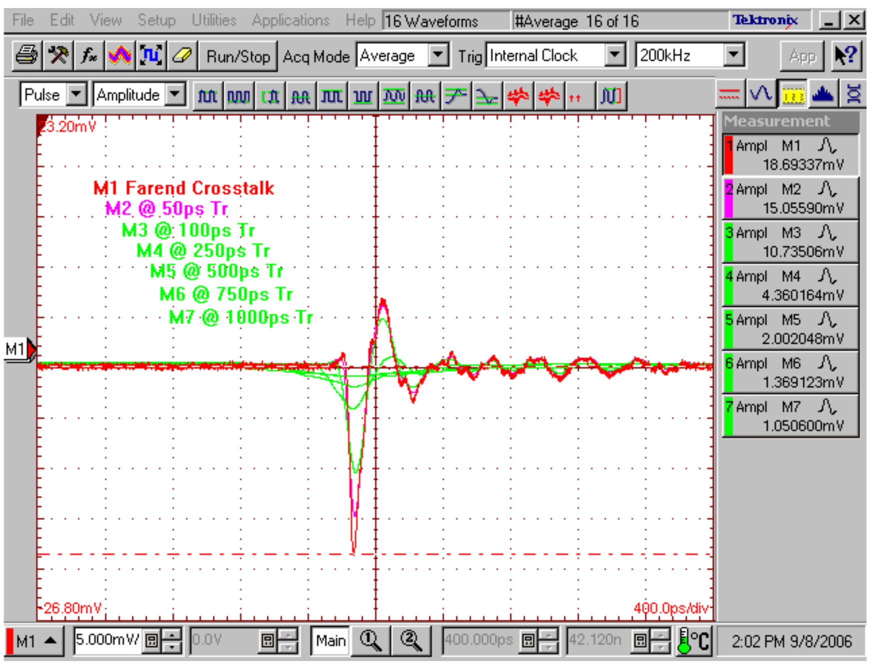


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – NEXT, "Worst Case in Row" Configuration

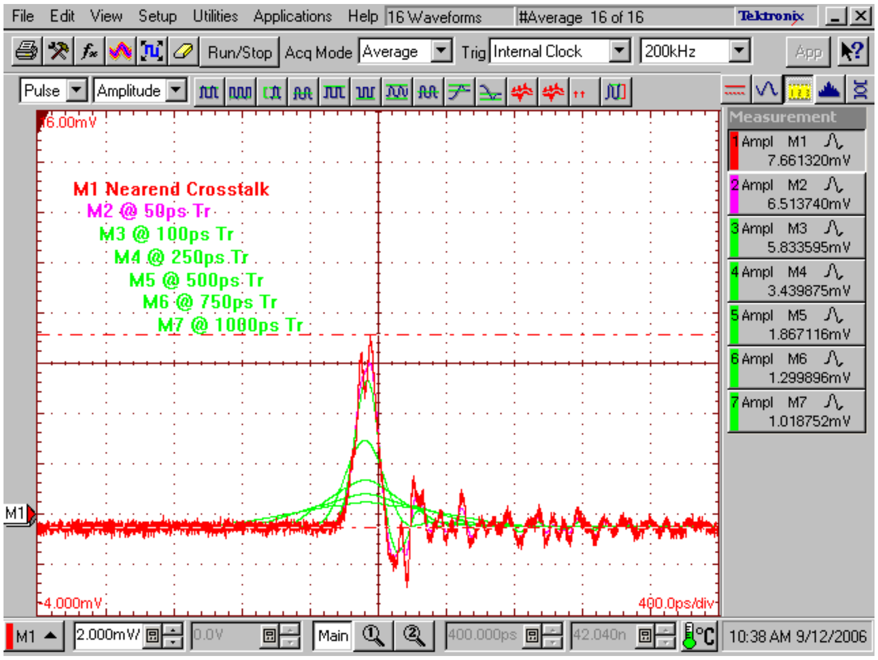


Single-Ended Application – FEXT, "Worst Case in Row" Configuration

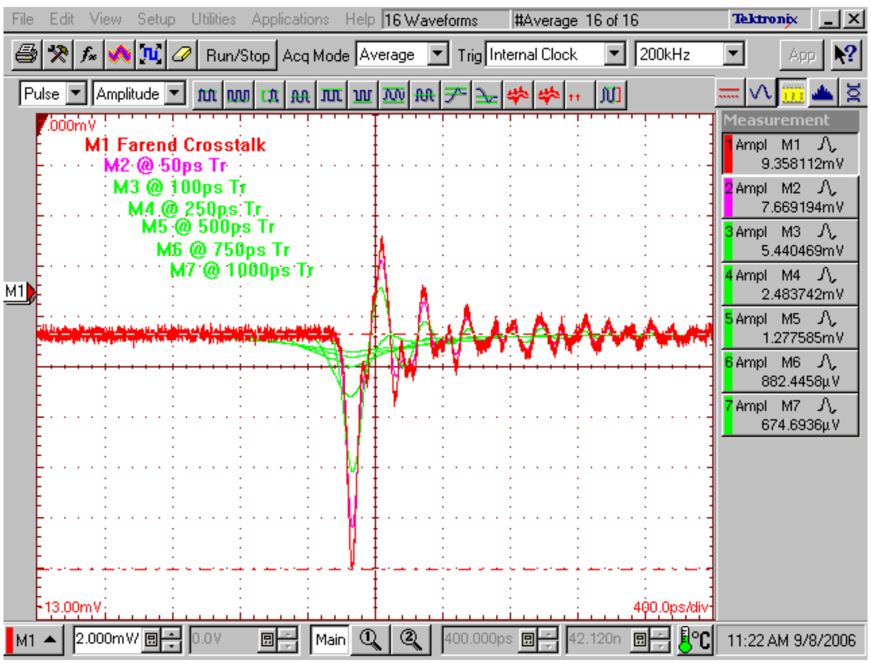


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – NEXT, "Best Case in Row" Configuration

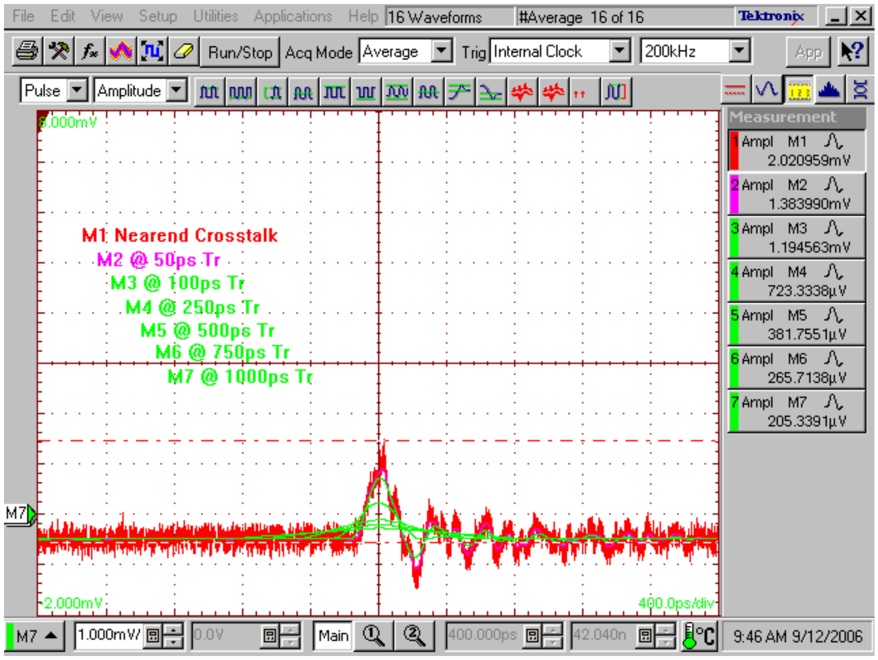


Single-Ended Application – FEXT, "Best Case in Row" Configuration

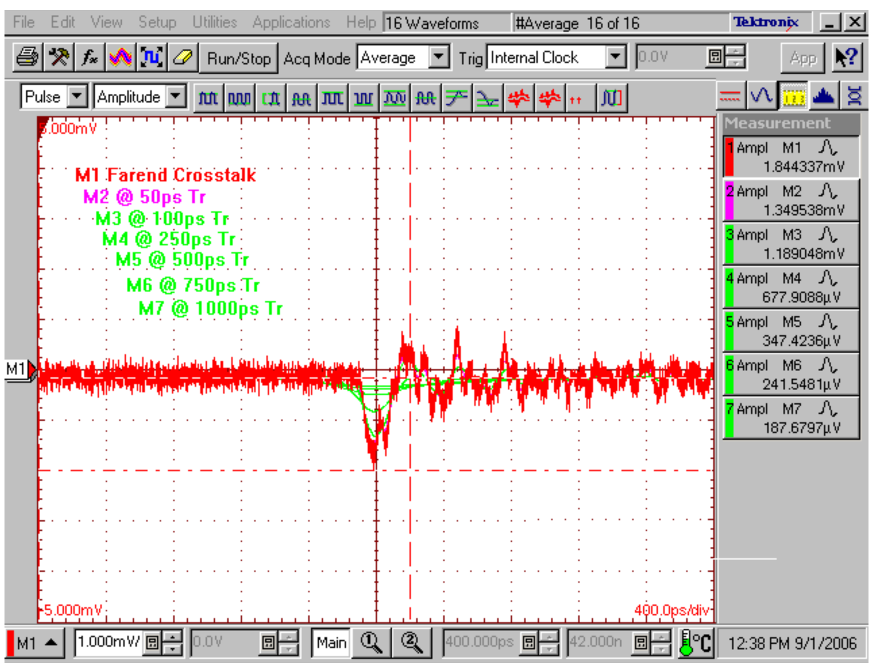


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – NEXT, "Across Row" Configuration

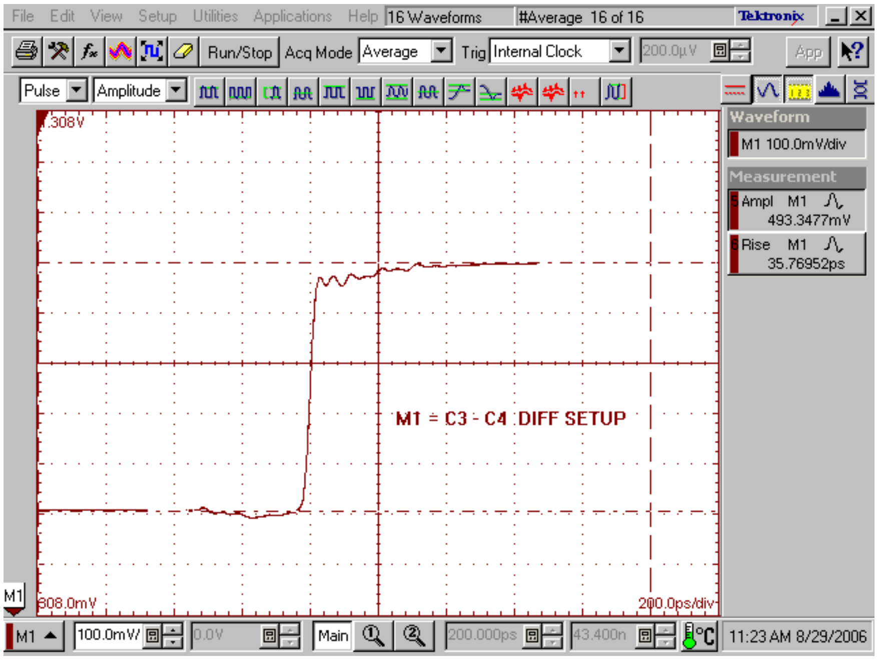


Single-Ended Application – FEXT, "Across Row" Configuration



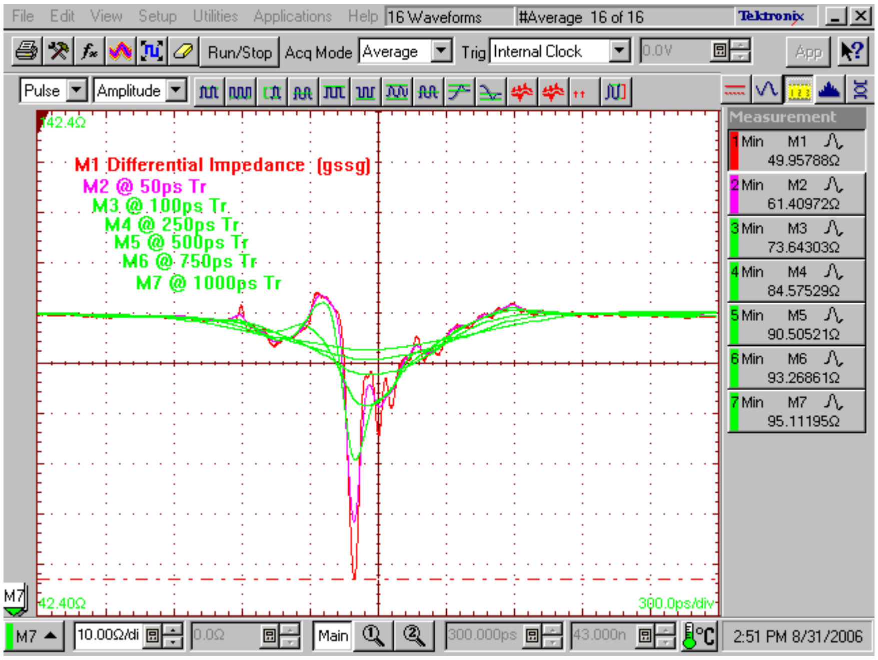
Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Differential Application – Input Pulse

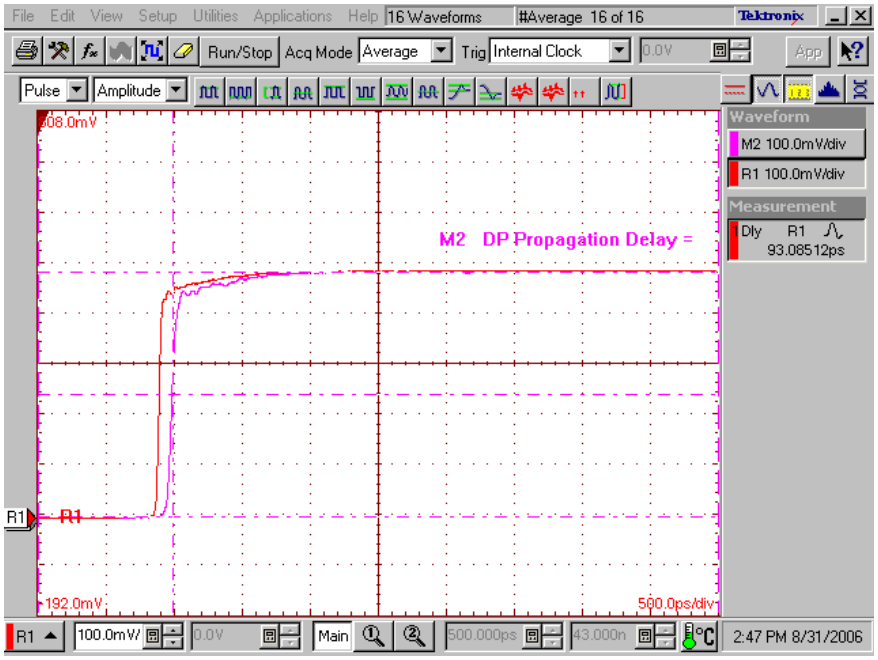


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Differential Application – Impedance

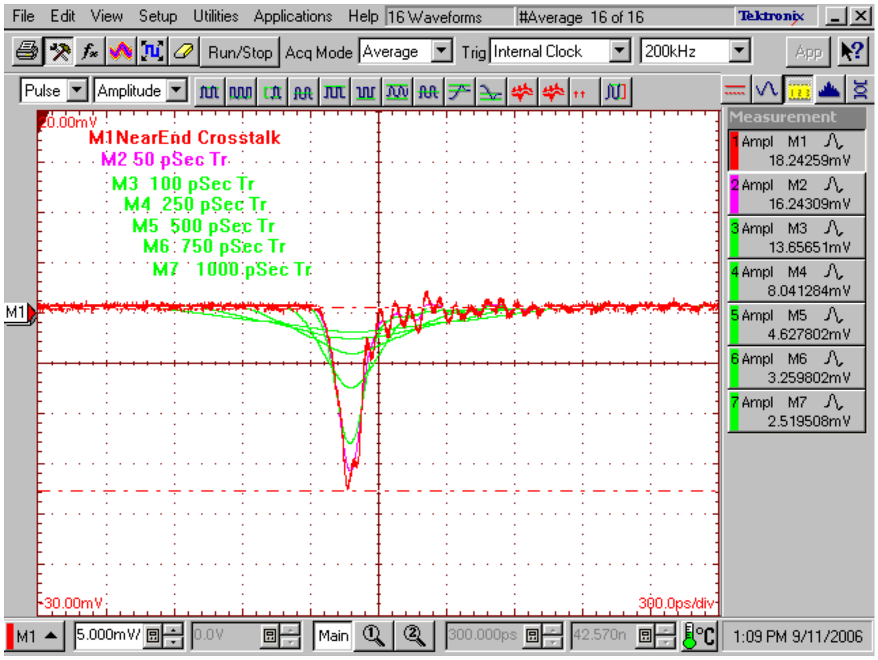


Differential Application – Propagation Delay

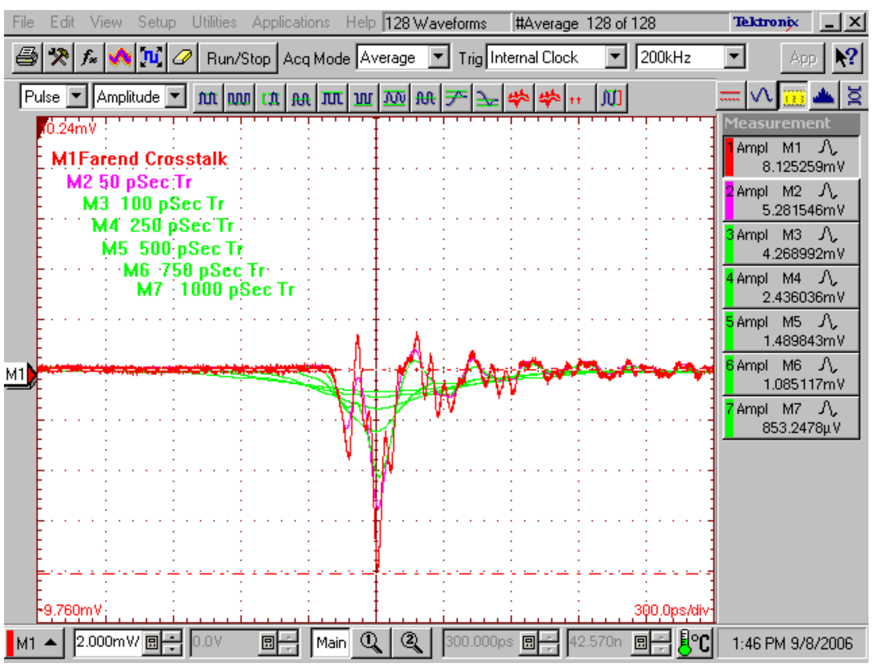


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Differential Application – NEXT, “Worst Case in Row” Configuration

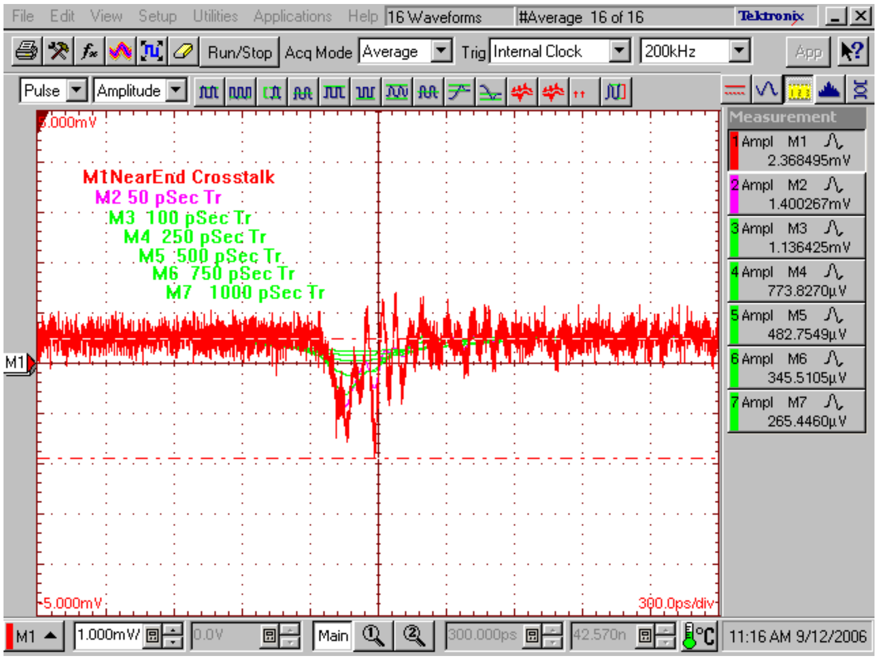


Differential Application – FEXT, “Worst Case in Row” Configuration

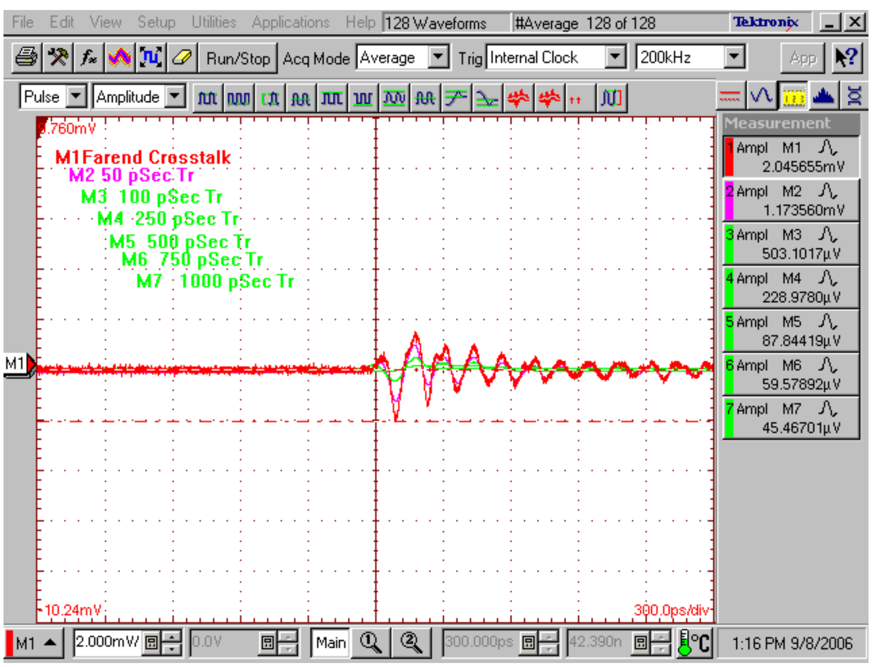


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Differential Application – NEXT, "Best Case in Row" Configuration

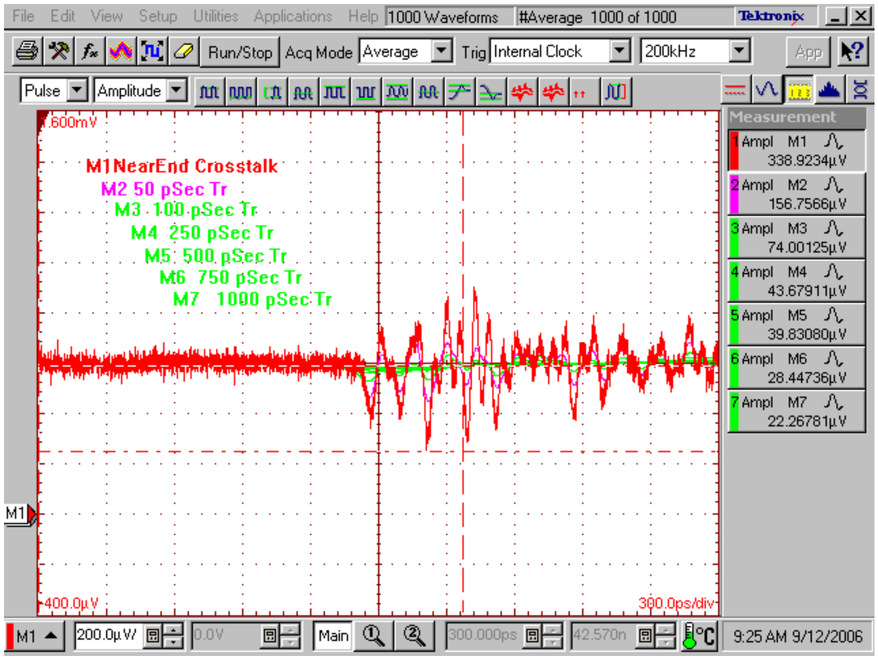


Differential Application – FEXT, "Best Case in Row" Configuration

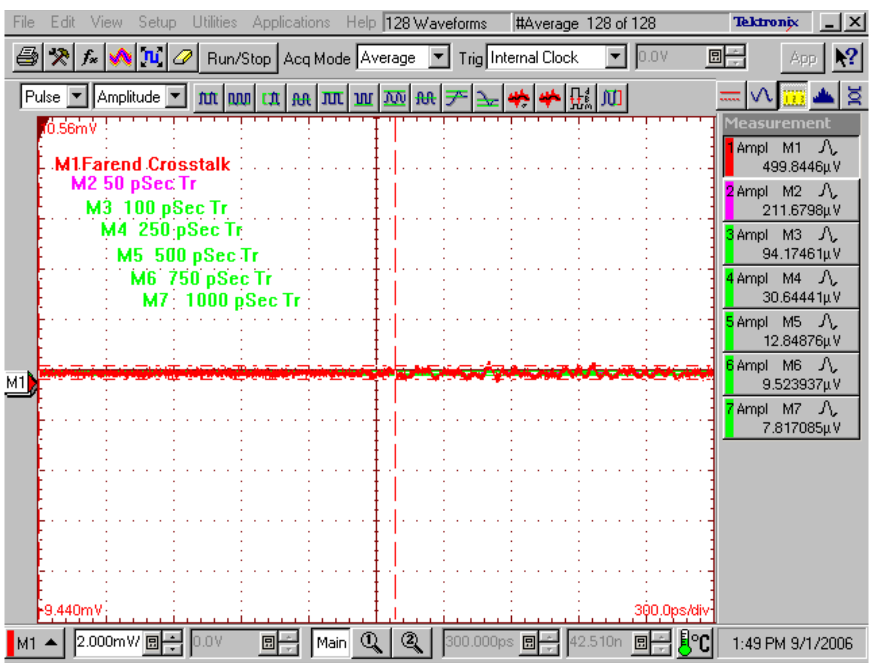


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Differential Application – NEXT, "Across Row" Configuration



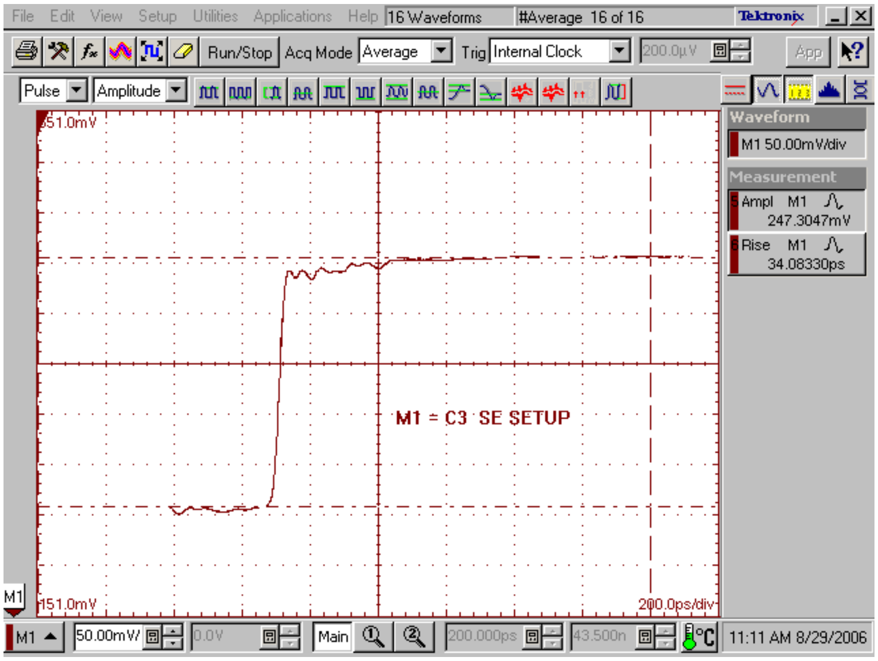
Differential Application – FEXT, "Across Row" Configuration



Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

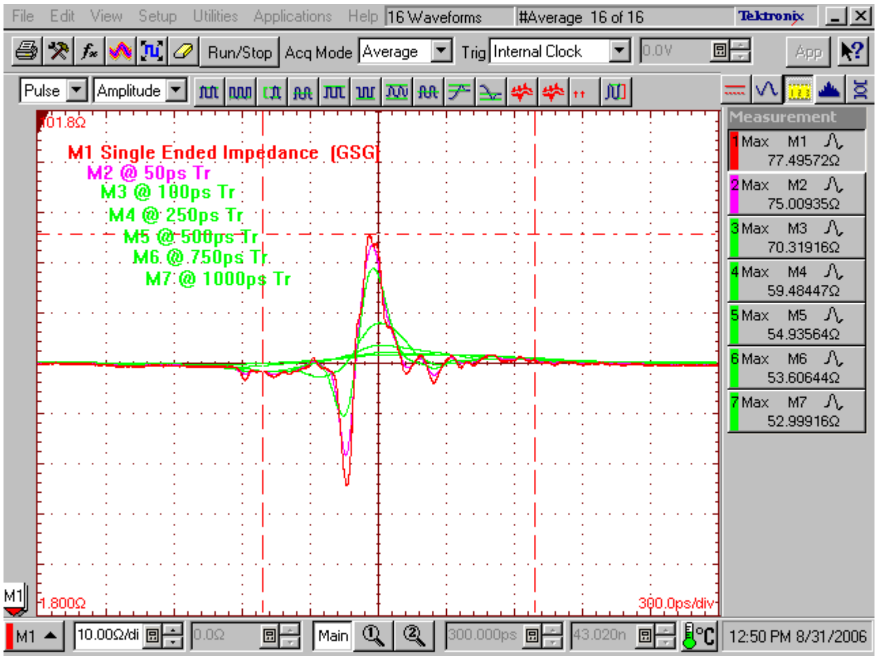
Appendix D – Time Domain Response Graphs *(Row 2 - Outer)*

Single-Ended Application – Input Pulse

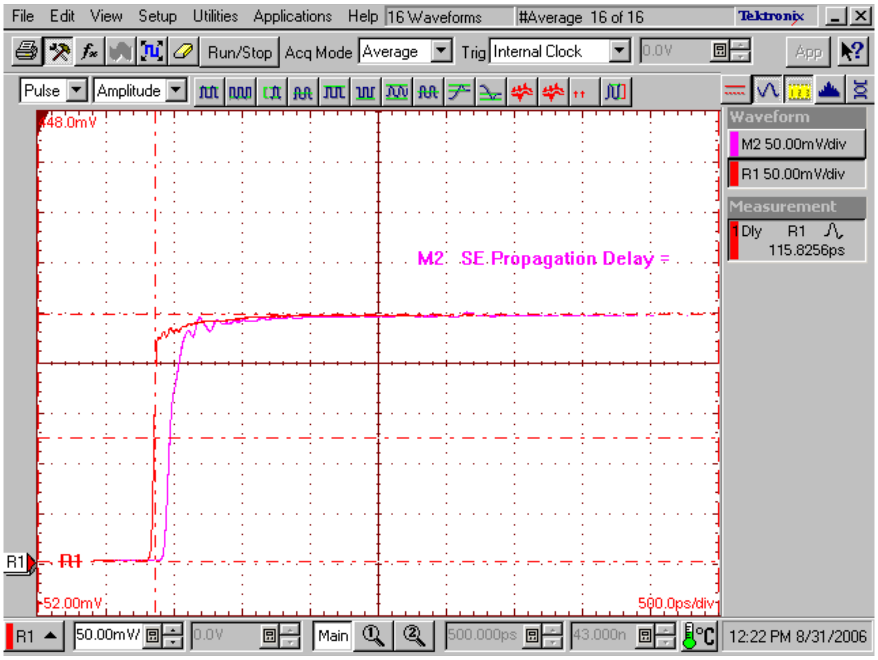


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – Impedance

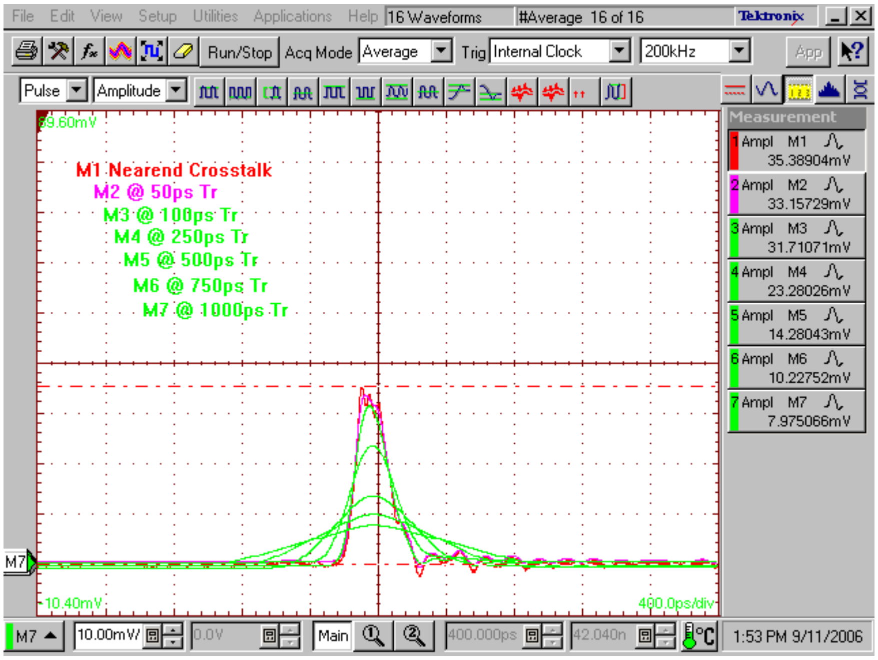


Single-Ended Application – Propagation Delay

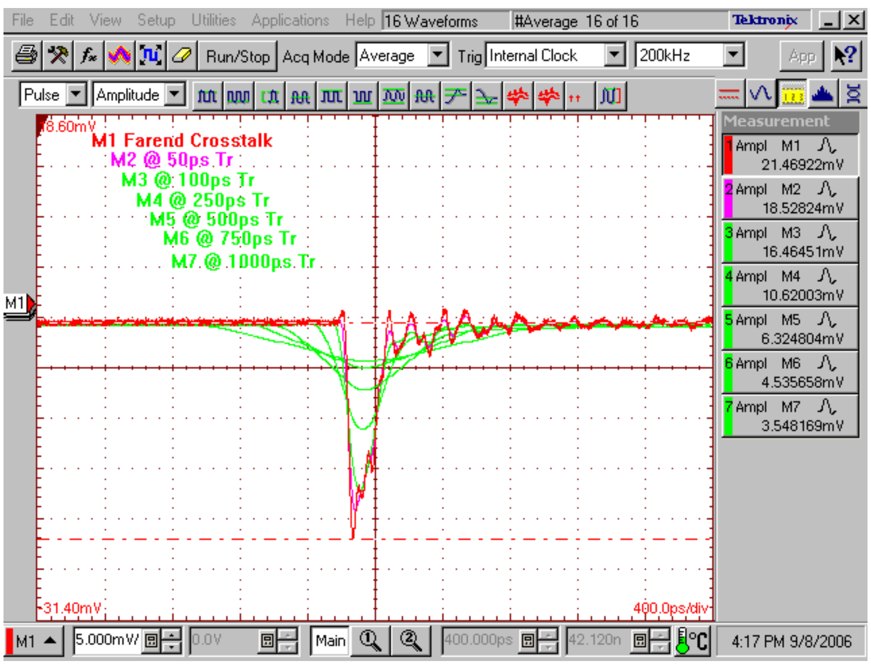


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – NEXT, "Worst Case in Row" Configuration

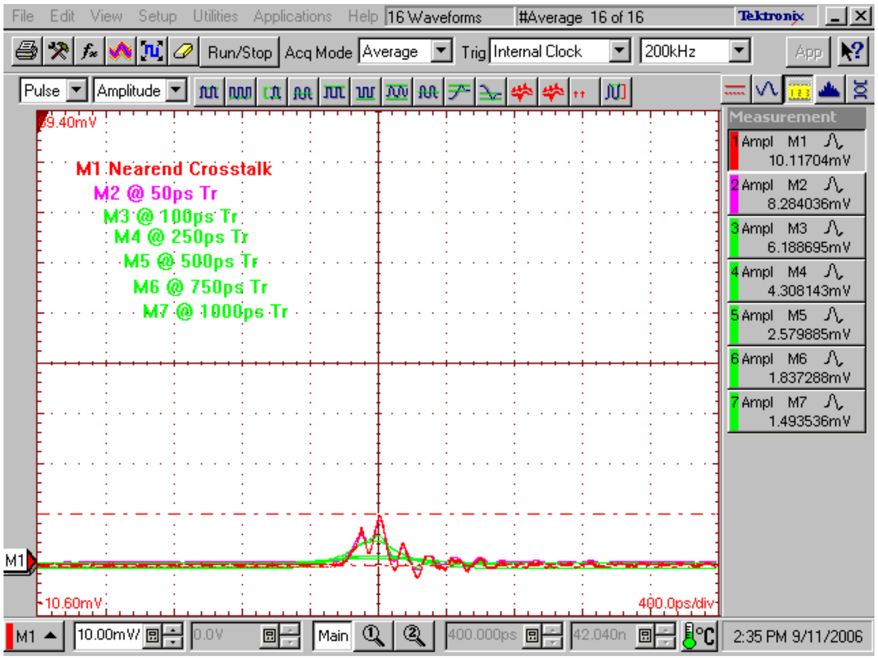


Single-Ended Application – FEXT, "Worst Case in Row" Configuration

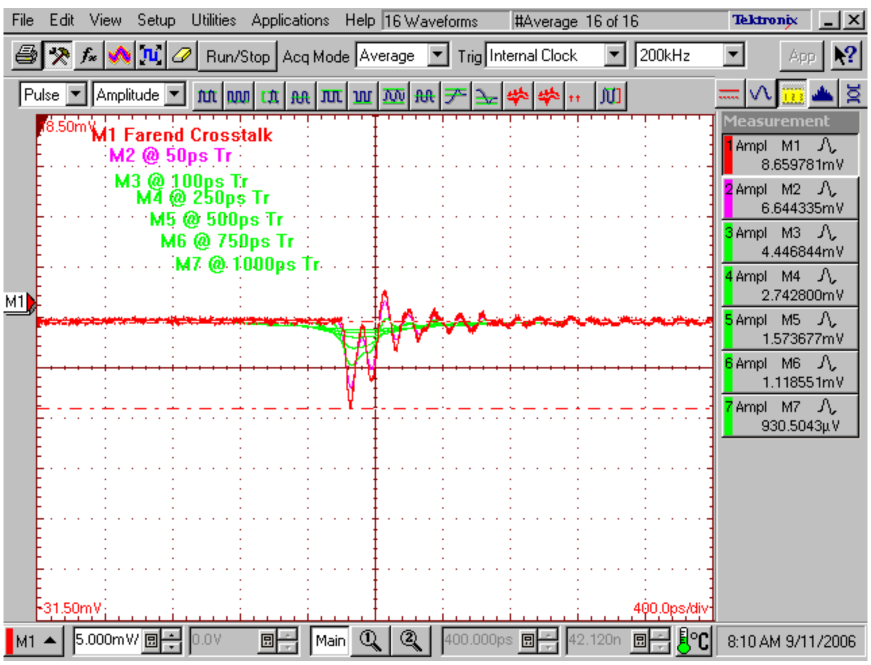


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Single-Ended Application – NEXT, "Best Case in Row" Configuration



Single-Ended Application – FEXT, "Best Case in Row" Configuration



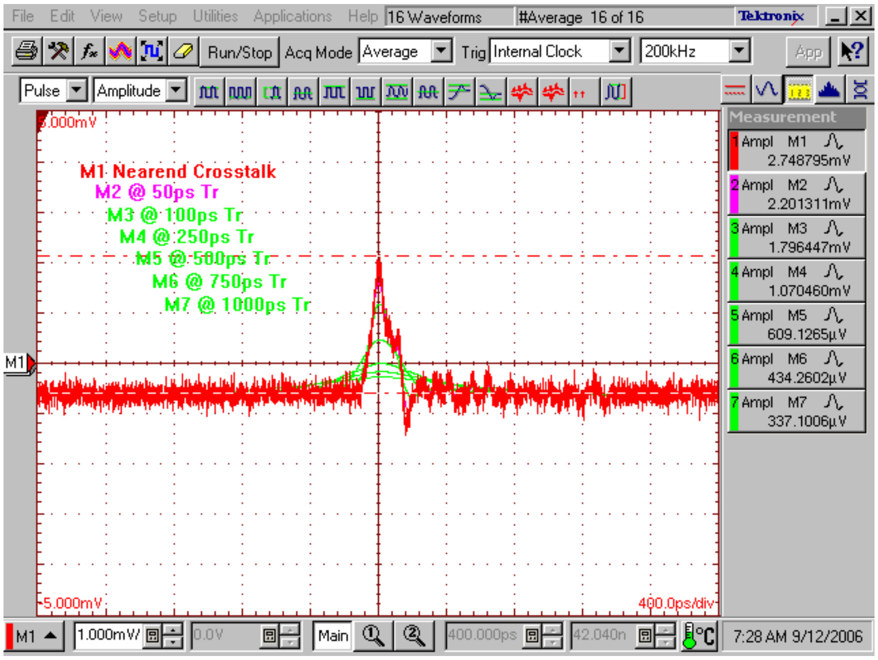
Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

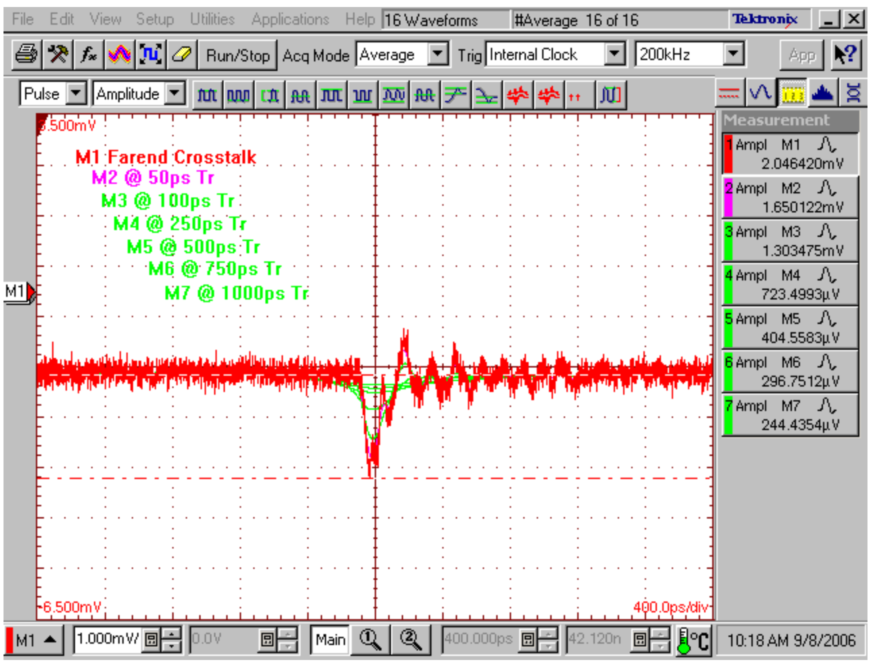
Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 10/3/2006

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Single-Ended Application – NEXT, “Across Row” Configuration

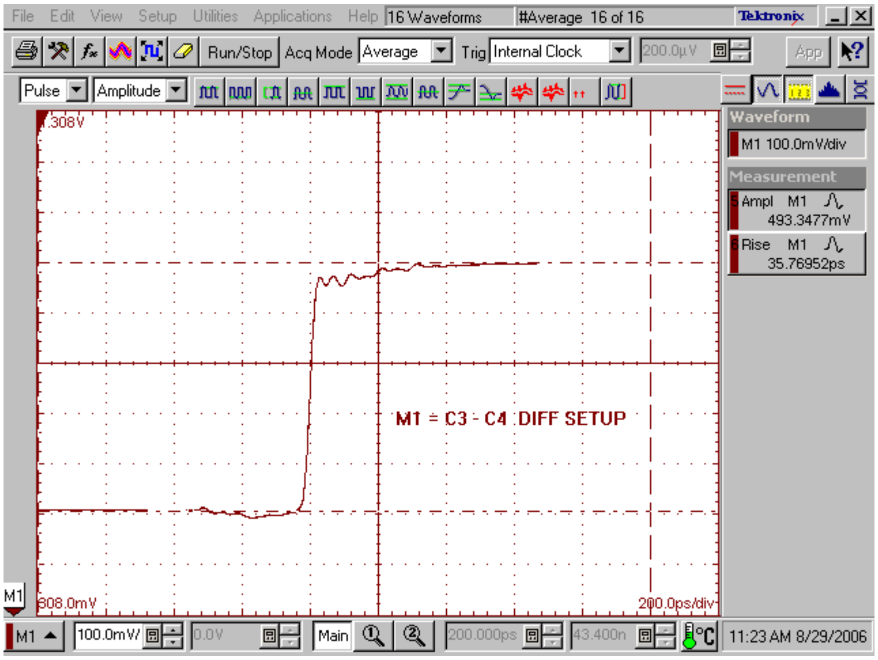


Single-Ended Application – FEXT, “Across Row” Configuration



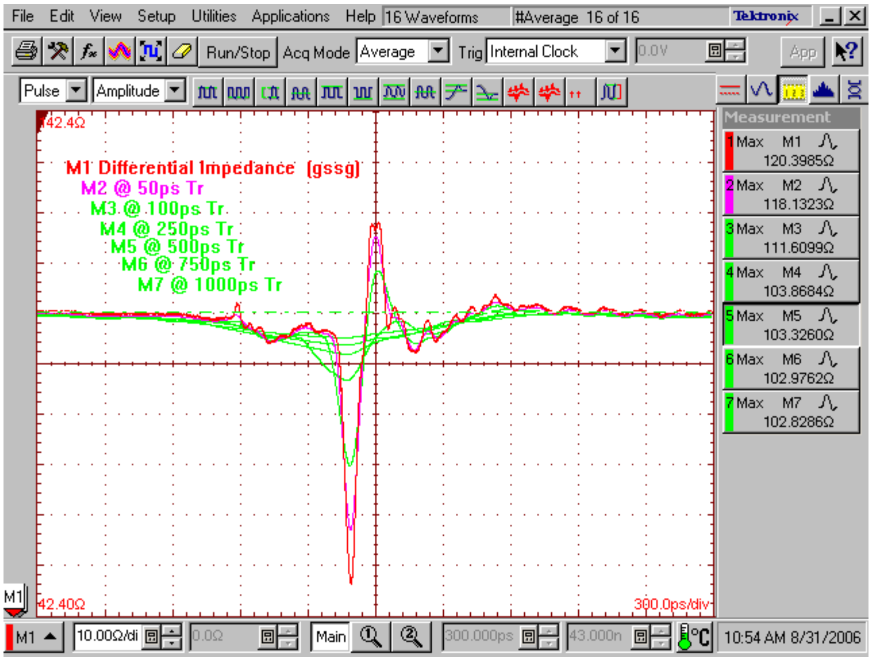
Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Differential Application – Input Pulse

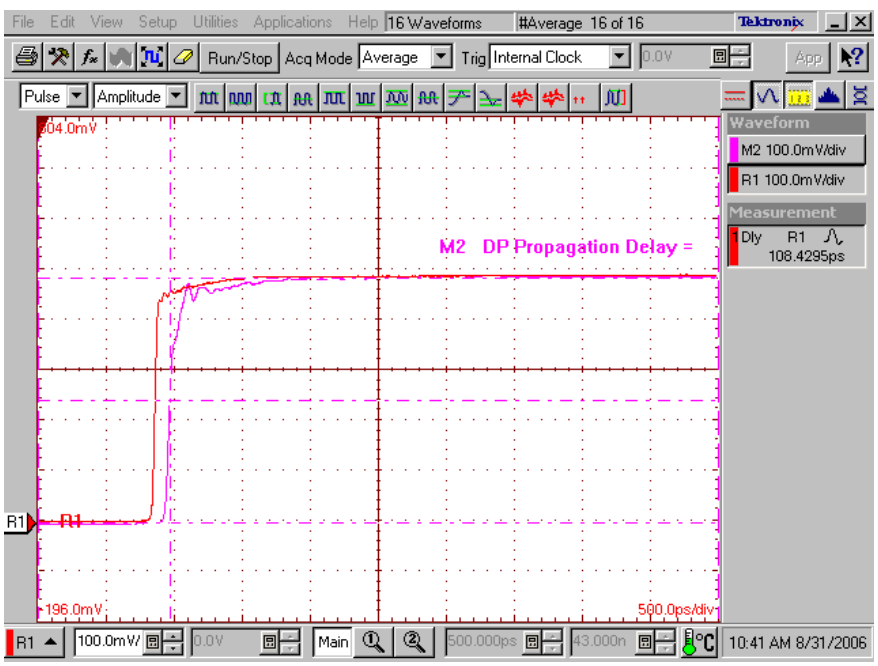


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Differential Application – Impedance



Differential Application – Propagation Delay



Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
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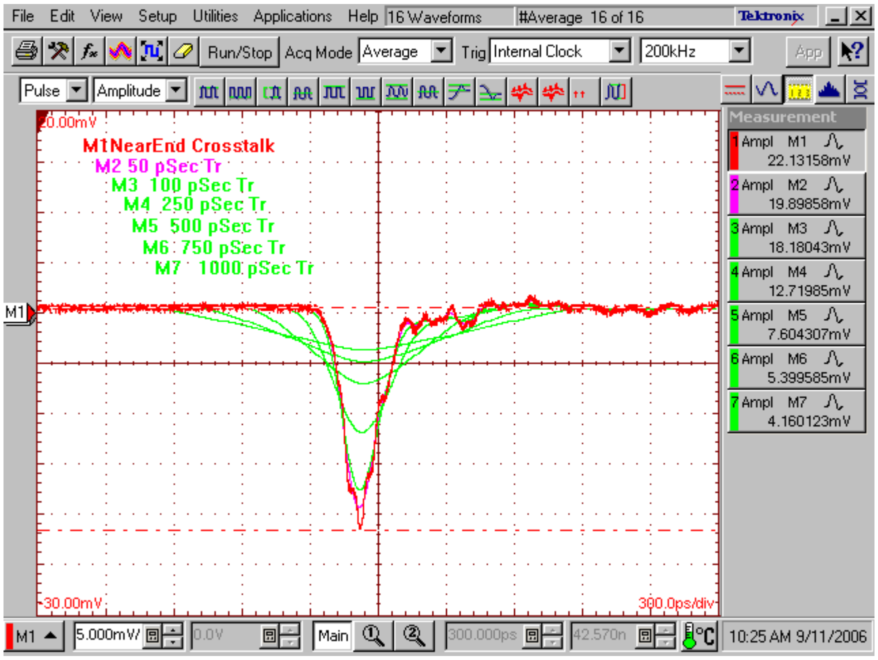
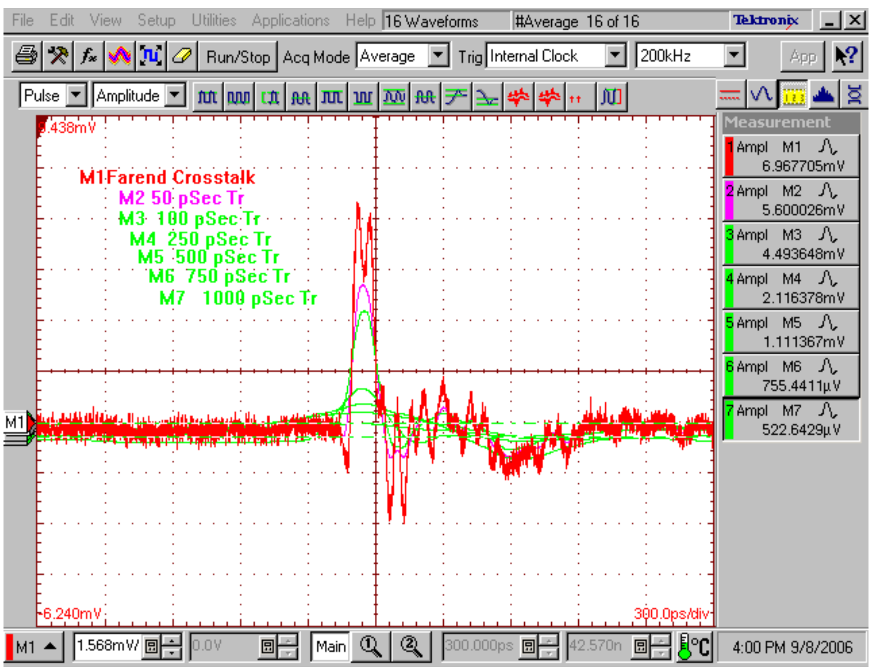
Differential Application – NEXT, "Worst Case in Row" Configuration

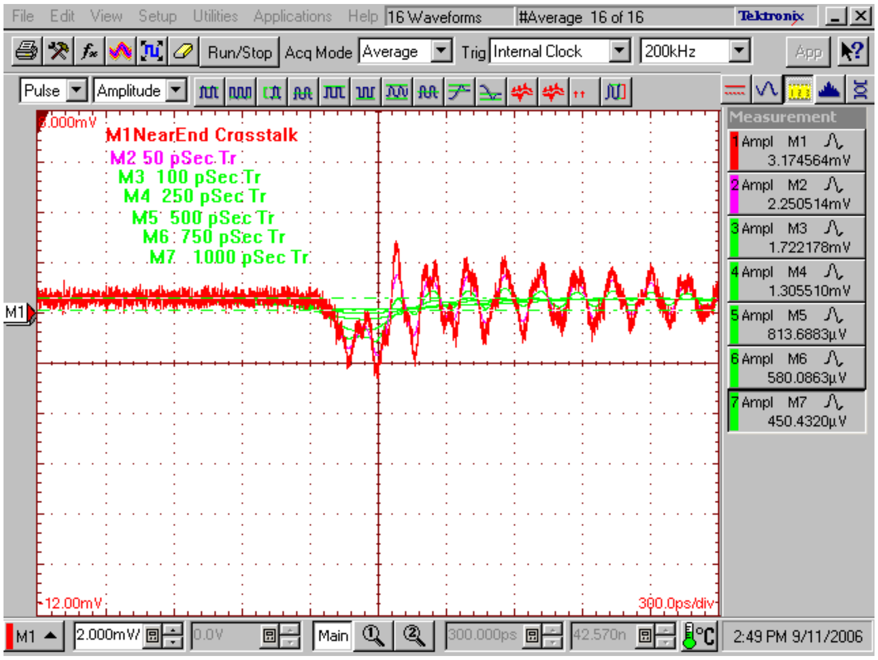


Differential Application – FEXT, "Worst Case in Row" Configuration

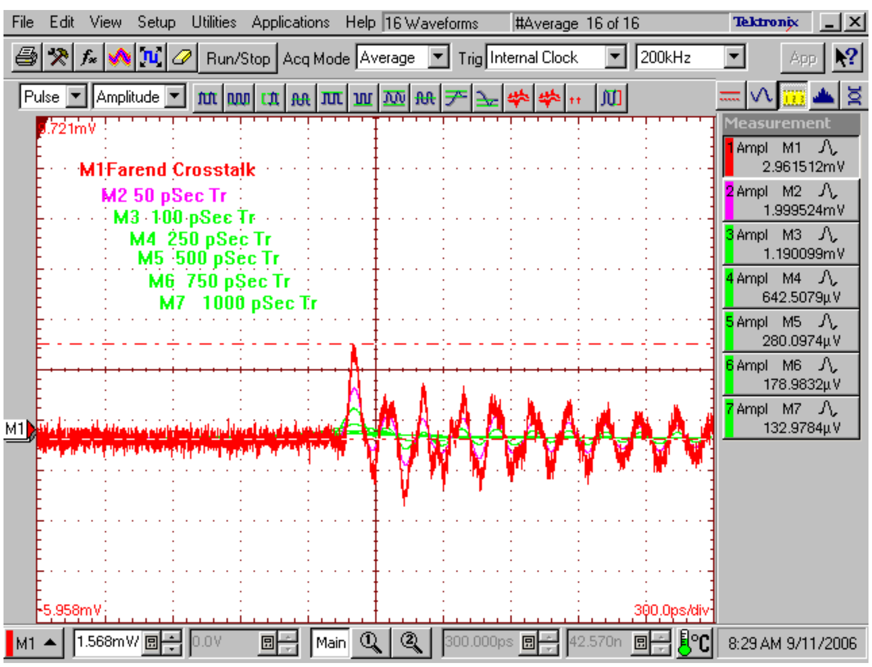


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Differential Application – NEXT, "Best Case in Row" Configuration

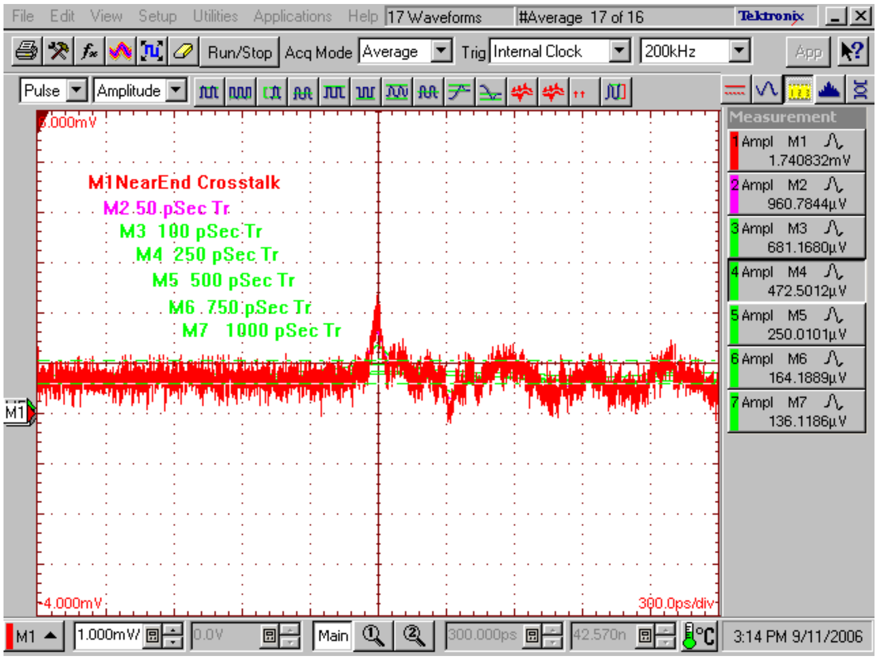


Differential Application – FEXT, "Best Case in Row" Configuration

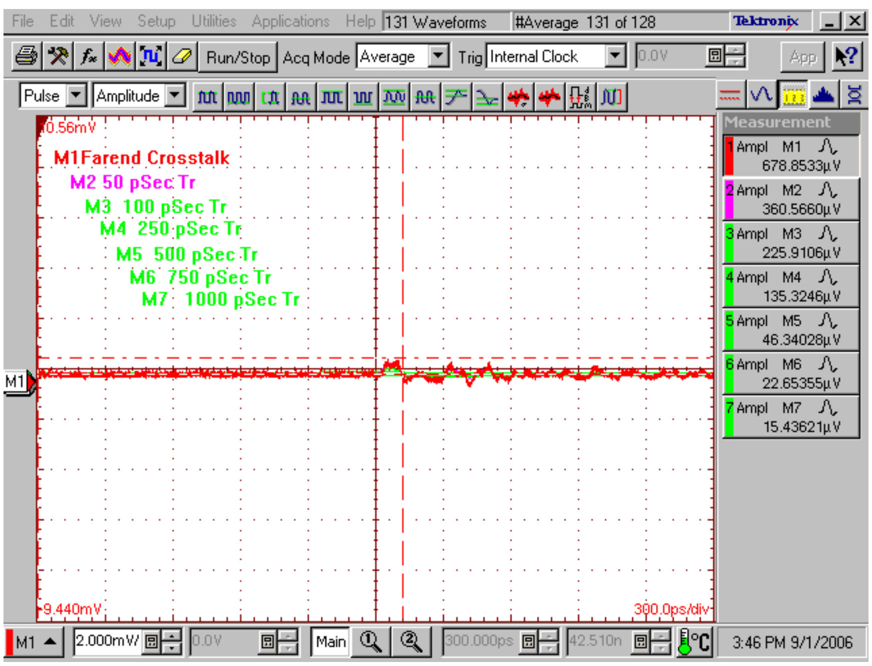


Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Differential Application – NEXT, “Across Row” Configuration



Differential Application – FEXT, “Across Row” Configuration



Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Appendix E– Product and Test System Descriptions

Product Description

The product sample is a 1.0mm pitch double row right angle mount socket connector. The structure is comprised of two banks of short & long right angle surface mount terminals (Figure 1). Short and long signal paths are identified as row 1 and row 2 respectively (Figure 2). MEC1-150-02-L-D-RA1 houses 40 signal paths in one bank and 58 signal paths in the second bank. The 1.0mm pitch mating edge-card is a test specific microprobe dual signal configuration launch.

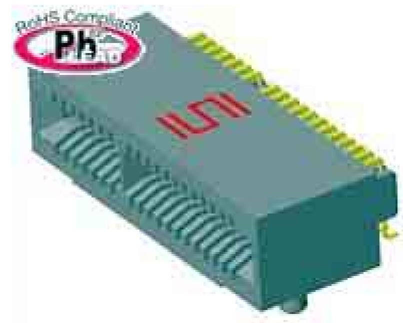


Figure 1 1mm Body Structure

Test System Description

The test fixtures are composed of a 4-layer FR-4 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. Since the double row right angle connector is not homogeneous as most Samtec micro product, it presents both mechanical signal routing design difficulties and incongruous electrical properties between rows. For this testing mechanical difficulties are overcome by creating two connector fixtures, one routing shorter path row 1 signals to the opposite side of the test board through vias while Row 2 longer path signals remained same side throughout. However, in order to test the short path signals the connector fixture is oriented in an upside down position necessitating the edge-card be designed to this orientation. Electrically results from both short and long electrical paths are reported.

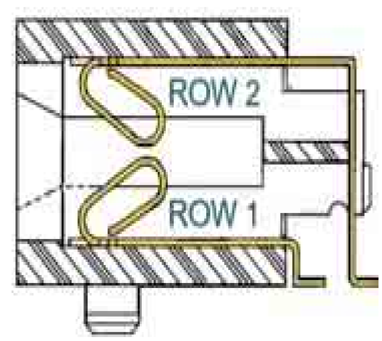


Figure 2 Terminal Structures

Connector and edge-card fixtures for characterization are identified by Samtec part number PCB-100559-TST. The succeeding labels following the part number identify the test parameters each fixtures can characterize. Connector fixture labels are CONN-SPBC, CONN-LPBC, CONN-SPWC and CONN-LPWC. "CONN" indicates the fixture is terminated with the connector under test. "LP" or "SP" defines whether a shorter or longer electrical path is under test. "BC" indicates the fixture (Figures 3 & 4) can be used to characterize single ended and differential signal types for impedance, propagation delay, best case crosstalk and across row crosstalk (XR) parameters. Fixtures des-

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

ignated with the "WC" label characterize the worst case crosstalk parameter only (Figures 5 & 6).

Figure 3 Short Path, Best Case Edge-Card & Connector Card

Figure 4 Long Path, Best Case Edge-Card & Connector Card

Figure 5 Short Path, Worst Case Edge-Card & Connector Card

Figure 6 Long Path, Worst Case Edge-Card & Connector Card

The edge.-card fixtures are dual terminal configurations utilized in mating to the signal paths of the worse case, best case or across row configurations of the socket fixtures. Edge-cards are also identified by PCB-100559-TST and succeeded by either suffix labels EDGE-SP or EDGE-LP.   EDGE-SP (short path) signal terminals mate with row one socket terminals. EDGE-LP (long path) signal terminals mate with row two socket

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terminals. Signals are launched from the edge card (RAEC1) side of the mated fixture. Data and waveforms presented in this report are results from the edge-card signal launch. Table 16 and 16 below identify the launch, monitoring, and adjacent line termination points used in generating characterization data for this report.

Characterization & Termination Matrix

Table 15 – PCB100559-TST Fixture (Long Path)

	Differential				Single Ended			
	Launch	Monitor	100Ω across Sig. Pair Termination		Launch	Monitor	50Ω to Gnd. Termination	
USE PCB	**EDGE-LP**	CONN-LPBC	EDGE-LP	CONN-LPBC	**EDGE-LP**	CONN-LPBC	EDGE-LP	CONN-LPBC
IL, RL Z, PD	J5	J34	J6 J7	J33 J35	J8	J36	J9 J10	J37 J38
FEXT (bc)	J5	J35	J6 J7	J33 J34	J8	J37	J9 J10	J36 J38
FEXT (xr)	J5	J33	J6 J7	J34 J35	J8	J38	J9 J10	J36 J37
USE PCB	**EDGE-LP**	**CONN -LPWC**	**EDGE-LP**	**CONN-LPWC**	**EDGE-LP**	**CONN-LPWC**	**EDGE-LP**	**CONN-LPWC**
FEXT (wc)	J4	J29	J3	J28	J2	J31	J1	J30
USE PCB	EDGE-LP	EDGE-LP	EDGE-LP	CONN-LPWC	EDGE-LP	EDGE-LP	EDGE-LP	CONN-LPWC
NEXT (wc)	J4	J3		J28 J29	J2	J1		J30 J31
USE PCB	EDGE-LP	EDGE-LP	EDGE-LP	CONN-LPBC	EDGE-LP	EDGE-LP	EDGE-LP	CONN-LPBC
NEXT (bc)	J5	J6	J7	J33 J34 J35	J8	J9	J10	J36 J37 J38
NEXT (xr)	J5	J7	J6	J33 J34 J35	J8	J10	J9	J36 J37 J38

Samtec Inc.
520 Park East Blvd.
New Albany IN 47151-1147 USA

WWW.SAMTEC.COM
1-800-SAMTEC-9 (US & Canada)
SIG@samtec.com

Phone: 812-944-6733
Fax: 812-948-5047
Report Revision: 10/3/2006

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

Table 16 – PCB100559-TST Fixture (Short Path)								
	Single Ended				**Differential**			
	Launch	Monitor	50Ω to Gnd. Termination		Launch	Monitor	100Ω across Sig. Pair Termination	
USE PCB	**EDGE-SP**	CONN-SPBC	EDGE-SP	CONN-SPBC	**EDGE-SP**	CONN-SPBC	EDGE-SP	CONN-SPBC
IL, RL Z, PD	J20	J52	J18 J19	J53 J54	J17	J55	J15 J16	J53 J54
FEXT (bc)	J20	J54	J18 J19	J37 J38		J57	J15 J16	J55 J56
FEXT (xr)	J20	J53	J18 J19	J52 J54	J17	J56	J15 J16	J55 J57
USE PCB	**EDGE-SP**	**CONN-SPWC**	**EDGE-SP**	**CONN-SPWC**	**EDGE-SP**	**CONN -SPWC**	**EDGE-SP**	**CONN-LPWC**
FEXT (wc)	J11	J48	J12	J47	J13	J50	J14	J49
USE PCB	EDGE-SP	EDGE-SP	EDGE-SP	CONN-SPWC	EDGE-SP	EDGE-SP	EDGE-SP	CONN-SPWC
NEXT (wc)	J11	J12		J47 J48	J13	J14		J49 J50
USE PCB	EDGE-SP	EDGE-SP	EDGE-SP	CONN-SPBC	EDGE-SP	EDGE-SP	EDGE-SP	CONN-SPBC
NEXT (bc)	J20	J19	J18	J52 J53 J54	J17	J15	J16	J55 J56 J57
NEXT (xr)	J20	J18	J19	J52 J53 J54	J17	J16	J15	J55 J56 J57

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Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Printed Circuit Board Edge Card & Connector Card Signal Layouts

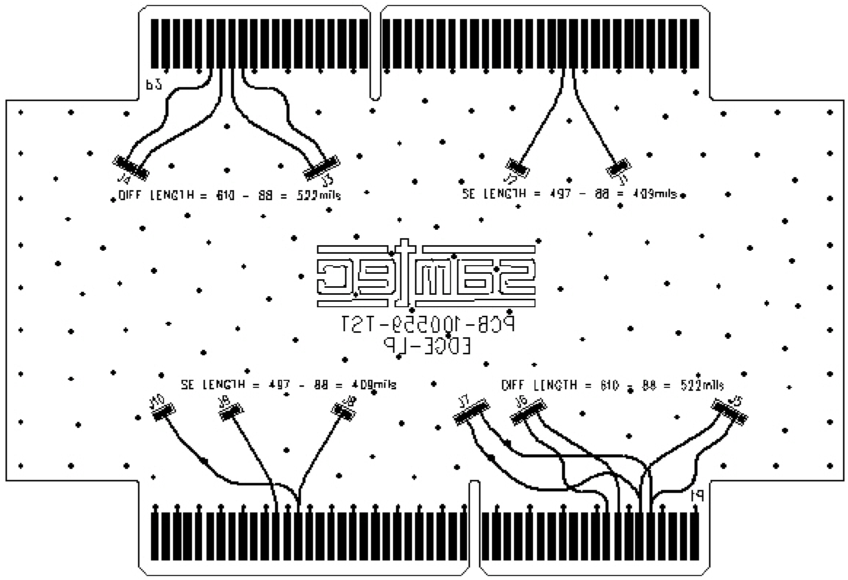

Figure 7 PCB-100559-TST, EDGE-LP, Dual Configuration Edge-Card Fixture Used for All Long Signal Path Measurements

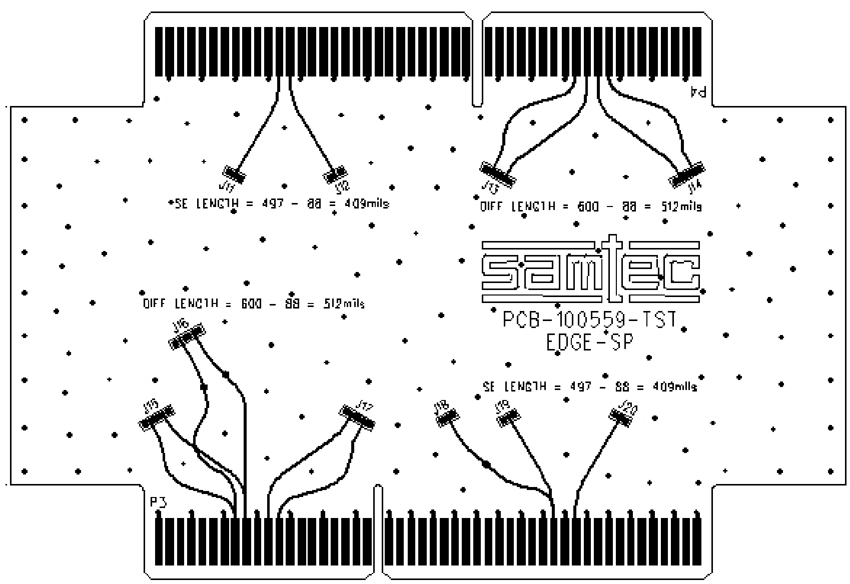

Figure 8 PCB-100559-TST, EDGE-SP, Dual Configuration Edge-Card Fixture Used for All Short Signal Path Measurements

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

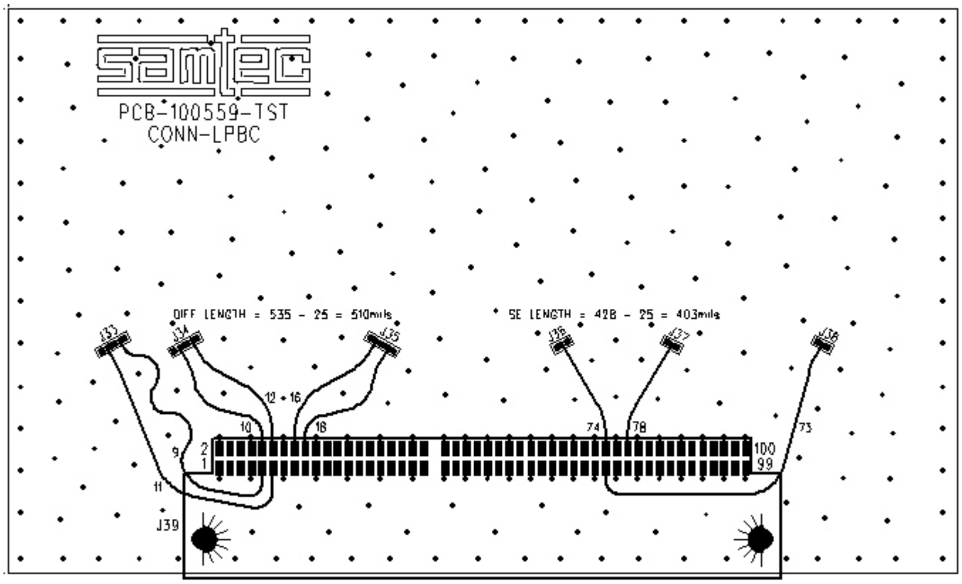

Figure 9 PCB-100559-TST CONN-LPBC, Long Signal Path Fixture for Z, PD, IL, RL, and Best Case & Across Row Time Based & RF Crosstalk Measurements

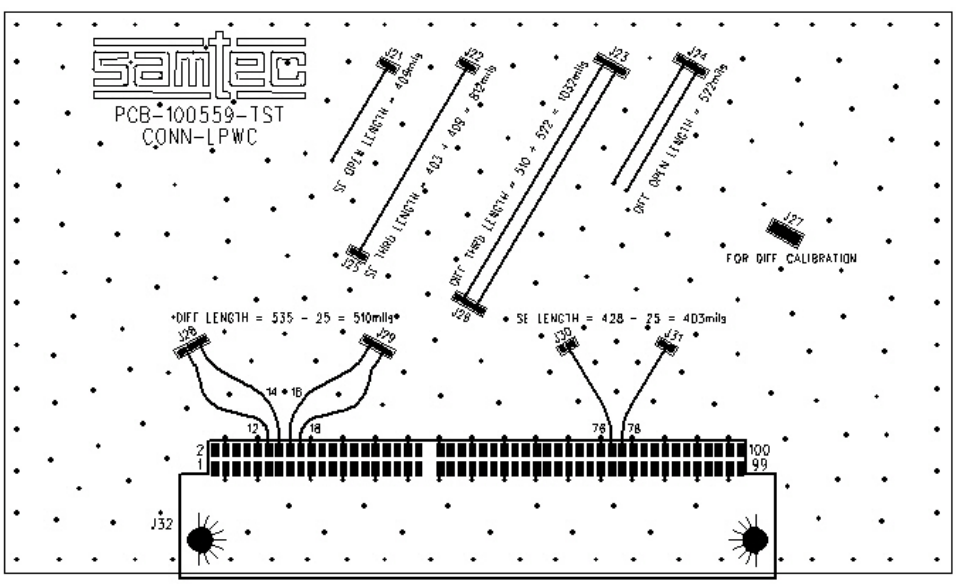

Figure 10 PCB-100559-TST, CONN-LPWC, Long Signal Path Fixture for Time Based & RF Worst Case Crosstalk Measurements Only

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937") Pitch, Mates w/ 1.60mm (.062") cards

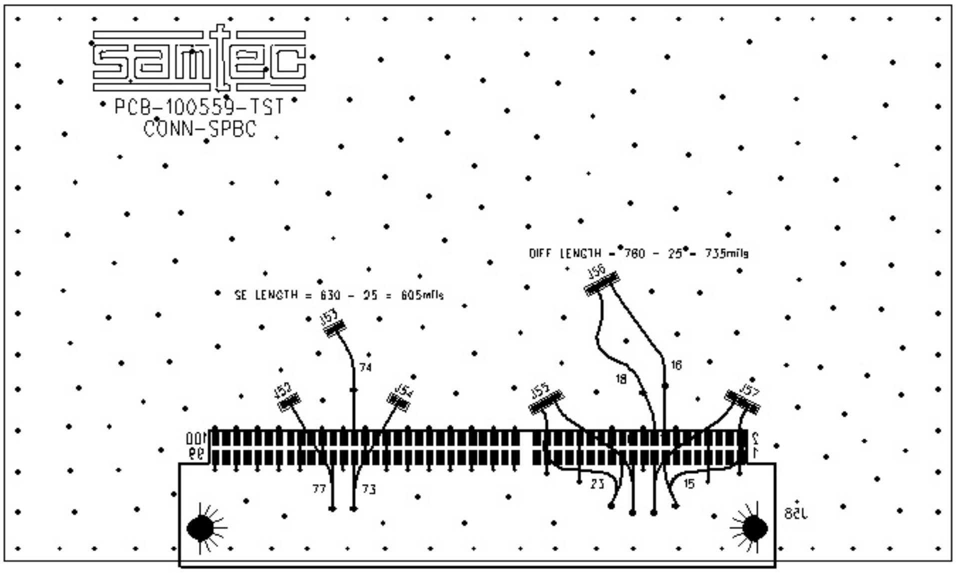

Figure 11 PCB-100559-TST CONN-SPBC, Long Signal Path Fixture for Z, PD, IL, RL, and Best Case & Across Row Time Based & RF Crosstalk Measurements

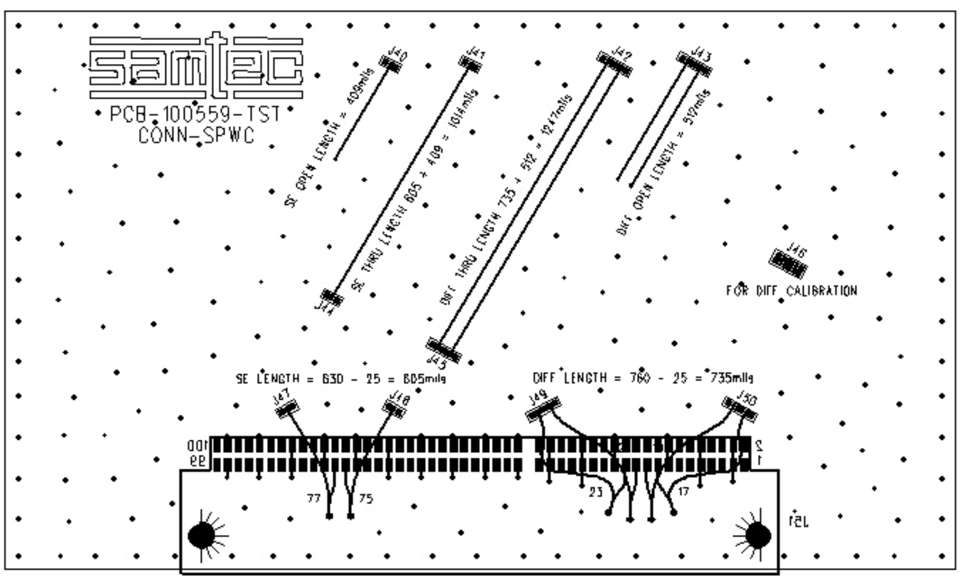

Figure 12 PCB-100559-TST, CONN-SPWC, Short Signal Path Fixture for Time Based & RF Worst Case Crosstalk Measurements Only

Series: MEC1- RA1 Series
Description: Right Angle Body Style, 1.0mm (.03937”) Pitch, Mates w/ 1.60mm (.062”) cards

Appendix F – Test and Measurement Setup

The test instrument is the Tektronix CSA8000 Communication Signal Analyzer Mainframe. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. Time domain results are generated using the TDR/Sampling Head capability. S-parameter data is generated from a TDR based software tool called I-Connect Probing is accomplished using a video microscopy system, microprobe positioners, and 40GHz capable microprobes. The 450 micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a ≥18 dB return loss, and an isolation of 38 dB providing high-bandwidth and low parasitic measurement results. Combined, the above technology provides a stable measurement environment along with the electrical accuracies for obtaining precise calibrations and signal launch capabilities (Figures 13 & 14).

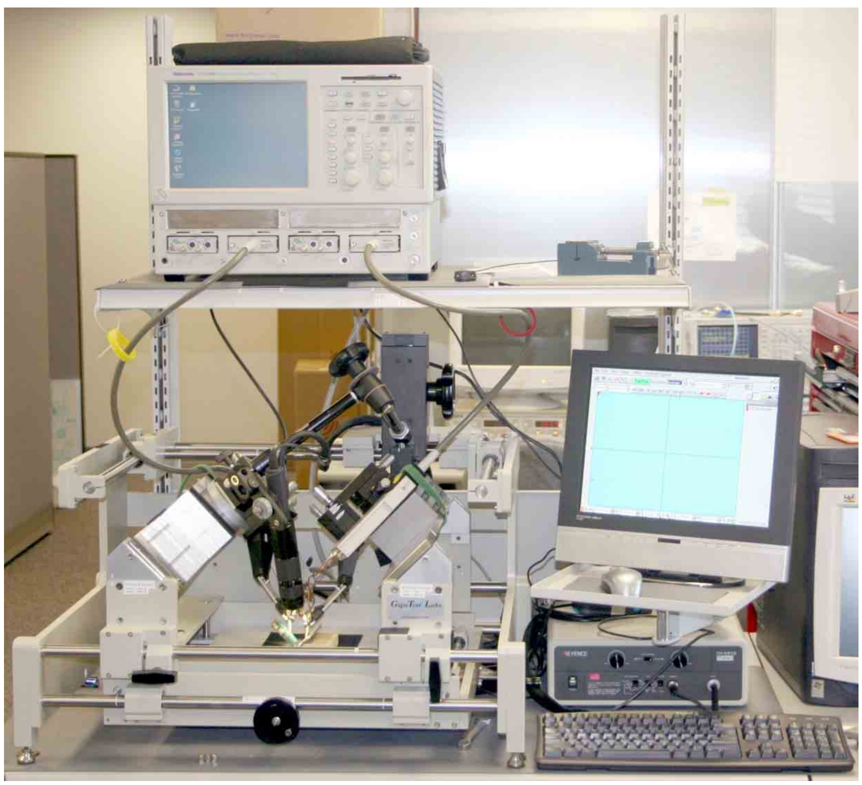

Figure 13 Measurement Station Capability
Horizontal Plane or 45˚ Probing

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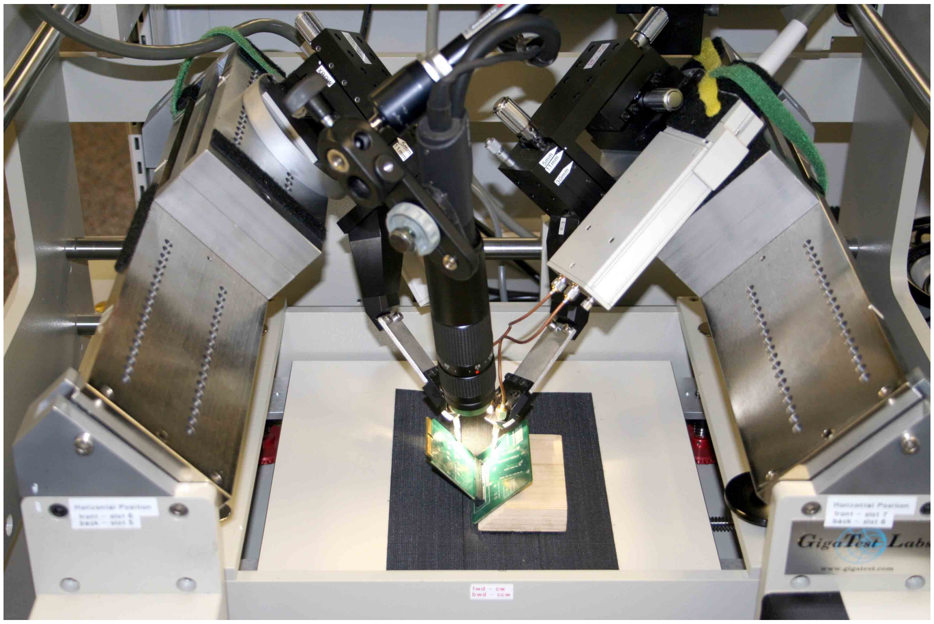

Figure 14 Dual 40 GHz Microprobes – Right Angle Orientation

Test Instruments

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
3	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Tektronix 80E03 Dual Channel 20 GHz Sampling Module

Measurement Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
2	Picoprobe by GGB Ind. Model 40A GSG (single ended applications)
2	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

QTY	Description
4	Pasternack Enterprises 2.9mm Semi-Rigid (.086) 6" Cable Assemblies
2	Tektronix 1 Meter Module Extenders

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Appendix G - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Related time and frequency test parameter data recorded for this report were gathered simultaneously.

Frequency (S-Parameter) Domain Procedures
Frequency data extraction involves two steps that first measure the frequency related time domain waveform followed by post-processing of the time domain waveforms into loss and crosstalk response parameters versus frequency. The first step utilizes the Tektronix CSA8000 time based instrument to capture frequency related single-ended or differential signal types propagating through an appropriately prepared SUT. The second step involves a correlation of the time based waveforms using the TDA Systems IConnect software tool to post-process these waveforms into frequency response parameters. TDA Systems labels these frequency related waveform relationships as the *Step* and *DUT* reference. This report establishes the setup procedures for defining the *Step* and *DUT* reference for frequency parameters of interest. Once established, the *Step* and *DUT* references are post-processed in IConnect’s S-parameter computations window.

CSA8000 Setup
Listed below is the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. These frequency boundaries are determined by a time domain instruments functional settings such as window length, number of points and averaging capability. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process.

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	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 16	≥ 16

Insertion Loss
SUT Preparation - For signal launch and monitoring path guidelines reference table 15 or 16, dependent on signal row being characterized. Terminate all the active or adjacent signal lines at the impedance value recommended. Verify the appropriate signal type and test parameter path using PCB signal layout schematics (Figures 7 through 12).

Step Reference - Establish waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. A transmission path is completed by inserting a negligible length of transmission standard between the homogeneous probes. To characterize the **thru** standard for I-Connect post-processing of a transmission parameter, use either of the "FOR DIFF CALIBRATION" standards fabricated onto PCB-100559-TST, CONN-SPWC or CONN-LPWC. The calibration standard is employed in both single ended and differential signaling (Figure 10 & 12).

DUT Reference - Establish waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the **SUT** between the probes in place of the transmission standard and record the measurement.

Return Loss
SUT Preparation – For signal launch and monitoring path guidelines reference table 15 or 16, dependent on signal row being characterized. Terminate all the active or adjacent signal lines at the impedance value recommended. Verify the appropriate signal type and test parameter path using PCB signal layout schematics (Figures 7 through 12).

Step Reference – Establish waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an **open** standard. To characterize the open standard for I-Connect post-processing of a reflection parameter, employ either of the "FOR DIFF CALIBRATION" standards fabricated onto PCB-100559-TST, CONN-SPWC or CONN-

LPWC. The calibration standard is employed in both single ended and differential signaling (Figure 10 & 12).

DUT Reference – Retain same signal path and test setup used in obtaining insertion loss waveforms. Create waveform by making a TDT (matched) reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. For this condition hi-Speed quality cables and adapters located on the far-end of the inserted SUT serve as the resistive load impedance. The load impedance should closely match that of the test system impedance of 50Ω single-ended and/or 100Ω differential.

Near-End Crosstalk (NEXT)
SUT Preparation – For signal launch and monitoring path guideline reference table 15 or 16, dependent on signal row being characterized. Terminate all active or adjacent signal lines at the impedance value recommended. Verify the appropriate signal type and test parameter path using PCB signal layout schematics (Figures 7 through 12).

Step Reference - Establish waveform by making an active measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an **open** standard. To characterize the open standard for I-Connect post-processing of the transmission parameter, use either of the "FOR DIFF CALIBRATION" standards fabricated onto PCB-100559-TST, CONN-SPWC or CONN-LPWC. The calibration standard is employed in both single ended and differential signaling (Figure 10 or 12).

DUT Reference - Establish waveform by driving the suggested signal line and monitoring the TDR coupled energy at the adjacent near-end signal line. Create 3 single ended & 3 differential short path waveforms and 3 single ended & 3 differential short path waveforms for worst case, best case and across row coupling conditions.

Far-End Crosstalk (FEXT)
SUT Preparation - For signal launch and monitoring path guideline reference table 15 or 16, dependent on signal row being characterized. Terminate all active or adjacent signal lines at the impedance value recommended. Verify the appropriate signal type and test parameter path using PCB signal layout schematics (Figures 7 through 12).

Step Reference - Establish waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. A transmission path is completed by inserting a negligible length of transmission standard between the homogeneous probes. To characterize the **thru** standard for I-Connect post-processing of a transmission parameter, use either of the "FOR DIFF

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CALIBRATION" standards fabricated onto PCB-100559-TST, CONN-SPWC or CONN-LPWC. The calibration standard is employed in both single ended and differential signaling (Figure 10 or 12).

DUT Reference - Establish waveform by driving the suggested signal line and monitoring the TDR coupled energy at the adjacent near-end signal line. Create 3 single ended & 3 differential short path waveforms and 3 single ended & 3 differential short path waveforms for worst case, best case and across row coupling conditions.

Time Domain Procedures

Measurements involving digital type pulses are performed utilizing either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. For this series of tests, TDR methods are employed for the impedance and propagation delay measurements. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to accurately and fully characterize the SUT.

Impedance

The signal line(s) of the SUT's signal configuration is energized with a TDR pulse. The far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. For signal launch and monitoring path guidelines reference either table 15 or 16, dependent on signal type and connector row being characterized.

Propagation Delay

This test reports differential or single ended signal delay as the measured difference of propagation between a referenced length of the signal pads and signal traces (30 ± 5 ps edge rate) and the device under test (DUT) plus the electrical length of the signal pads and signal traces ($PD^{pads/traces}$- $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$). $PD^{pads/traces}$ is the referenced physical length of PCB signal pads & traces equal to the PCB pads & traces entering and leaving the device under test (DUT). These measurable reference *lengths {(i.e.; long path SE pads & traces = J22 to J25 & DIFF pads & traces = J23 to J26) (i.e.; short path SE pads & traces = J41 to J44 & DIFF pads & traces = J42 to J45)}* are featured on PCB100559-TST fixtures shown in figures 10 and 12. The PD^{DUT} + $PD^{pads/traces}$ variable is the mated MEC8-RA surface mount connector card with pads & traces plus the edge card with pads & signal traces. Both $PD^{pads/traces}$ & $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$ waveform edgerates are measured and recorded at 50 % amplitude of each recorded rising edge. The distance in time between the rising edges is the propagation delay of the device under test. For the MEC1-RA product there is present a short & long path propagation delay. Row 1 will be the shorter propagation delay, row 2 the longer delay (Figure 2). For signal launch and monitoring path guidelines reference either table 15 or 16, dependent on signal type and connector row being characterized.

Crosstalk

An active pulsed waveform is transmitted through a selected SUT signal line. The adjacent quiet signal lines are monitored for the coupled energy at the near-end and far-end. Active and quiet lines not being monitored are terminated in the test systems characteristic impedance. Signal lines adjacent to the quiet lines remain terminated on both ends throughout the test sequence. Failing to terminate the active near or far end, quiet lines, or in some cases, signal lines adjacent to the quiet line may have an effect on amplitude and shape of the coupled energy. Measure the worse and best case in row coupling scenarios. Also measure the direct coupling effects that occur across a row of terminals. For signal launch and monitoring path guidelines reference either table 15 or 16, dependent on signal type and connector row being characterized.

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Appendix H – Glossary of Terms

BC – Best Case Crosstalk Configuration
DP – Differential Pair signal configuration
DUT – Device Under Test, Term Used For TDA I-Connect & Propagation Delay Wave-forms
EC1 – Edge Card With A 1.0mm Pitch Between Signal Terminal Pads
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; Geometric Configuration
LEC8 – Signal Launch Edge Card With A .8mm Signal Pad Pitch
RAEC1- 1.0mm Pitch Edge Card For Right Angle Socket Connector
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single Ended
SI – Signal Integrity
SUT – System Under Test
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case Crosstalk Configuration
$Xrow^{se}$ – Cross Ground/Power Bar Crosstalk, Single Ended Signal
$Xrow^{diff}$ – Cross Ground/Power Bar Crosstalk, Differential Signal
Z – Impedance (expressed in ohms)
THRU – Transmission Through a 2-Port or 4-Port Device to A Receiver