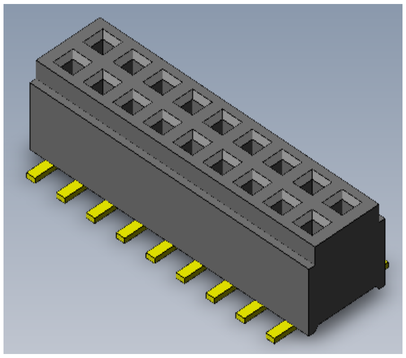
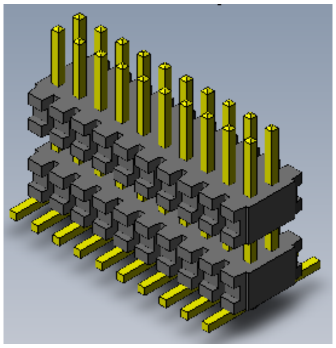
High Speed Characterization Report

CLM-1XX-02-X-D-X



Mates with

MW-XX-03-X-D-XXX-XXX-X



Description:

Surface Mount Board Stacker, 1.00mm Pitch, 8.48mm (0.334”) Stack Height

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Series: MW/CLM
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Connector Overview

Surface Mount Board Stacker series (MW) are capable of mating to SMT Micro Socket Strip series (CLM) and SMT Socket Strip series (MLE). MW and CLM are available with up to 100 pins. The mated connector achieves up to 100 I/Os with 8.48mm (0.334") stack height. The data in this report is applicable only to the MW mates to CLM.

Connector System Speed Rating

MW/CLM SMT Micro Strip, 1.00mm Pitch, 8.48 mm (0.334”) stack height

Signaling	Speed Rating
Single-Ended:	**5.5GHz/ 11Gbps**
Differential:	**9.5GHz/ 19Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded-up to the nearest half-GHz level. The up rounding corrects for a portion of the test board’s trace loss, since a short length of trace loss included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/ 15 Gbps.

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Frequency Domain Data Summary

Table 1 - Single-Ended Connector System Performance		
Test Parameter	**Configuration**	
Insertion Loss	GSG	-3dB@ 5.36GHz
Return Loss	GSG	-6.12dB@ 5.36GHz
Near-End Crosstalk	GAQG	-31.84dB@ 5.36GHz
	GAGQG	-18.24dB@ 5.36GHz
	Xrow, GAG to GQG	-15.33dB@ 5.36GHz
Far-End Crosstalk	GAQG	-14.25dB@ 5.36GHz
	GAGQG	-19.33dB@ 5.36GHz
	Xrow, GAG to GQG	-21.19dB@ 5.36GHz

Table 2 - Differential Connector System Performance		
Test Parameter	**Configuration**	
Insertion Loss	GSSG	-3dB@ 9.48GHz
Return Loss	GSSG	-3.71dB@ 9.48GHz
Near-End Crosstalk	GAAQQG	-23.21dB@ 9.48GHz
	GAAGQQG	-36.22dB@ 9.48GHz
	Xrow, GAAG to GQQG	-26.69dB@ 9.48GHz
Far-End Crosstalk	GAAQQG	-29.29dB@ 9.48GHz
	GAAGQQG	-26.39dB@ 9.48GHz
	Xrow, GAAG to GQQG	-23.06dB@ 9.48GHz

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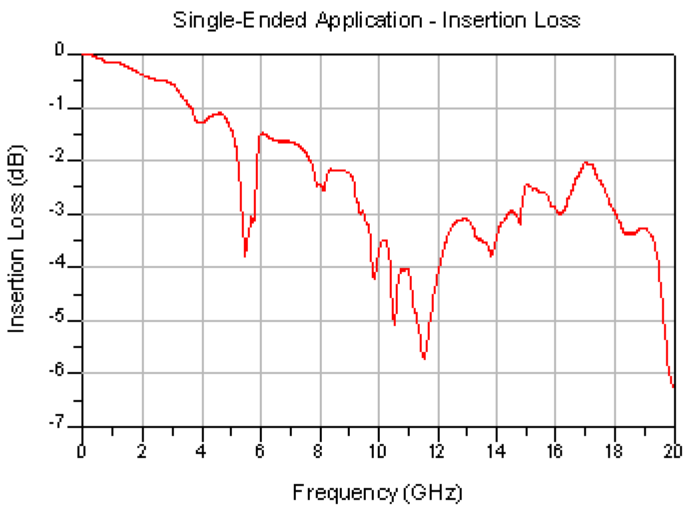
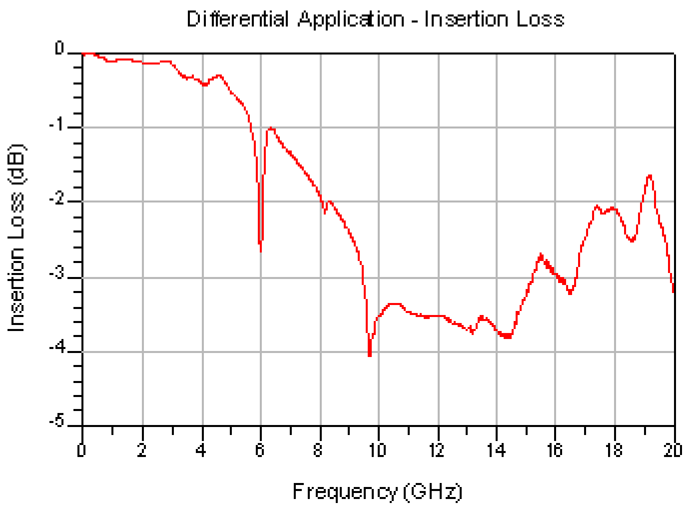
Bandwidth Chart – Single-Ended & Differential Insertion Loss

MW/CLM Connector Series





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Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω)

Signal Rise-time	30ps	50ps	100ps	250ps	500ps
Maximum Impedance	96.15	82.61	67.73	57.69	54.95
Minimum Impedance	47.52	49.03	49.44	49.83	49.88

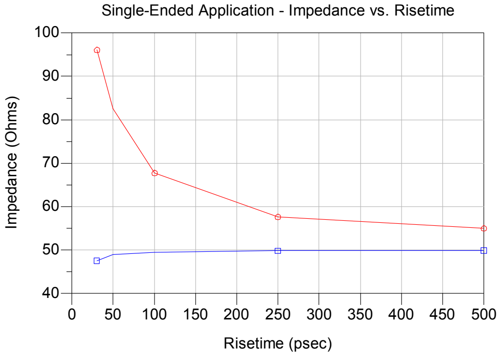

Table 4 - Differential Impedance (Ω)

Signal Rise-time	30ps	50ps	100ps	250ps	500ps
Maximum Impedance	147.77	128.62	109.22	104.05	102.91
Minimum Impedance	85.14	91.89	98.47	99.11	99.13

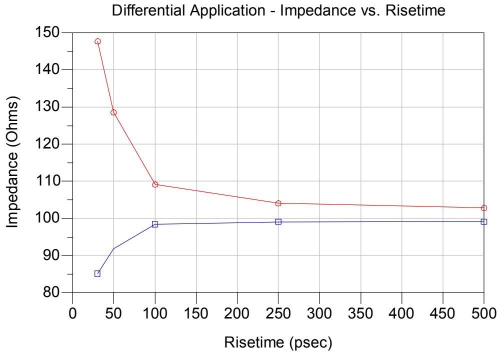

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Table 5 - Single-Ended Crosstalk (%)

Input(t_r)		30ps	50ps	100ps	250ps	500ps
NEXT	GAQG	17.49	16.40	13.95	8.35	4.66
	GAGQG	2.24	2.00	1.64	0.87	0.46
	Xrow	10.45	9.42	7.35	3.71	1.93
FEXT	GAQG	10.30	8.59	6.74	3.62	2.00
	GAGQG	3.28	2.19	1.31	0.64	0.34
	Xrow	6.11	5.27	3.57	1.73	0.98

Table 6 - Differential Crosstalk (%)

Input(t_r)		30ps	50ps	100ps	250ps	500ps
NEXT	GAAQQG	5.79	5.34	4.57	2.75	1.53
	GAAGQQG	0.45	0.35	0.26	0.13	<0.1
	Xrow	5.90	5.51	4.03	1.83	0.94
FEXT	GAAQQG	1.79	1.22	0.86	0.55	0.33
	GAAGQQG	0.54	0.35	0.18	<0.1	<0.1
	Xrow	2.23	1.94	1.17	0.47	0.24

Table 7 - Propagation Delay (Mated Connector)

Single-Ended	82ps
Differential	81ps

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Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector’s true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as “ground”. In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

For this connector, the following array configurations are evaluated:

Single-Ended Impedance**:**
- GSG (ground-signal-ground)

Single-Ended Crosstalk**:**
- Electrical “worst case”: GAQG (ground-active-quiet-ground)
- Electrical “best case”: GAGQG (ground-active-ground-quiet-ground)
- Across row: “xrow case”: GAG to GQG (from one row of terminals to the other row)

Differential Impedance**:**
- GSSG (Ground-positive signal-negative signal-ground)

Differential Crosstalk**:**
- Electrical “worst case”: GAAQQG (ground-active-active-quiet-quiet-ground)
- Electrical “best case”: GAAGQQG (ground-active-active-ground-quiet-quiet-ground)
- Across row: “xrow case”: GAAG to GQQG (from one row of terminals to the other row)

Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):

In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

For this report, measured rise times were at 10%-90% signal levels.

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Frequency Domain Data

Frequency Domain parameters are helpful in evaluating the connector system’s signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. The measured S-Parameters from the network analyzer are post-processed using Agilent Advanced Design System to obtain the time domain response. Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 51.5 mils of PCB trace on the MW connector side and 73 mils of trace on the CLM PCB. Delay is measured at 30 picoseconds signal rise-time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

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Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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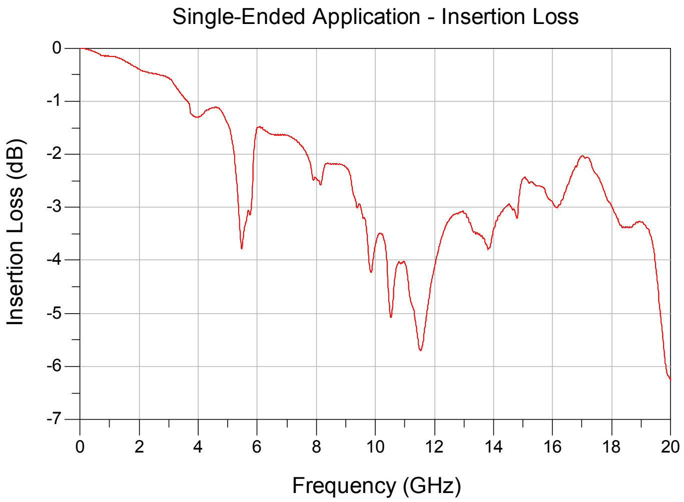
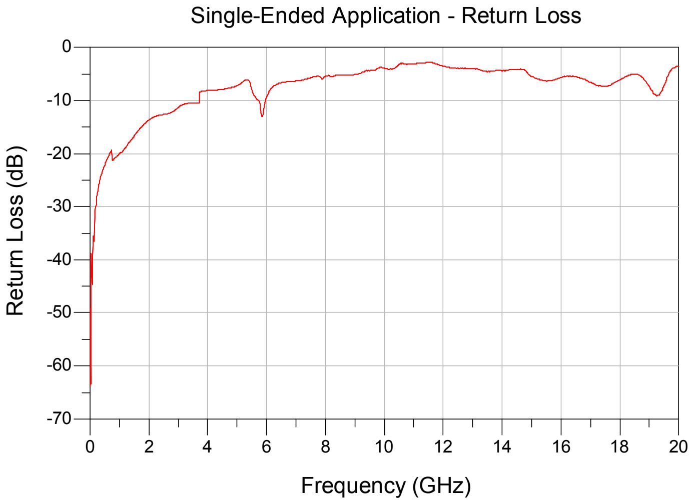
Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss

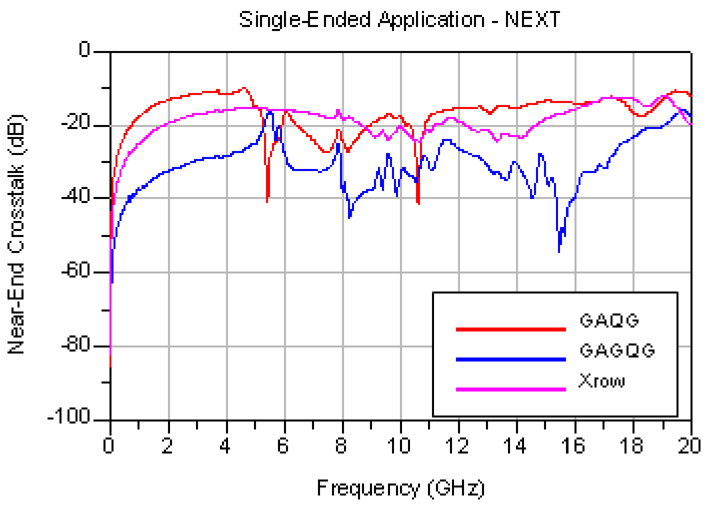


Single-Ended Application – Return Loss

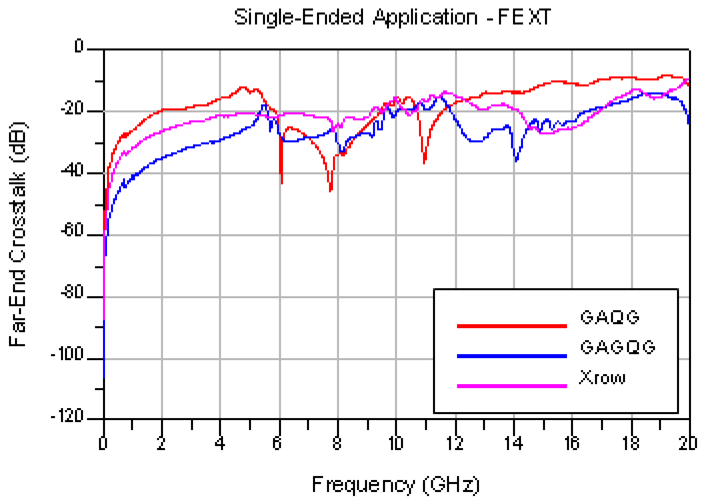


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334") stack height

Single-Ended Application – NEXT Configurations



Single-Ended Application – FEXT Configurations



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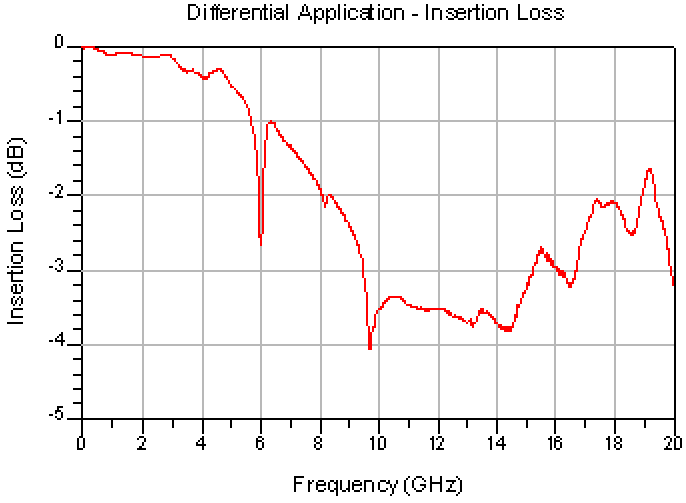
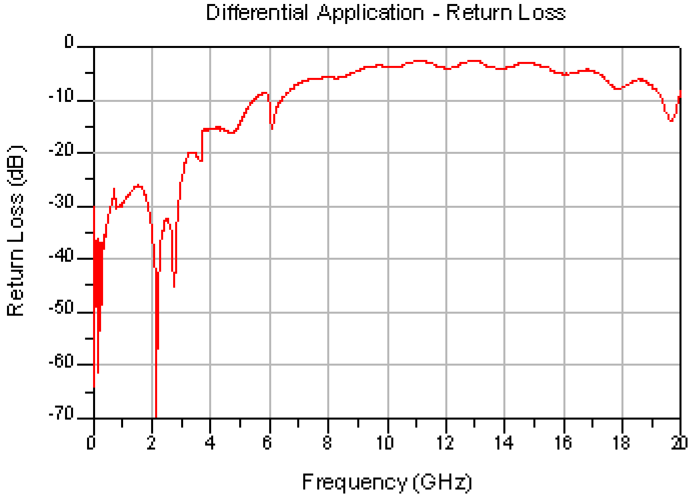
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

Differential Application – Insertion Loss

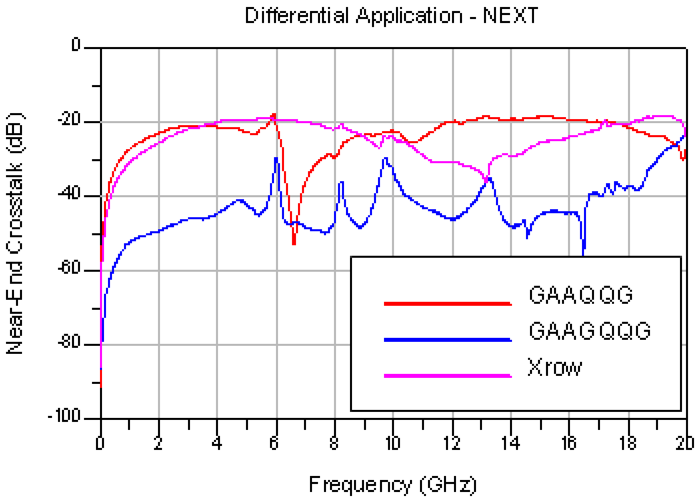


Differential Application – Return Loss

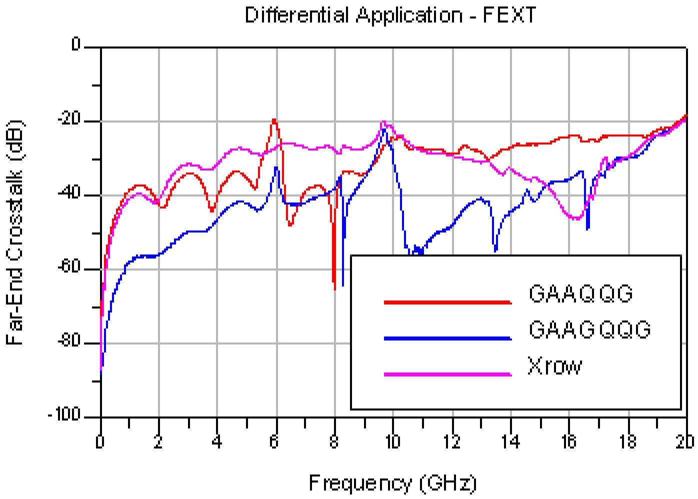


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

Differential Application – NEXT Configurations



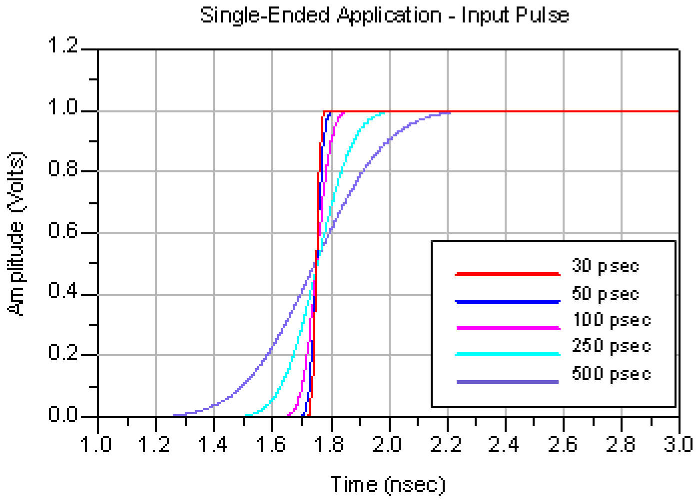
Differential Application – FEXT Configurations



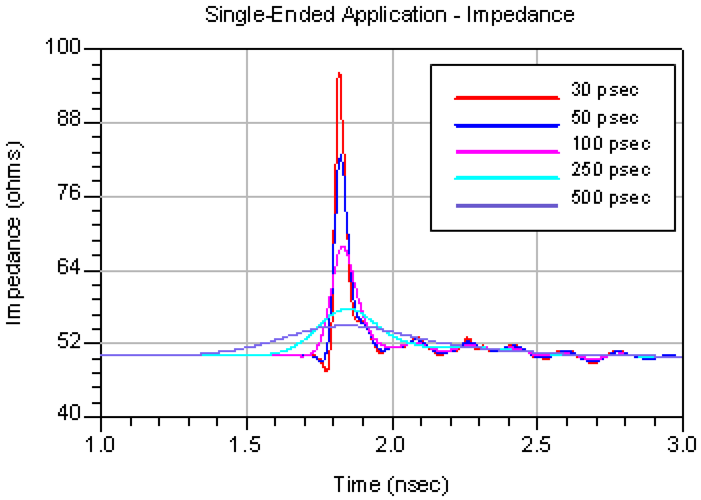
Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334") stack height

Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse



Single-Ended Application – Impedance



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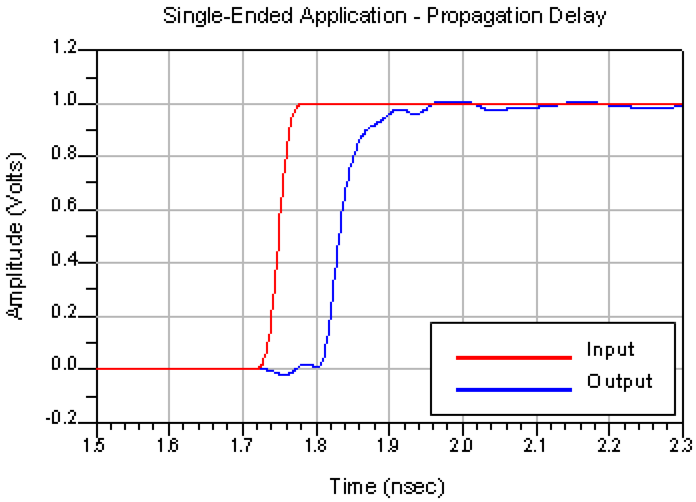
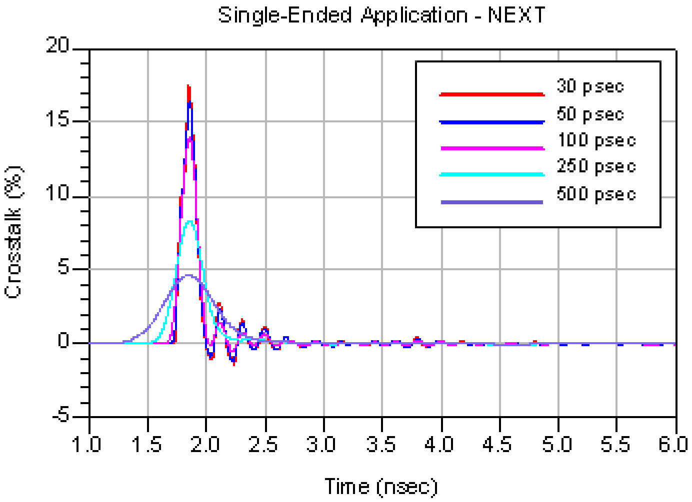
Single-Ended Application – Propagation Delay

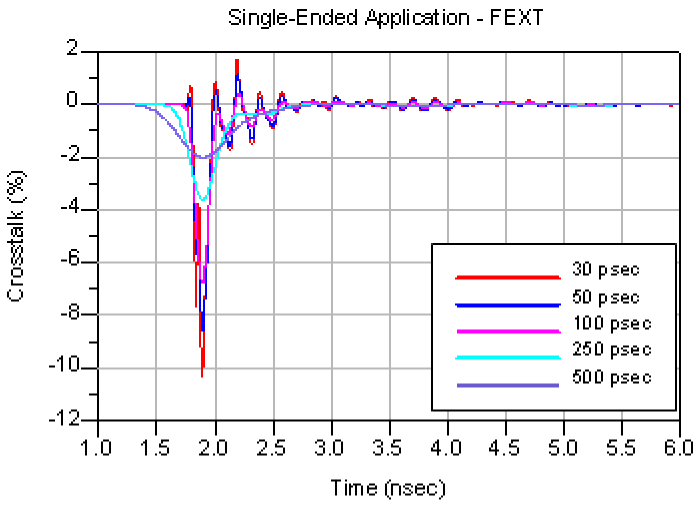


Single-Ended Application – NEXT, Worst Case Configuration

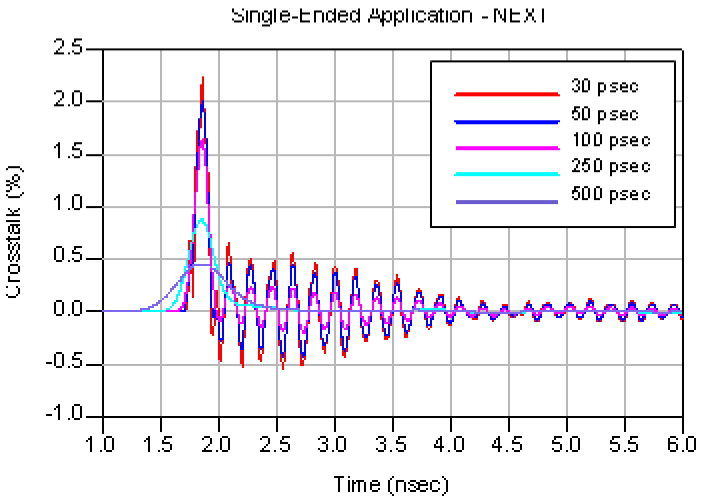


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

Single-Ended Application – FEXT, Worst Case Configuration

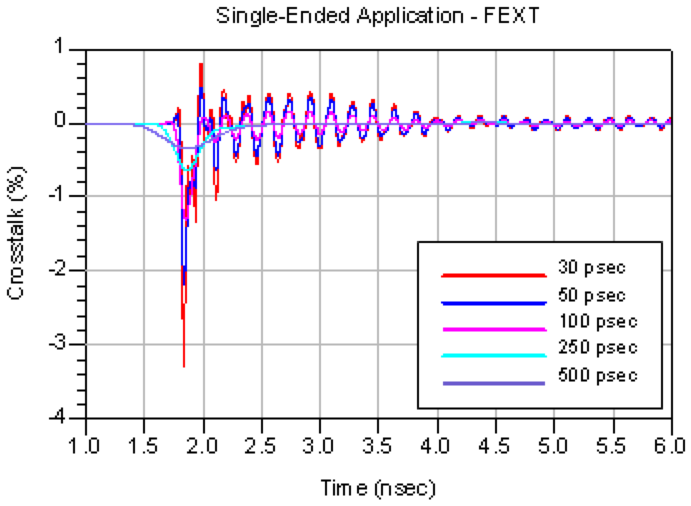


Single-Ended Application – NEXT, Best Case Configuration

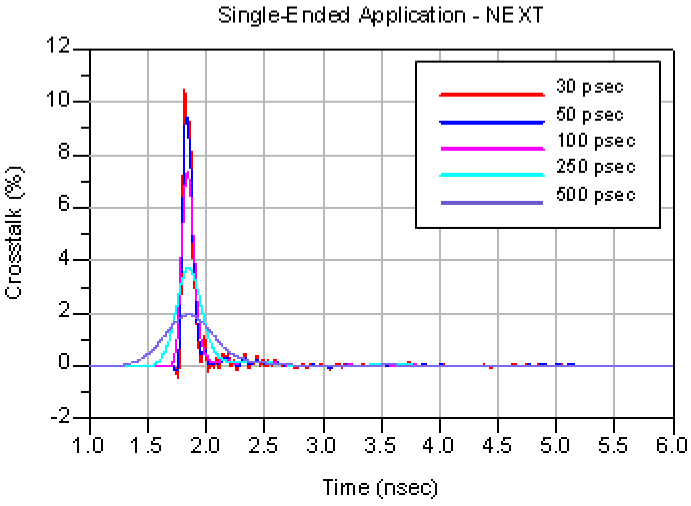


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

Single-Ended Application – FEXT, Best Case Configuration

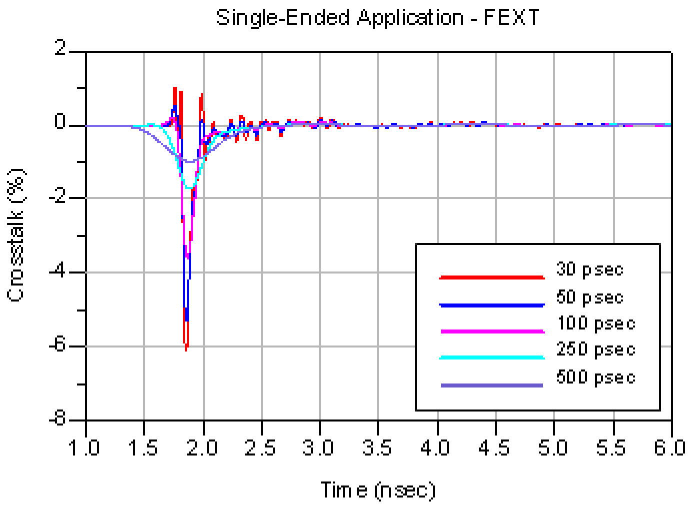


Single-Ended Application – NEXT, Across Row Configuration

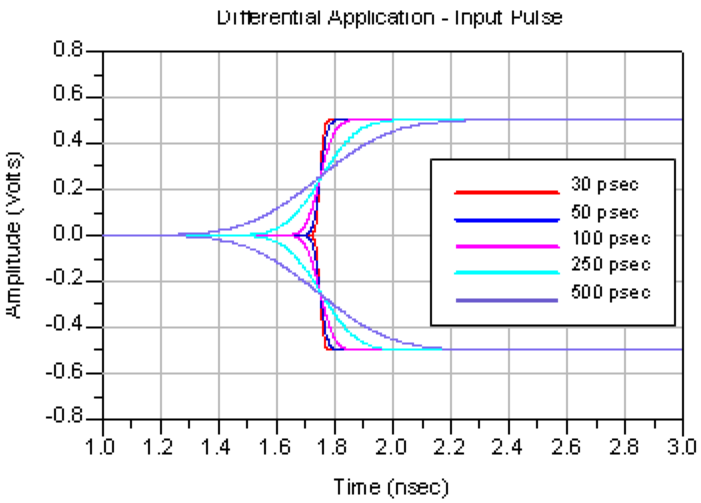


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

Single-Ended Application – FEXT, Across Row Configuration

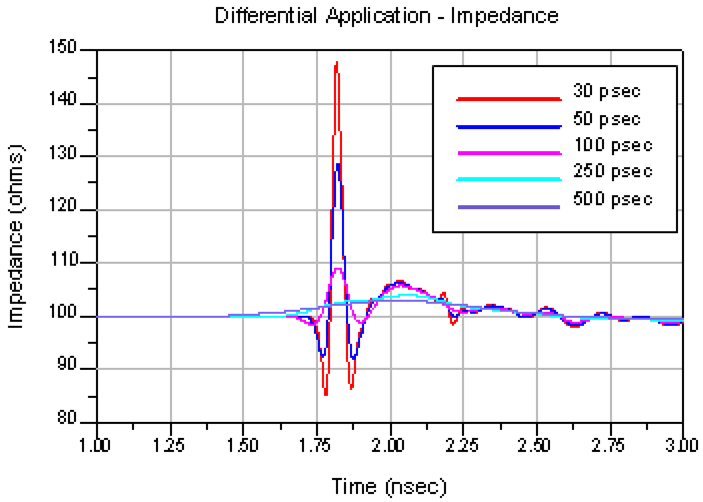


Differential Application – Input Pulse

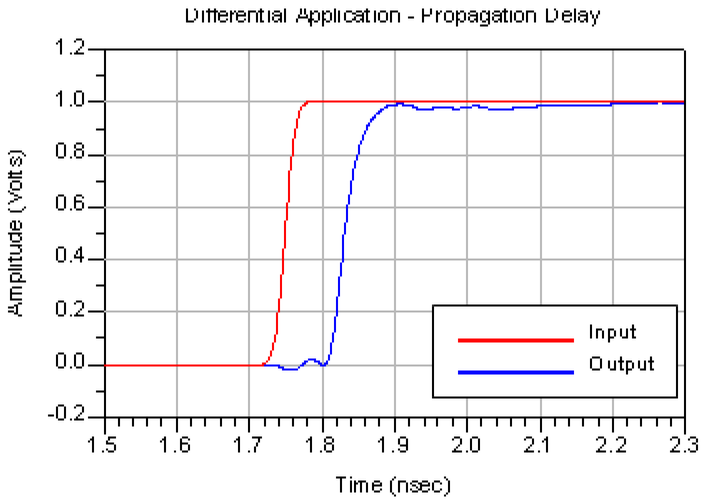


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

Differential Application – Impedance

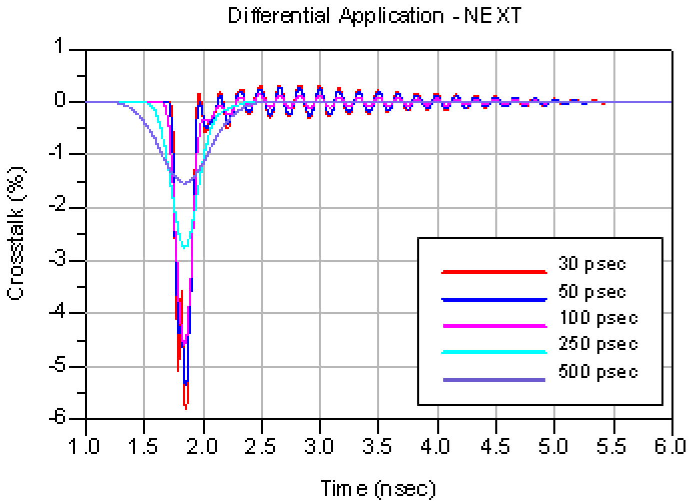


Differential Application – Propagation Delay

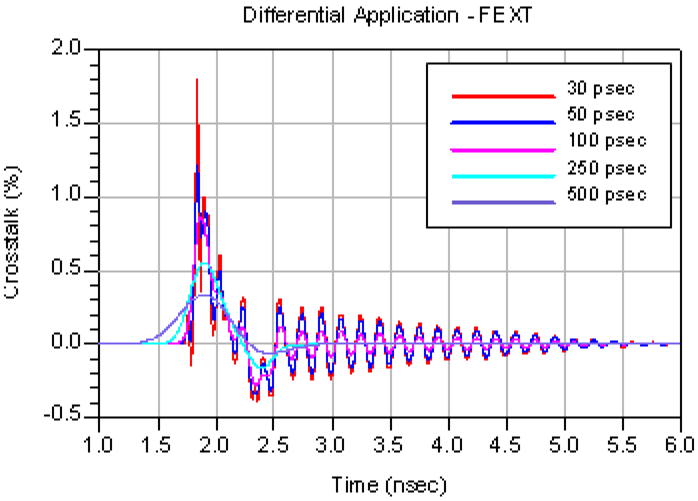


Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334”) stack height

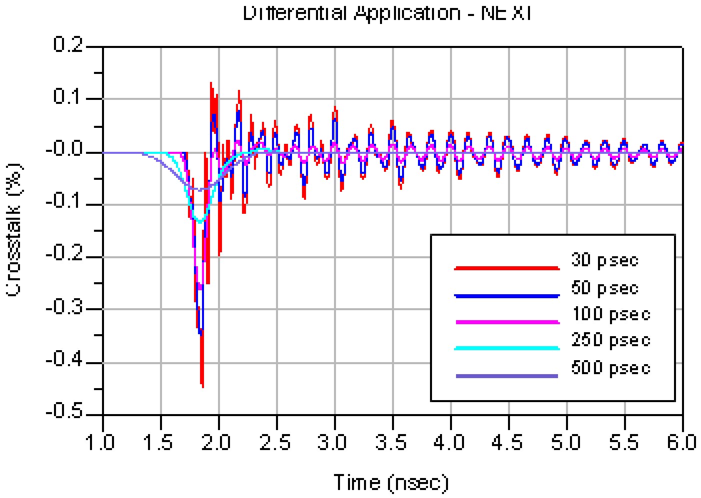
Differential Application – NEXT, Worst Case Configuration



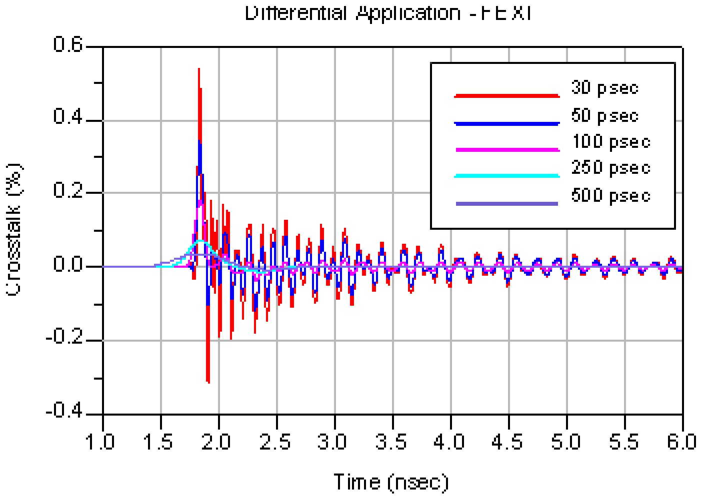
Differential Application – FEXT, Worst Case Configuration



Differential Application – NEXT, Best Case Configuration



Differential Application – FEXT, Best Case Configuration



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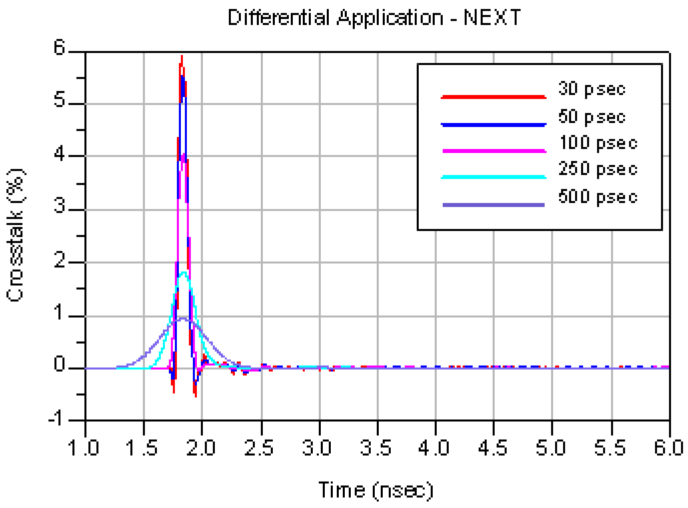
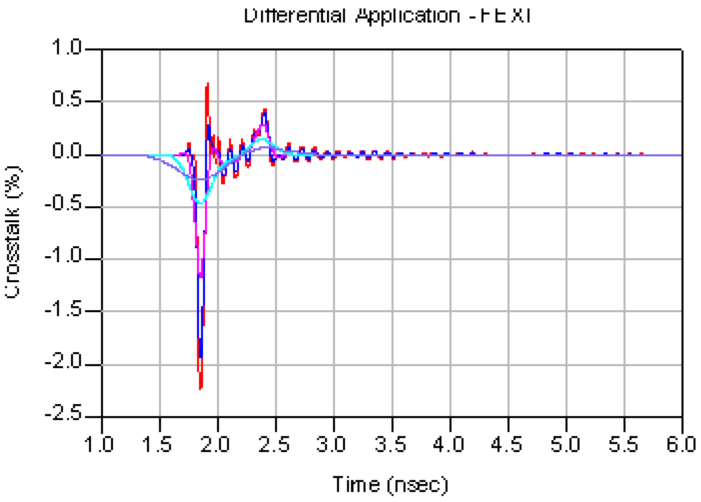
Differential Application – NEXT, Across Row Case Configuration



Differential Application – FEXT, Across Row Case Configuration



Appendix C – Product and Test System Descriptions

Product Description

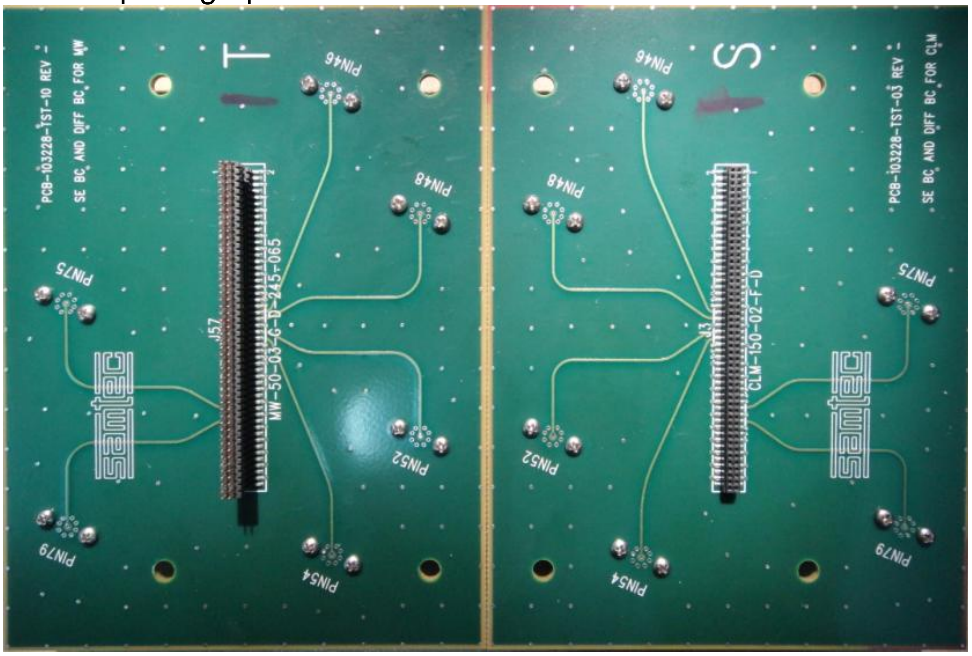
Product test samples are 8.48mm (0.334”) stack height MW/ CLM Series connectors. The part numbers are MW-50-03-G-D-245-065 and CLM-150-02-F-D. The MW/ CLM Series connectors are surface mount products. The MW/ CLM Series socket uses a strip contact system. Each connector has two rows of contacts evenly spaced on a 1.00 mm (0.0394”) pitch. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Six test fixtures are specific to the MW/CLM Series connector set and identified by part numbers PCB-103228-01, PCB-103228-03, PCB-103228-05 and PCB-103228-TST-09 to 11. Calibration standards specific to the MW/CLM Series are located on the calibration boards PCB-103228-TST-07 and PCB-103228-TST-08. To keep trace lengths short, three different test board sets were required to access the necessary signal pins.

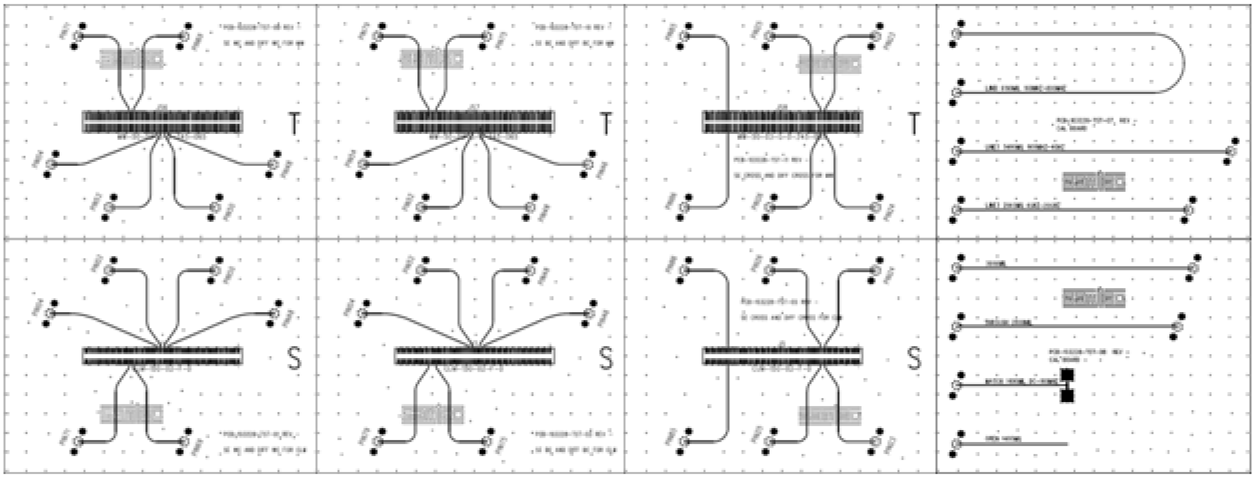
PCB-103228-TST-XX Test Fixtures

Shown below is a photograph of one of the three test board sets.



PCB-103228-TST-XX PCB Layout Panel

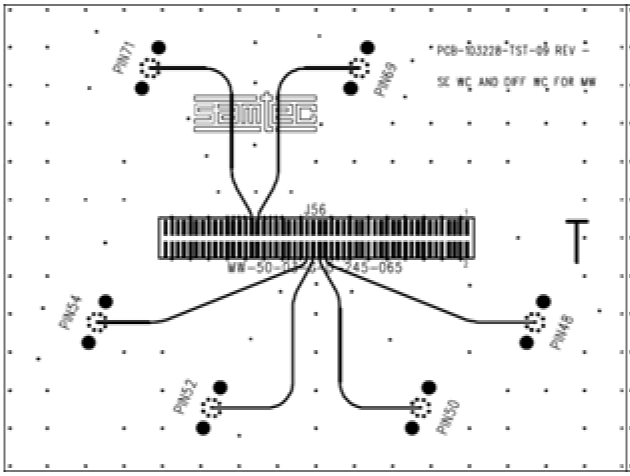
Artwork of the PCB design is shown below.



PCB Fixtures

The test fixtures used are as follows:

PCB-103228 -TST-01 Rev – CLM Series Test Board for worst-case crosstalk
PCB-103228 -TST-09 Rev – MW Series Test Board for worst-case crosstalk
PCB-103228 -TST-03 Rev – CLM Series Test Board for best-case crosstalk
PCB-103228 -TST-10 Rev – MW Series Test Board for best-case crosstalk
PCB-103228 -TST-05 Rev – CLM Series Test Board for cross row crosstalk
PCB-103228 -TST-11 Rev – MW Series Test Board for cross row crosstalk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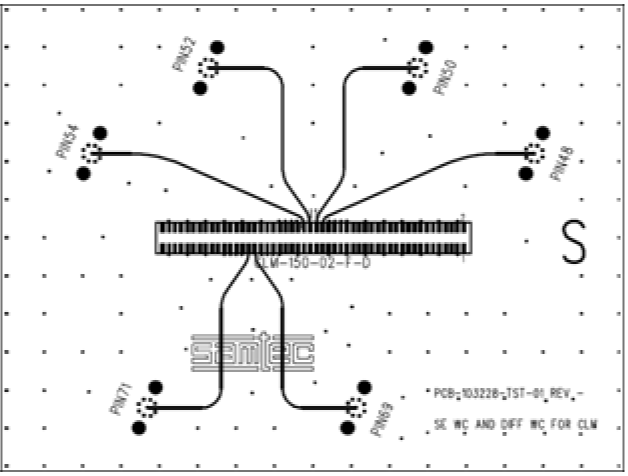
PIN69
PCB-103228-TST-09 REV –
SE WC AND DIFF WC FOR MW
J56
MW-50-03-G-D-245-065
T
PIN54
PIN48
PIN52
PIN50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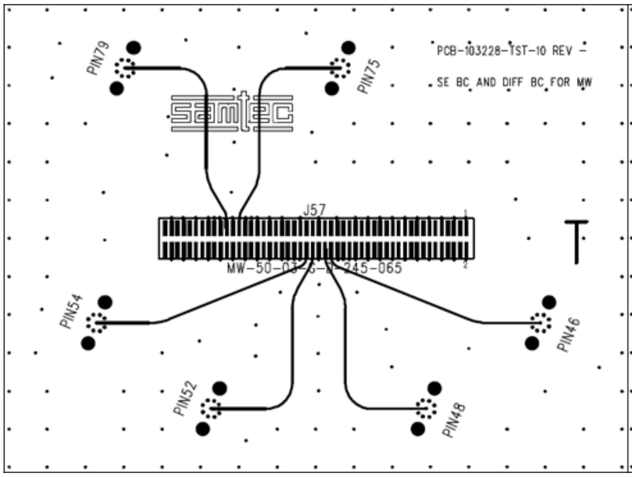
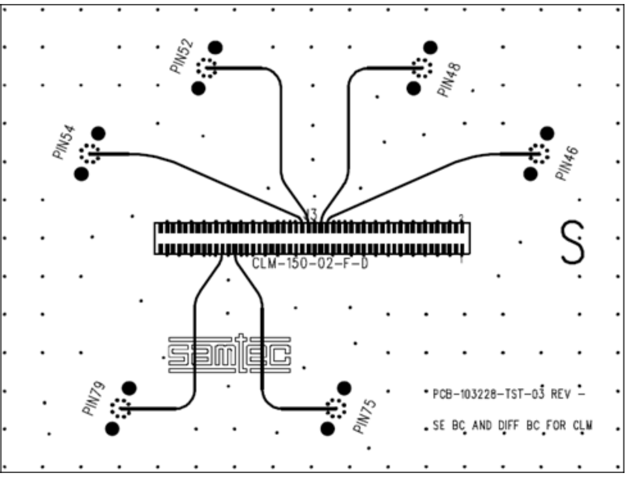
PCB-103228-TST-01 REV –
SE WC AND DIFF WC FOR CLM


PIN79
PIN75
PCB-103228-TST-10 REV –
SE BC AND DIFF BC FOR MW
J57
MW-50-03-G-D-245-065
T
PIN54
PIN46
PIN52
PIN48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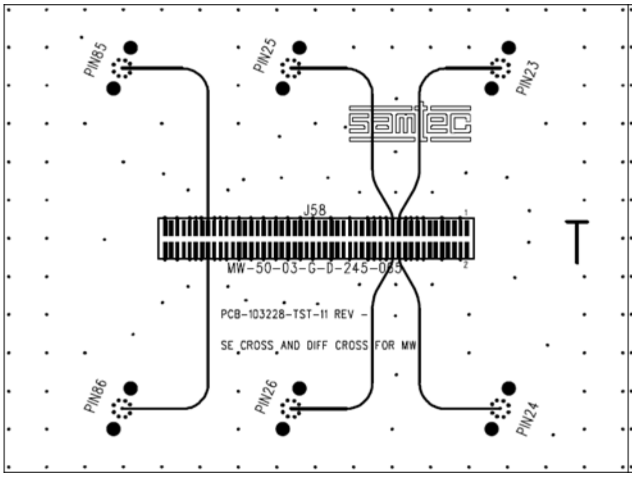
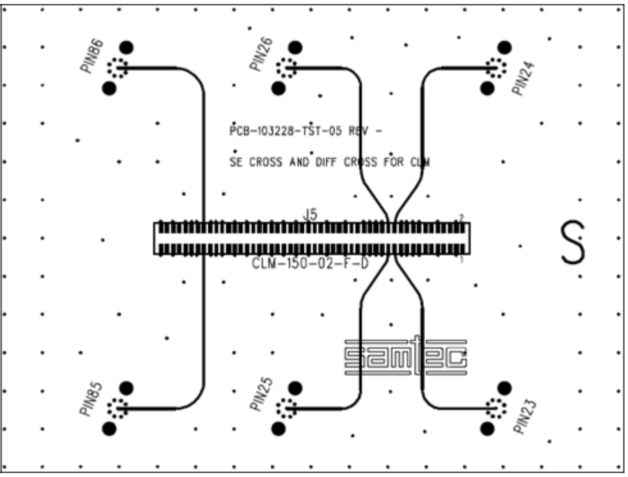
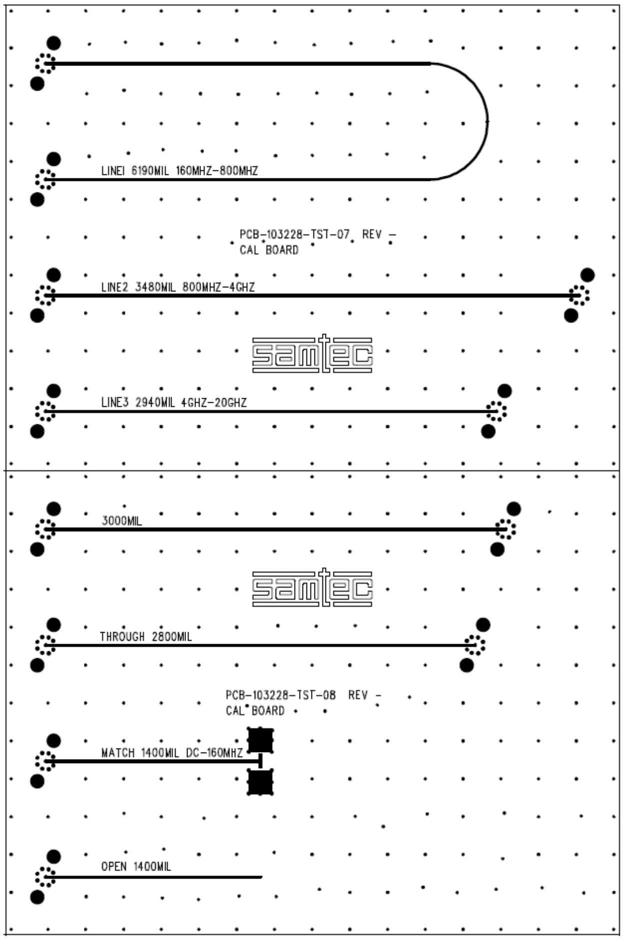
PIN48
PIN54
PIN46
J3
CLM-150-02-F-D
S
PIN79
PIN75
PCB-103228-TST-03 REV –
SE BC AND DIFF BC FOR CLM


PIN85
PIN25
PIN23
J58
MW-50-03-G-D-245-065
T
PCB-103228-TST-11 REV –
SE CROSS AND DIFF CROSS FOR MW
PIN86
PIN26
PIN24


PIN86
PIN26
PIN24
PCB-103228-TST-05 REV –
SE CROSS AND DIFF CROSS FOR CLM
J5
CLM-150-02-F-D
S
PIN85
PIN25
PIN23

Calibration Board

Test fixture losses and test point reflections were removed from the data by use of TRL calibration. The calibration board is shown below. Prior to making any measurements, the calibration board is characterized to obtain parameters required to define the calibration kit. Once a cal kit is defined, calibration using the standards on the calibration board can be performed. Finally, the device can be measured and the test board effects are automatically removed.



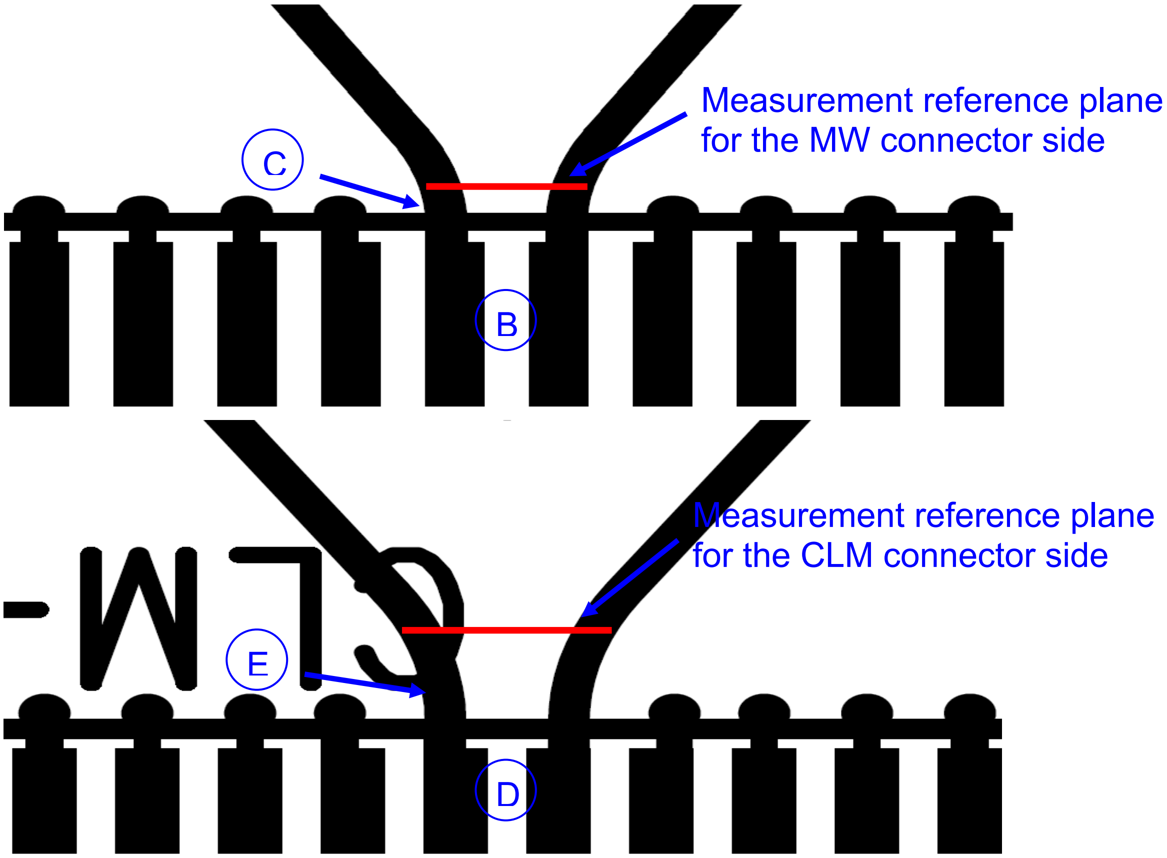
Thru line – 2800 mils
Open Reflect – 1400 mils
Line 1 – 6190 mils
Line 2 – 3480 mils
Line 3 – 2940 mils
Match – 1400 mils

Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334") stack height

All traces on the test boards are length matched to 1.5" measured from the center of the pad to the SMA. The TRL calibration effectively removes 1.4" of test board trace effects. Since the pad sizes for the MW and CLM connectors are different sizes, the reference plane location is slightly different on each test board. This means that 51.5 mils of test board trace length effects for the MW connector side and 73 mils for the CLM connector side are included in the measurement. The S-Parameter measurement includes:

A- The MW Series connector set
B- Test board vias, pads (footprint effects) for the MW connector side.
C- 51.5 mils of 16 mil wide microstrip trace.
D- Test board vias, pads (footprint effects) for the CLM connector side.
E- 73 mils of 16 mil wide microstrip trace.

The figure below shows the location of the measurement reference plane.



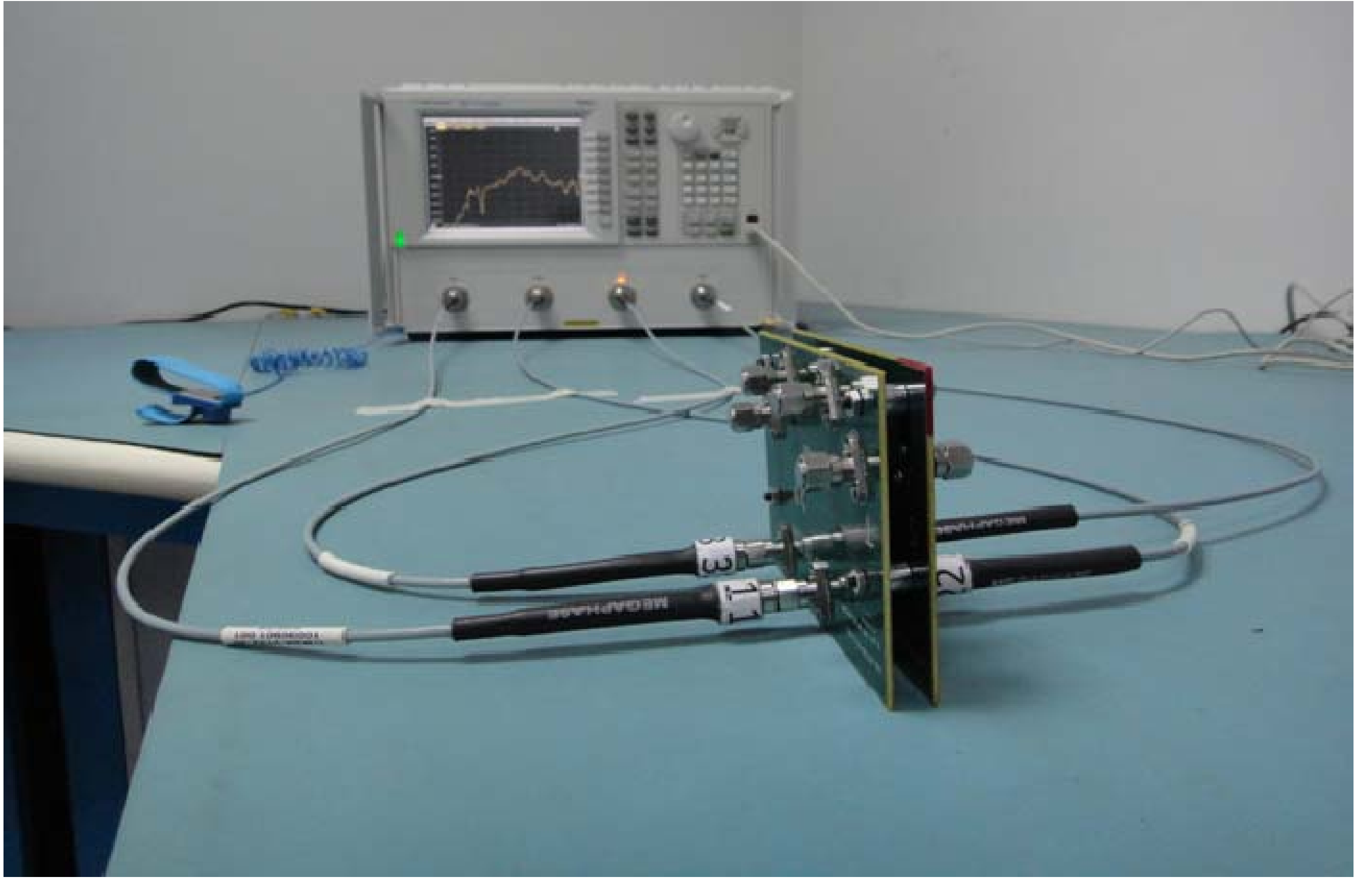
Appendix D – Test and Measurement Setup

The test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz
Stop Frequency – 20 GHz
Number of points -1601
IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Series: MW/CLM
Description: Surface Mount Board, 1.00mm Pitch, 8.48mm (0.334") stack height

Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Megaphase CM26 (DC-26 GHz)

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the LRM calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the LRM calibration standards. A coaxial SOLT calibration is performed using an N4433A ecal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the reflect and 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the MW/ CLM Series test boards, this is greater than 20 GHz.

From the LRM calibration standard measurements, a user defined calibration kit is developed and stored in the network analyzer. Calibration is then performed on all 4 ports following the calibration wizard within the Agilent N5230C. This calibration is saved and can be recalled at any time. Calibration takes roughly 30 minutes to perform.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2009 update 1. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)
A step pulse is applied to the touchstone model of the connector and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Near-End Crosstalk (TDT) & Far End Crosstalk (TDT)

A step pulse is applied to the touchstone model of the connector and the coupled voltage is monitored. The amplitude of the peak-coupled voltage is recorded and reported as a percentage of the input pulse.

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
BC – Best Case crosstalk configuration
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
Z – Impedance (expressed in ohms)