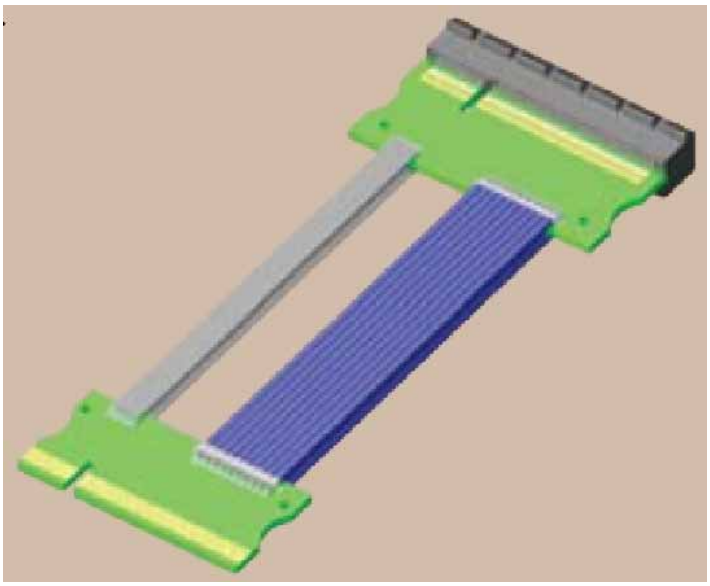
High Speed Characterization Report

PCIEC-064-1000-EC-EM-P-85



Mated with:
PCIEC-064-02-F-D-TH

Description:
PCI Express Data Rate Cable Jumper,
85 Ohm Twinax Cable

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Series: PCIEC-85
Description: PCI Express Data Rate Cable Jumper, 85 Ohm Twinax Cable

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Introduction

This testing was performed to evaluate the high speed electrical performance of Samtec's 85 Ω PCI Express® Jumper cable.

The 85 Ω PCI Express® Jumper cable is capable of supporting one, four, eight and sixteen PCI Express links. It can be used as:

- a loop back extender from one PCIE slot to another PCIE slot,
- a Ser-Des physical extender from one PCIE slot to another PCIE Ser-DES or,
- as a physical extender for easy troubleshooting of PCIE card debug and analysis for one PCIE slot to Emulator or Analyzer.

All PCIE 85 Ω cable assembly test data presented in this report was acquired in the frequency domain using an Agilent Technologies N5230C PNA-L Network Analyzer. The ports' reference impedances for all test data was transformed from 50 Ω to 42.5 Ω using Agilent Physical Layer Test System (PLTS) 2012.1 software, and then exported in s4p format for post processing in Agilent Advanced Design System (ADS) 2011.1 software.

Product Description

The 85 Ω PCI Express® Jumper cable is constructed using 32 AWG 85 ohm shielded twinax cable for PCIe Gen 3 data transfer and using 30 AWG discrete ribbon cable for power, clock and JTAG operations. The cable is terminated at the first end with an 85 Ω edge card and terminated at the second end with an edge mount connector on an 85 Ω printed circuit board; see Figure 1 for a picture of the PCIE cable assembly and the relative pin mapping.

The part number of the sample tested is: PCIEC-064-1000-EC-EM-85. All test data presented in this report was taken with the sample mated to a PCIE-064-02-X-D-TH Express Card Socket at the first end and edge card test boards at the second end.

Two signal positions on the cable assembly were tested; the shortest physical path and the longest physical path. Testing these two positions allows for capturing the best case performance and worse case performance and the maximum skew of the sample.

Series: PCIEC-85
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The test positions, the crosstalk aggressors, and the victim positions are shown below in Table I:

Table I: Test Positions

Path	Position	Crosstalk Aggressor	Crosstalk Victim
Long path	A29 & A30	A29 & A30	A25 & A26
Short Path	B23 & B24	B19 & B20	B19 & B20

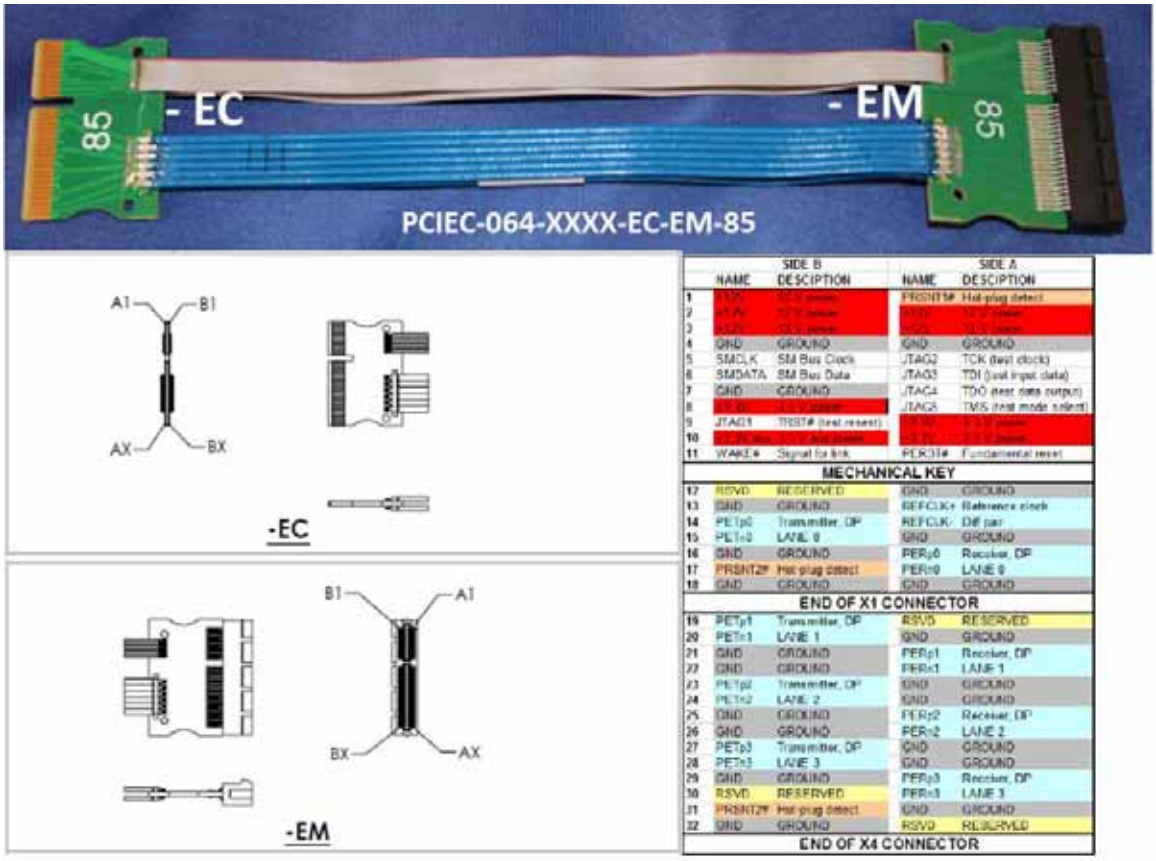

Figure 1: PCIEC-064-XXXX-EC-EM-85 Sample

(P/N:) PCIEC-064-0152-EC-EM-85

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Cable Assembly Speed Rating

The cable assembly Speed Rating is based on the -7 dB insertion loss point of the mated cable assembly. The -7 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -7 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for any loss from the test board's traces. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

The PCIE 85 Ω cable assembly has a -7 dB point of 4.23 GHz; therefore, the PCIE 85 Ω cable assembly has a Speed Rating of 4.5GHz/9.0 Gbps.

The Samtec Speed Rating is best considered as a figure of merit for comparing relative performance between cable assemblies. The Speed Rating becomes less meaningful in systems using multi-level signaling or where crosstalk or impedance mismatch are more critical parameters.

Modern high speed digital transceivers can accommodate roughly 9 dB of loss and still operate reliably. The -7dB rating is a conservative number that allocates 2 dB of system budget for other channel components such as short PCB traces and IC packaging effects.

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Results Summary

Note that all measurements were performed with the PCIEC cable assembly mated to the respective connector/test board.

Time Domain Data

Impedance

The impedance profile was positioned such that the mated connector and the cable impedance can be seen. The rise time is 100ps.

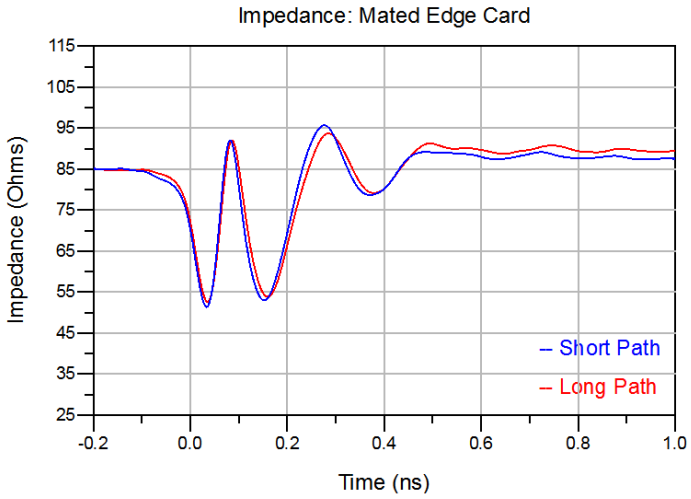

Figure 2: Impedance: Edge Card End

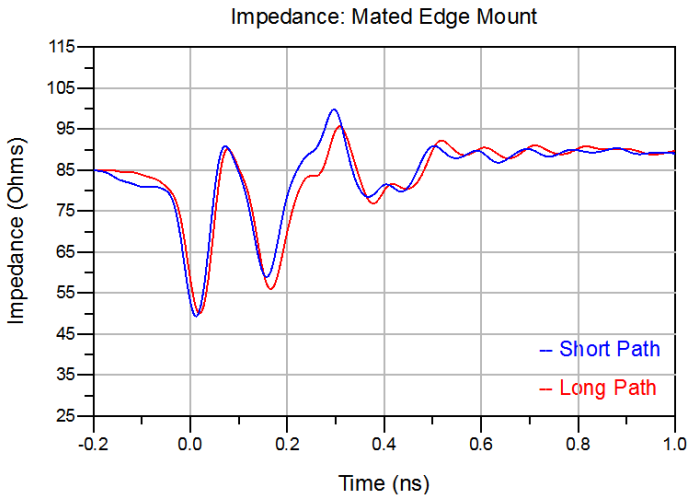

Figure 3: Impedance: Edge Mount End

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Timing Measurements

The cable assembly skew was calculated as the difference between the maximum (the longest physical path) and minimum (the shortest physical) propagation delays of the test sample.

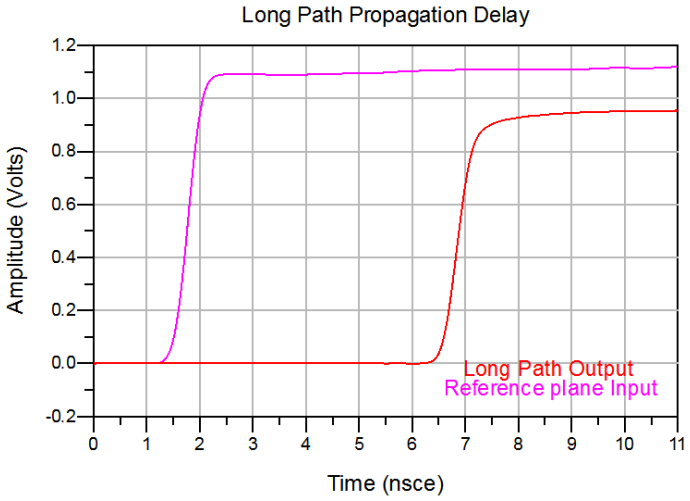

Figure 4: Propagation Delay; Long Path

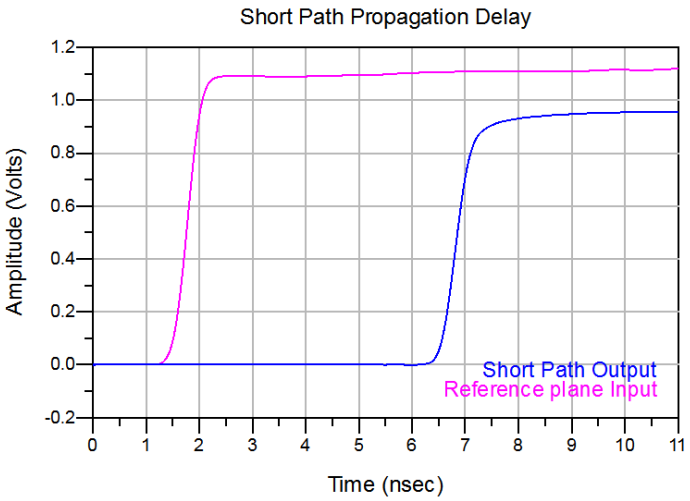

Figure 5: Propagation Delay; Short Path

Table II: Delay Measurements and Skew (nsec)

Propdelay_LongPath	Propdelay_ShortPath	Skew
5.08	5.05	0.025

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Near End Crosstalk

The termination designation is the source end of the assembly. The rise time is 100ps.

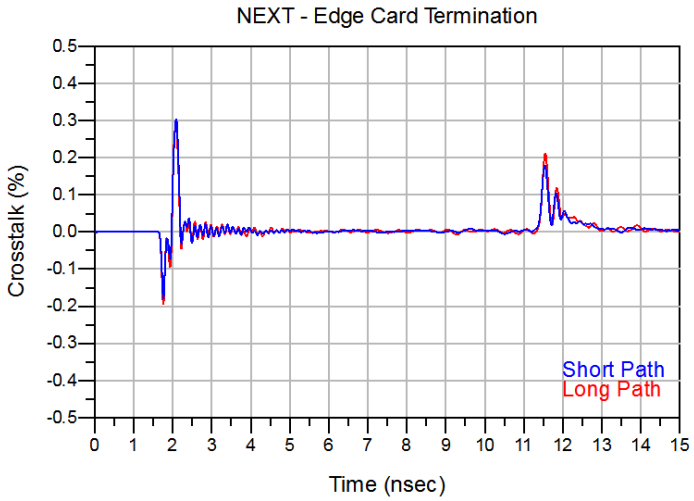

Figure 6: Percent Crosstalk: Edge Card Termination

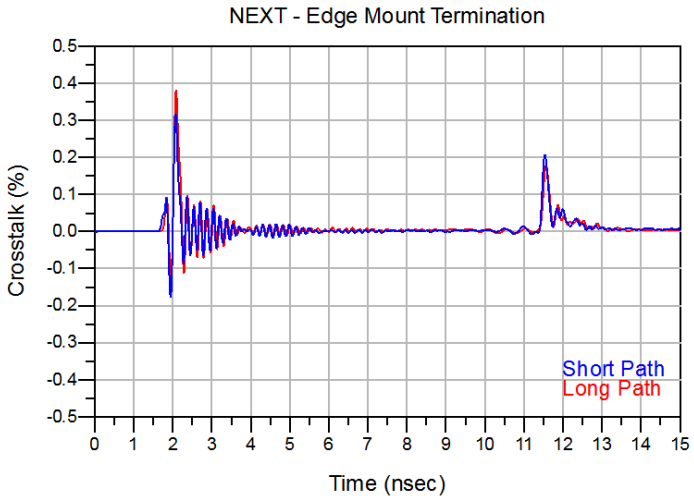

Figure 7: Percent NEXT: Edge Mount Termination

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Far End Crosstalk

The termination designation is the source end of the assembly. The rise time is 100ps.

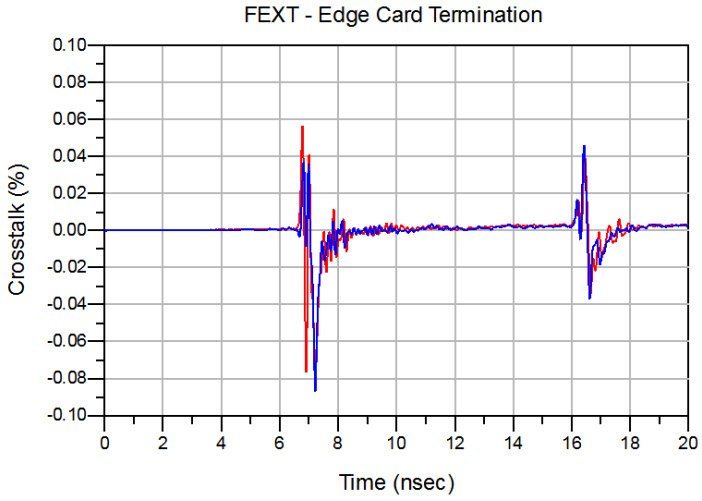

Figure 8: Percent FEXT: Edge Card Termination

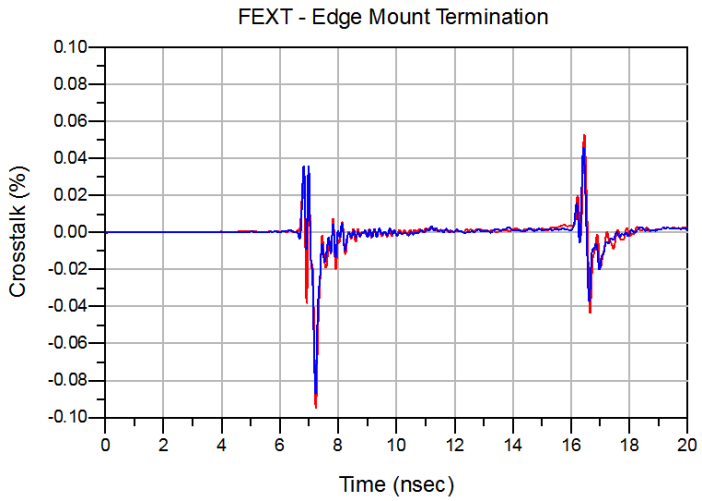

Figure 9: Percent FEXT; Edge Mount Termination

Series: PCIEC-85
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Frequency Domain Data

Insertion Loss

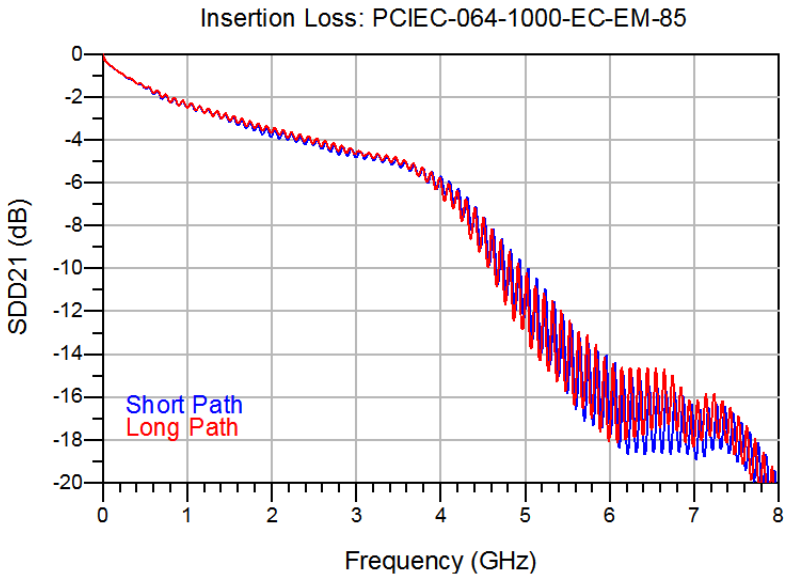

Figure 10: Differential Insertion Loss, SDD21

Return Loss

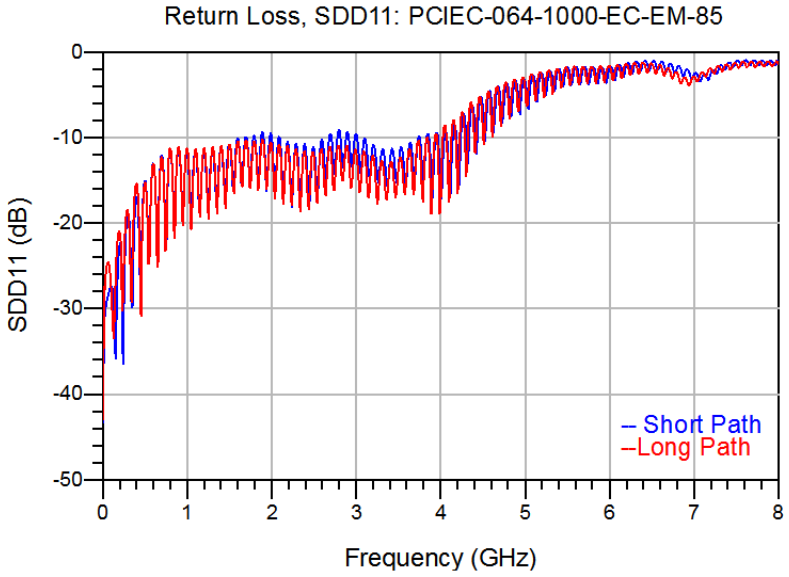

Figure 11: Differential Return Loss, SDD11

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Near End Crosstalk

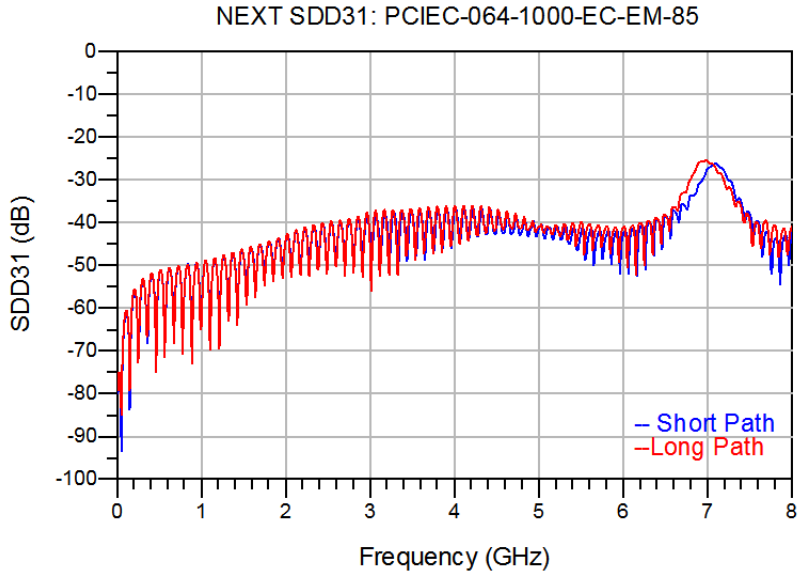

Figure 12: Differential NEXT SDD31

Far End Crosstalk

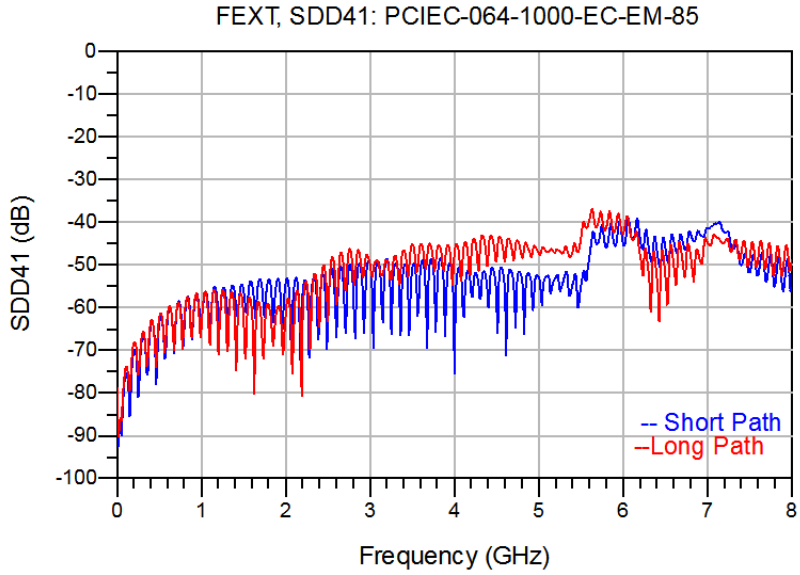

Figure 13: Differential FEXT SDD41

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PCB-103857-TST Test Fixtures

The test fixtures are composed of four-layer FR-406 material with 50Ω signal traces and pad configurations designed for the electrical characterization of Samtec high speed cable assemblies. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Three test fixtures are specific to the PCIEC-85 cable assembly and are identified by the part numbers: PCB-103857-TST-03 (PCIE Connector Card), PCB-103857-TST-01 (Edge Card Side "B") and PCB-103857-TST-02 (Edge Card Side "A"). Calibration standards specific to the PCIEC-85 cable assembly located on the calibration boards PCB-103314-TST-99 (Calibration Card).

Shown below in Figure 14 is a photograph the test boards used for testing the PCIEC-85 cable assembly.

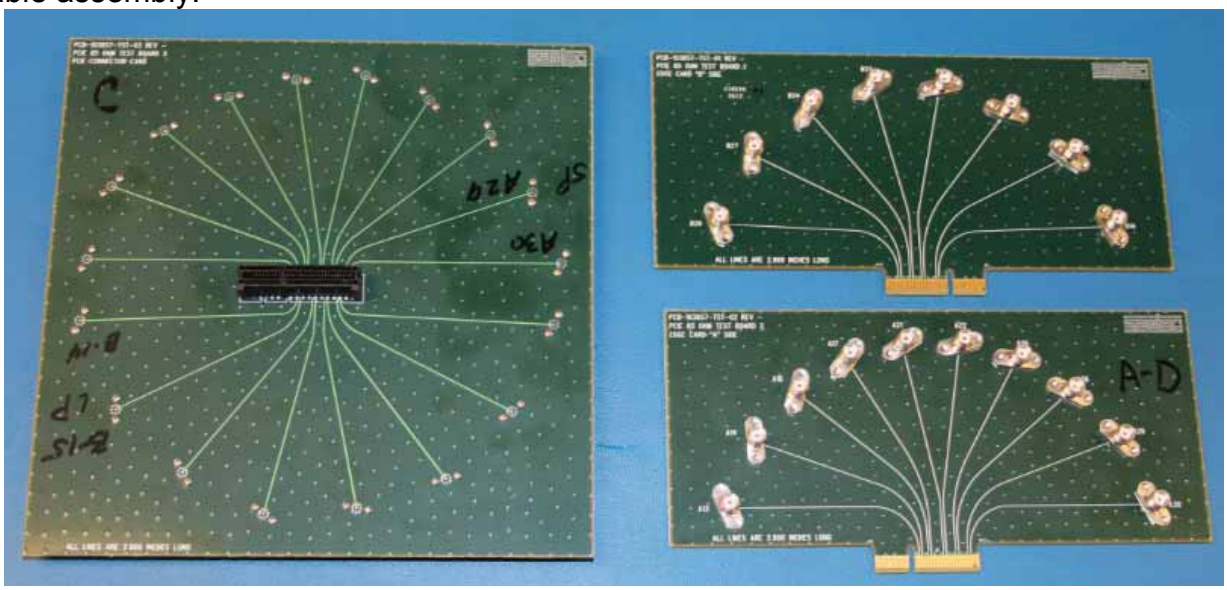

Figure 14: PCIE Test Boards

The test fixtures were mated to the cable assembly as follows:

- PCB-103857 -TST-03-B Rev, the PCIE Connector Card was mated to the edge card end of the cable assembly and was used to interface with both the "A" and "B" side of the cable assembly,
- PCB-103857 -TST-01-B Rev, the Edge Card "B" Side, mated to the edge mount connector and was used to interface with the "B" side positions,
- PCB-103857 -TST-02-B Rev, Edge Card "A" Side mated to the edge mount connector and was used to interface with the "A" side positions.

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Calibration Board

Test fixture losses and test point reflections were removed from the data by use of TRL calibration. The calibration board is shown below in Figure 15. Prior to making any measurements, the calibration board is characterized to obtain parameters required to define the calibration kit. Once a cal kit is defined, calibration using the standards on the calibration board can be performed. Finally, the device can be measured and the test board effects are automatically removed.

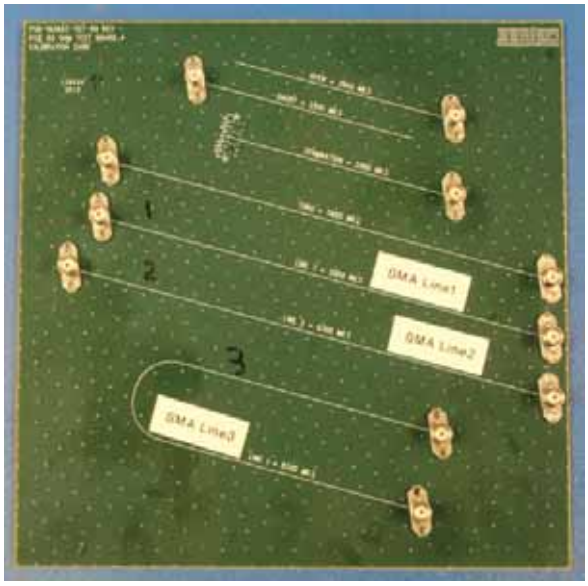

Figure 15: Calibration Board

The lengths of the calibration structures are:

- Thru line – 5800 mils
- Open Reflect – 2900 mils
- Load 2900 mils
- Line 1 – 8300 mils
- Line 2 – 6300 mils
- Line 3 – 5900 mils

All traces on the test boards are length matched to 5.8” measured from the edge of the pad to the SMA. The TRL calibration effectively removes all of test board trace effects. This means that 0 mils of test board trace length effects are included in the measurement. The S-Parameter measurements include the PCIE connector’s through-hole footprint.

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Figure 16 below shows the location of the measurement reference plane once the TRL calibration is implemented.

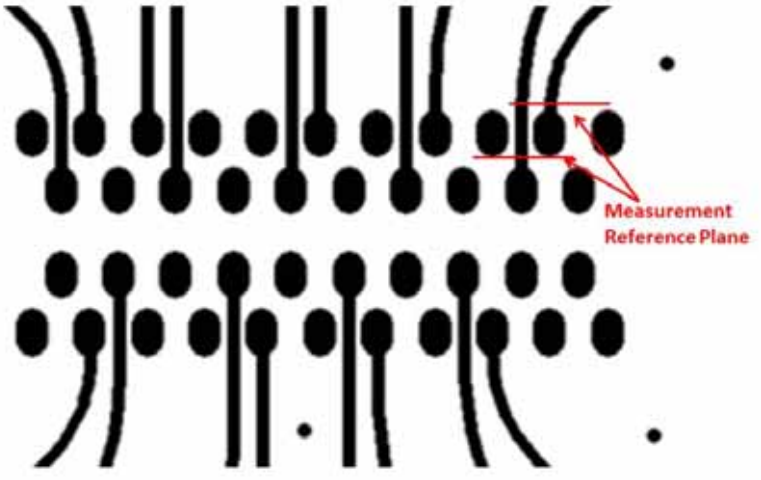

Figure 16: Measurement Reference Plane

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Test Procedures

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the LRM calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the LRM calibration standards. A coaxial SOLT calibration is performed using an N4433A Ecal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the reflect standard and the 2x thru line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the PCIEC 85 ohm test boards, this is greater than 20 GHz.

From the LRM calibration standard measurements, a user defined calibration kit is developed and stored in the network analyzer. Calibration is then performed on all 4 ports following the calibration wizard within the Agilent N5230C. This calibration is saved and can be recalled at any time.

Measurement Setup

Measurements were then performed using the test boards as shown below in Figure 17.

Figure 17: PCIE 85 Ohm Cable Assembly Test Setup

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Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A Ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Gore OWD01D02039-4 (DC-50 GHz)

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. However, a very accurate Time Domain response can be obtained with band-width limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2011 update 1. This tool has a transient convolution simulator which can generate a Time Domain response directly from measured S-Parameters.

Impedance (TDR)

The impedance was mathematically derived from the SDD11 and SDD22 S-parameter data using the tdr_sp_imped() measurement function within ADS.

Propagation Delay (TDT)

The Propagation Delay is a measure of the Time Domain delay through the fully mated cable assembly and connector footprint. A step pulse is applied to the Touchstone model of the mated cable assembly and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Near-End Crosstalk (TDT) & Far End Crosstalk (TDT)

A step pulse is applied to the Touchstone model of the mated cable assembly and the coupled voltage is monitored. The amplitude of the peak-coupled voltage is recorded and reported as a percentage of the input pulse.