High Speed Characterization Report

QFSS-052-01-L-D-A

Mated with

QMSS-052-11-L-D-A

Description:

Shielded High Speed Socket & Terminal Strip
0.635mm Centerline, Standard Configuration,
Vertical Board-to-Board
11mm Stack Height

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Report Revision: 9/27/2010

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

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Connector Overview

The 0.635mm (.025") centerline socket (QFSS) and terminal (QMSS) strip series is available with 52, 104, 156, and 208 total pins per connector set. It is hot pluggable with the shields and ground planes mating first followed by the signal pins. Standard shield grounding is GSSSSG. Q2 is surface mount, double row connector that when mated, equals an 11mm (.433") board-to-board stack height. The data presented in this report is applicable only to the QFSS /QMSS 0.635mm centerline; 11mm stack height Q2 series.

Connector System Speed Rating

Q2 Series, 0.635mm (.025") Centerline, Surface Mount, Double Row Vertical, Gold Plating, GSSSSG shield configuration

Signaling	Speed Rating
Single-Ended:	**6.0 GHz / 12Gbps**
Differential:	**7.0 GHz / 14Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded-up to the nearest half-GHz level. The up rounding corrects for a portion of the test board's trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

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Frequency Domain Data Summary

Table 1 – Single-Ended Signaling- Case I - System Performance				
Test Parameter	**File**	**Source**	**Victim**	
Insertion Loss	RLIL_P1_3_P2_3	port 1=QFSS_3, port 3=QMSS_3		-3dB @ 6.0 GHz
Return Loss	RLIL_P1_3_P2_3	port 1=QFSS_3, port 3=QMSS_3		≤ -5dB to 6.0 GHz
Near-End Crosstalk	NV1_P1_59_P2_61	QFSS_59	QFSS_61	≤ -7dB to 6.0 GHz
	NV2_P1_91_P2_95	QFSS_91	QFSS_95	≤ -14dB to 6.0 GHz
	NV3_P1_91_P2_92	QFSS_91	QFSS_92	≤ -22dB to 6.0 GHz
Far-End Crosstalk	FV1_P1_59_P2_61	QFSS_59	QMSS_61	≤ -18dB to 6.0 GHz
	FV2_P1_91_P2_95	QFSS_91	QMSS_95	≤ -43dB to 6.0 GHz
	FV3-P1_91_P2_92	QFSS_91	QMSS_92	≤ -42dB to 6.0 GHz

Table 2 – Single-Ended Signaling- Case II - System Performance				
Test Parameter	**File**	**Source**	**Victim**	
Insertion Loss	RLIL_P1_15_P2_15	port 1=QFSS_15, port 3=QMSS_15		-3dB @ 5.6 GHz
Return Loss	RLIL_P1_15_P2_15	port 1=QFSS_15, port 3=QMSS_15		≤ -7dB to 5.6 GHz
Near-End Crosstalk	NV1_P1_59_P2_61	QFSS_59	QFSS_61	≤ -7dB to 5.6 GHz
	NV2_P1_91_P2_95	QFSS_91	QFSS_95	≤ -14dB to 5.6 GHz
	NV3_P1_91_P2_92	QFSS_91	QFSS_92	≤ -22dB to 5.6 GHz
Far-End Crosstalk	FV1_P1_59_P2_61	QFSS_59	QMSS_61	≤ -18dB to 5.6 GHz
	FV2_P1_91_P2_95	QFSS_91	QMSS_95	≤ -43dB to 5.6 GHz
	FV3-P1_91_P2_92	QFSS_91	QMSS_92	≤ -42dB to 5.6 GHz

Table 3- Differential Pair Signaling - System Performance				
Test Parameter	**File**	**Source**	**Victim**	
Insertion Loss	RLIL_P12_99_101_P34_99_101	port1+2-=QFSS_99-101, port3+4-=QMSS_99-101		-3dB @ 7.0 GHz
Return Loss	RLIL_P12_99_101_P34_99_101	port1+2-=QFSS_99-101, port3+4-=QMSS_99-101		≤-4dB to 7.0 GHz
Near-End Crosstalk	NV2_P12_100_102_P34_96_98	QFSS_100-102	QFSS_96-98	≤-18dB to 7.0 GHz
	NV1_P12_14_16_P34_8_10	QFSS_14-16	QFSS_8-10	≤-25dB to 7.0 GHz
	NV3_P12_99_101_P34_100_102	QFSS_99-101	QFSS_100-102	≤-40dB to 7.0 GHz
Far-End Crosstalk	FV2_P12_100_102_P34_96_98	QFSS_100-102	QMSS_96-98	≤-24dB to 7.0 GHz
	FV1_P12_14_16_P34_8_10	QFSS_14-16	QMSS_8-10	≤-24dB to 7.0 GHz
	FV3_P12_99_101_P34_100_102	QFSS_99-101	QMSS_100-102	≤-39dB to 7.0 GHz

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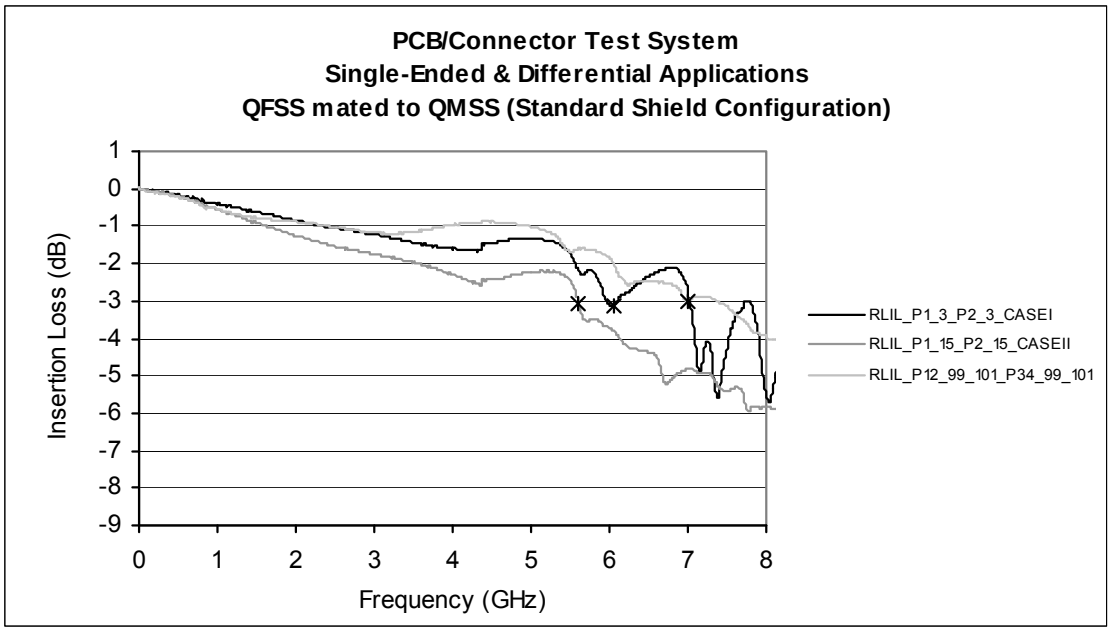
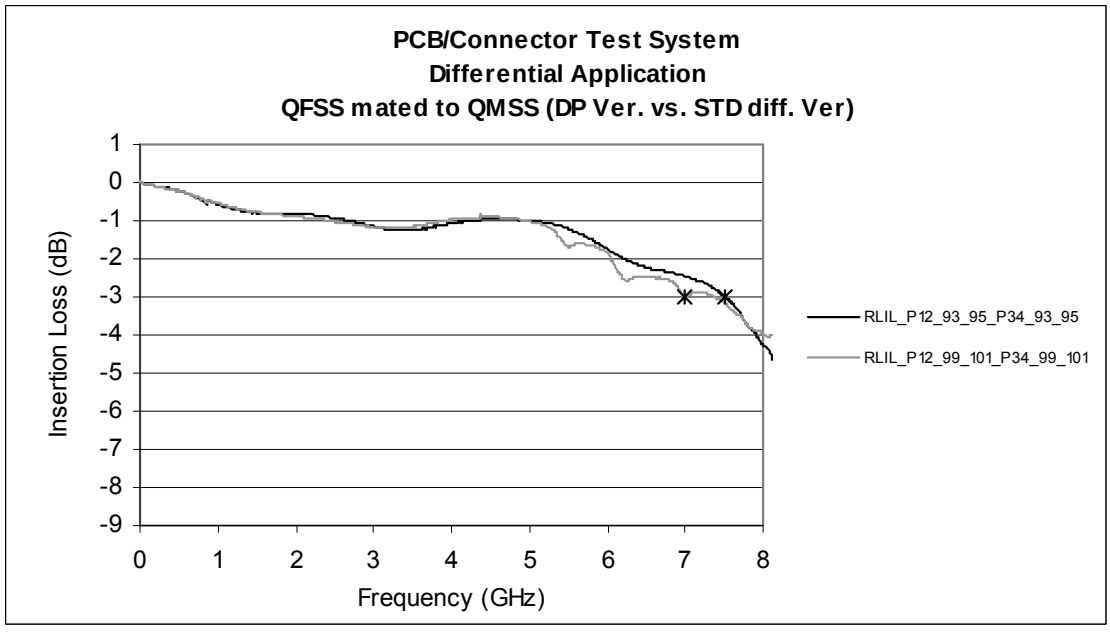
Bandwidth Chart –DP Version & Standard Differential Version





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Time Domain Data Summary

Table 4 – Single-Ended Impedance (Ω) – Case I							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	58.3	55.7	53.5	53.2	53.0	52.8	52.3
Minimum Impedance	40.0	43.9	47.5	50.4	51.4	51.8	51.8

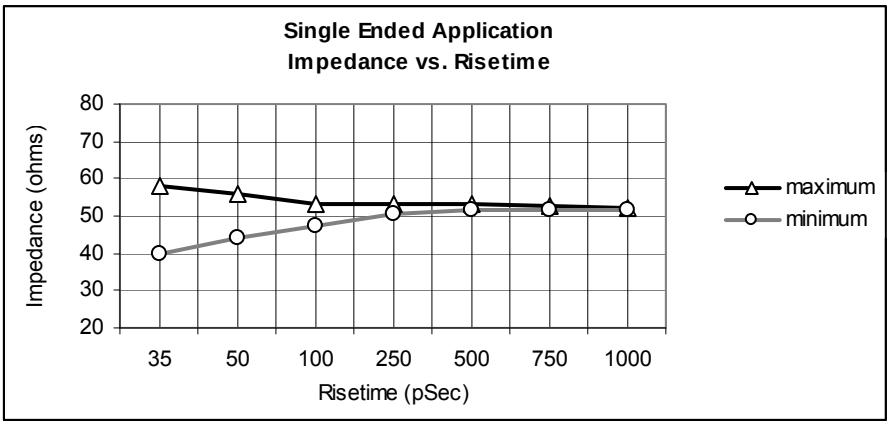

Table 5 – Single-Ended Impedance (Ω) – Case II							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	60.4	59.1	54.8	53.1	52.9	52.6	52.3
Minimum Impedance	39.3	43.9	48.3	51.2	51.9	52.1	52.1

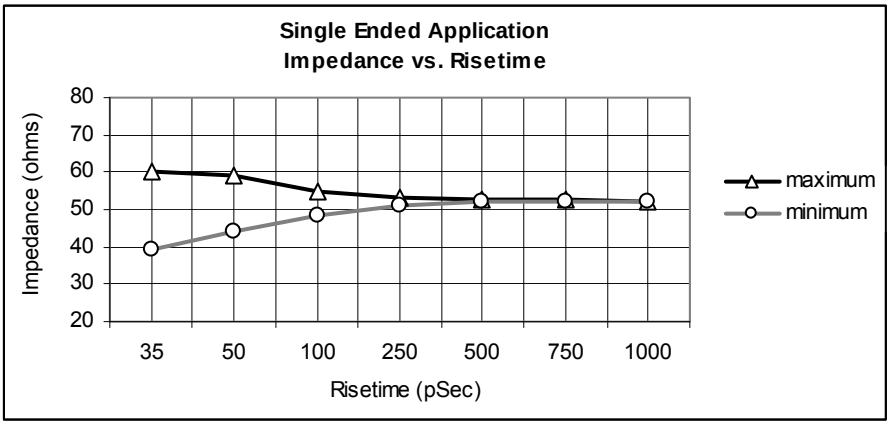

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Table 6 - Differential Crosstalk (%)

Input (t_r)	Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	QFSS_100-102	QFSS_96-98	5.2	5.0	4.5	3.0	1.9	1.3	1.1
	QFSS_14-16	QFSS_8-10	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	QFSS_99-101	QFSS_100-102	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	QFSS_100-102	QMSS_96-98	3.2	2.1	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	QFSS_14-16	QMSS_8-10	2.1	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	QFSS_99-101	QMSS_100-102	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay

Configuration		Signal Path	Mated Connector Only
Single-Ended, Case I	Ch3 to Ch5	probe 3=QFSS_3, probe 5=QMSS_3	82ps
Single-Ended, Case II	Ch3 to Ch5	probe 3=QFSS_15, probe 5=QMSS_15	77ps
Differential Pair	Ch56 to Ch34	QFSS-DP_93-95, QMSS-DP_93-95	80ps

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Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. However, other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provision must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others; connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So, care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

For this connector, the following array configurations are evaluated:

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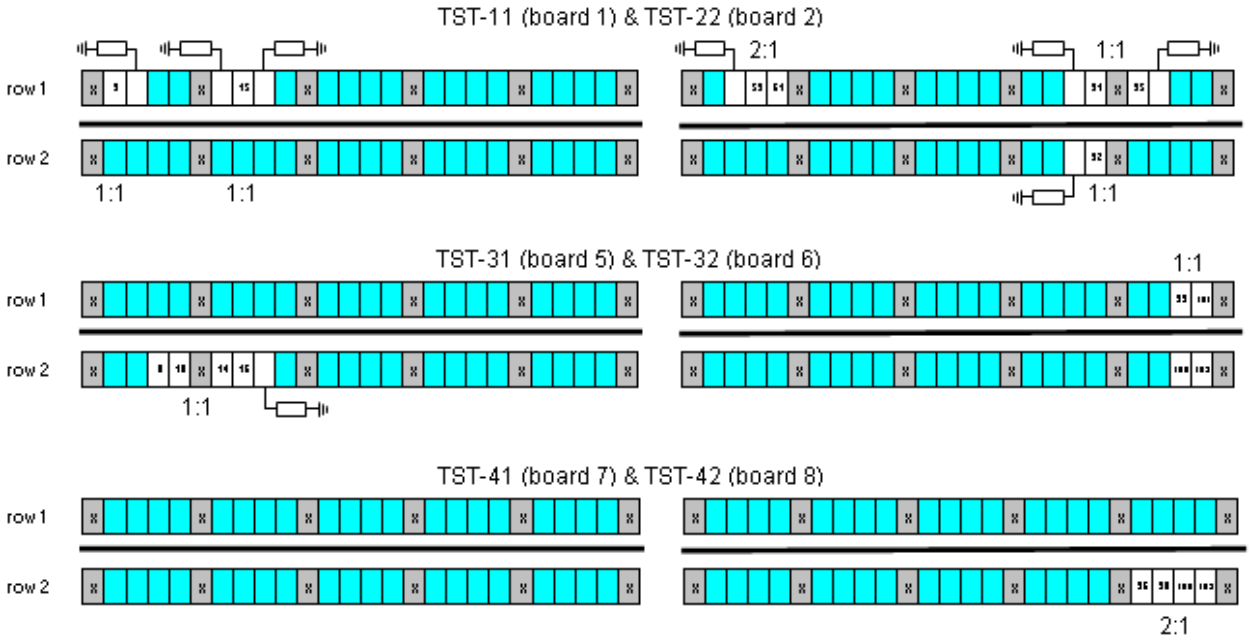
grounded pin field x shield ground pin

P# signal aggressor or signal victim pins



Single-Ended Impedance:

- Well-referenced line; 1:1, S:G ratio

Single-Ended Crosstalk:

- Well-referenced line; mimics 1:1 S:G ratio
- 2:1 S:G ratio

Only one single-ended signal was driven for crosstalk measurements.

Differential Impedance:

- Well-referenced line 1:1, S:G ratio

Differential Crosstalk:

- Well-referenced line; mimics 1:1 S:G ratio
- Higher Signal Density, 2:1 S:G ratio
- Full-Row Differential

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Only one differential pair was driven for crosstalk measurements.

*In all cases where a center ground blade is present in the connector it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect, can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 35 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data
Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT's frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

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Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 35 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 35 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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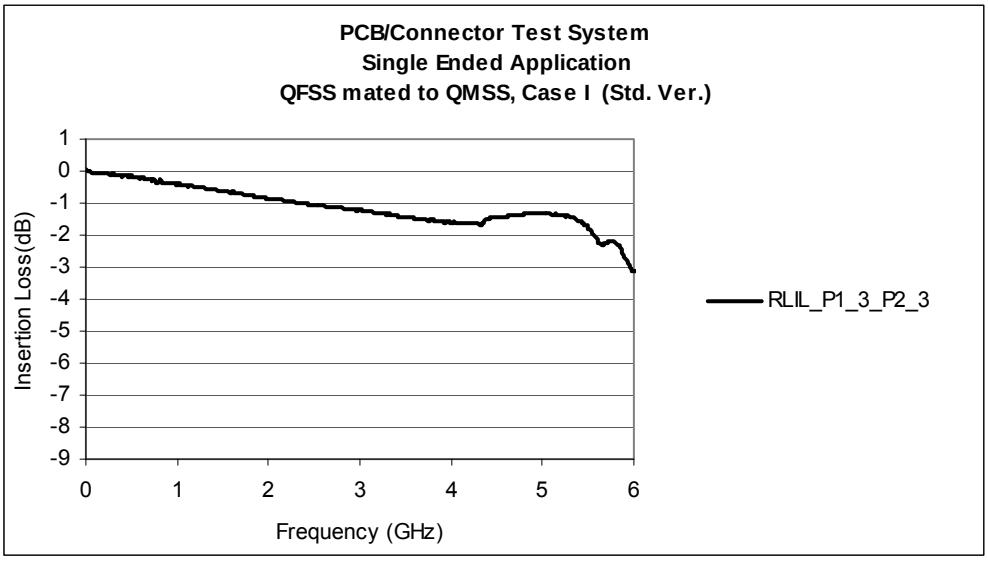
Appendix A – Frequency Domain Response Graphs

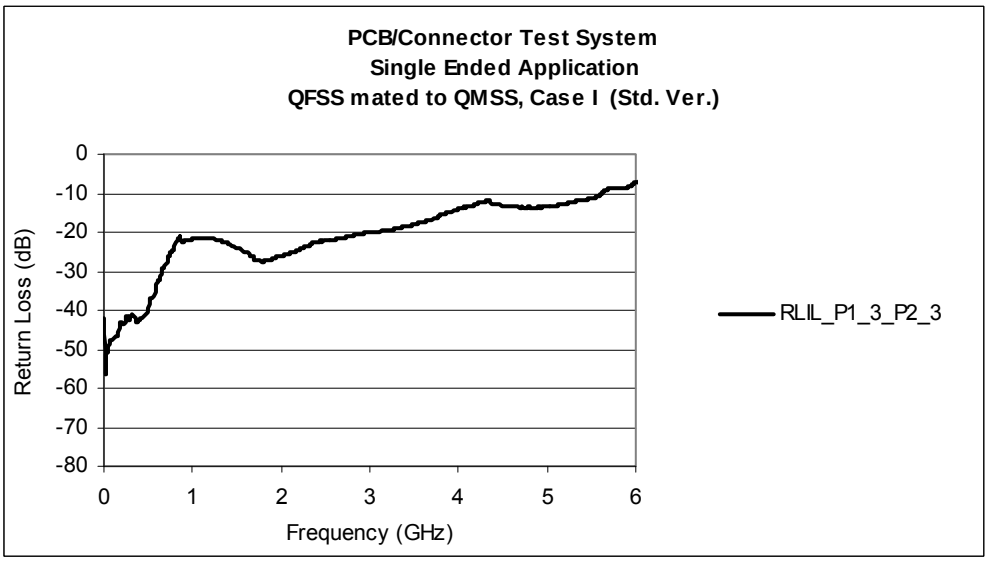
Single-Ended Application – Insertion Loss, Case I

Configuration: port 1=QFSS_3, port 3=QMSS_3



Single-Ended Application – Return Loss, Case I

Configuration: port 1=QFSS_3, port 3=QMSS_3



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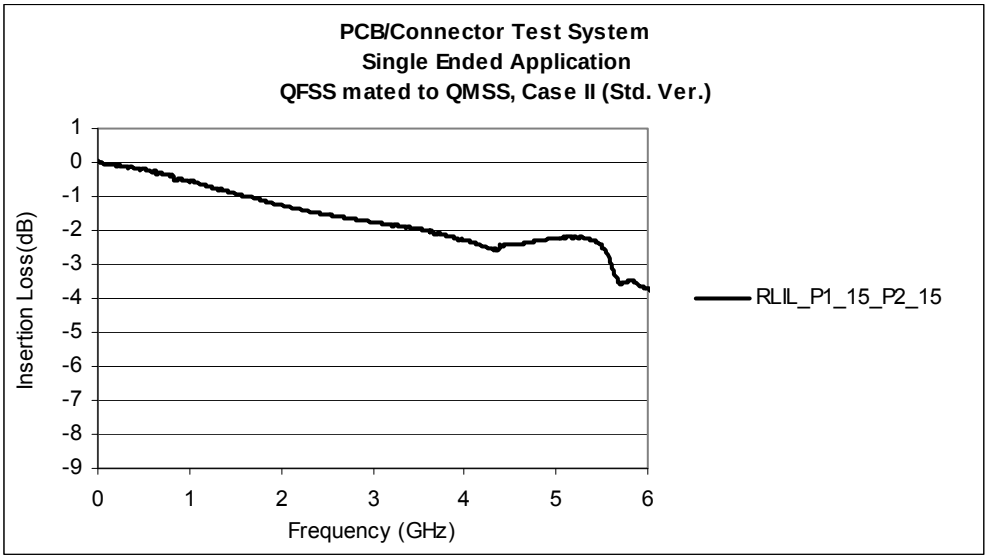
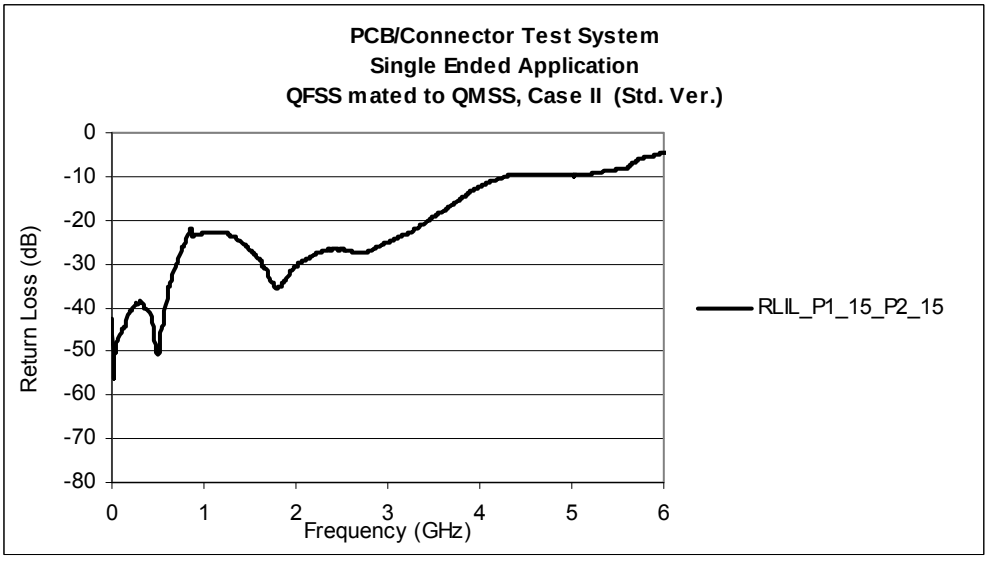
Single-Ended Application – Insertion Loss, Case II

Configuration: port 1=QFSS_15, port 3=QMSS_15



Single-Ended Application – Return Loss, Case II

Configuration: port 1=QFSS_15, port 3=QMSS_15



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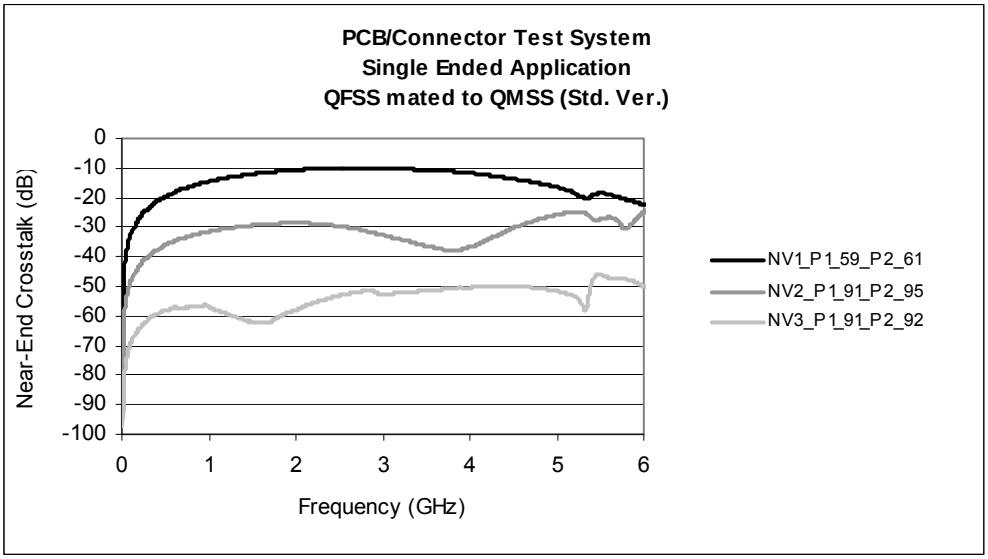
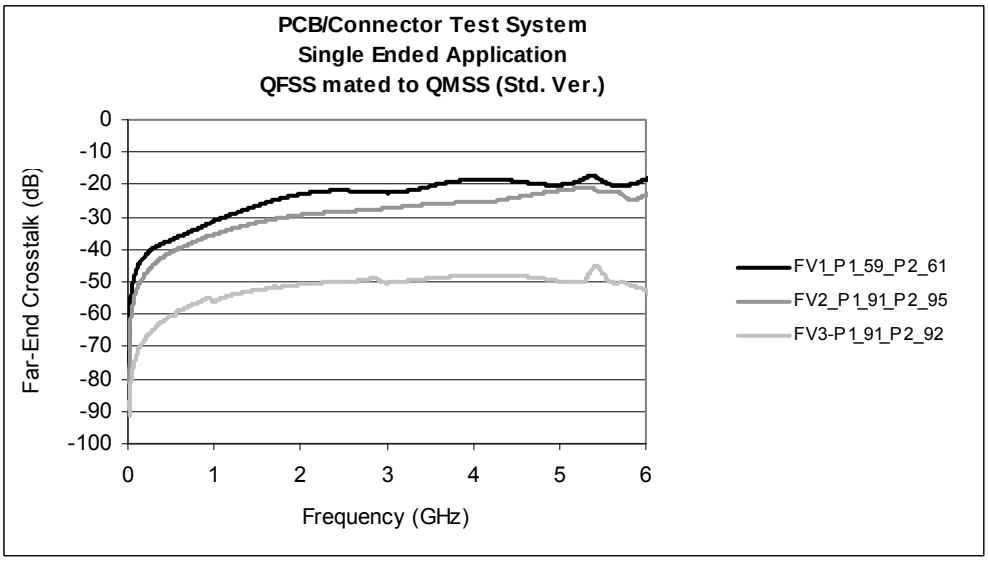
Single-Ended Application – NEXT Configurations

QFSS_59 QFSS_61
QFSS_91 QFSS_95
QFSS_91 QFSS_92



Single-Ended Application – FEXT Configurations

QFSS_59 QMSS_61
QFSS_91 QMSS_95
QFSS_91 QMSS_92



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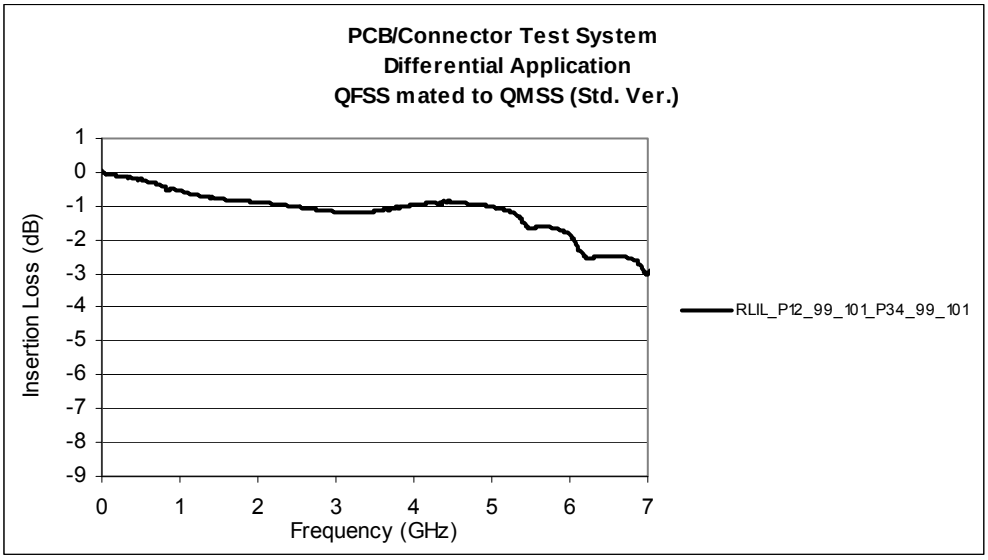
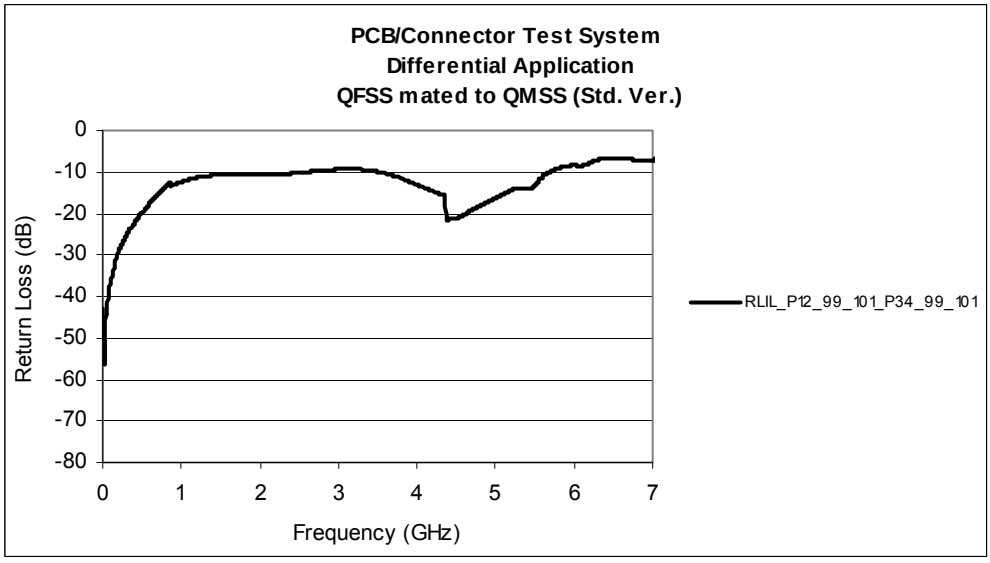
Differential Application – Insertion Loss

Configuration: port12=QFSS_99-101, port34=QMSS_99-101



Differential Application – Return Loss

Configuration: port12=QFSS_99-101, port34=QMSS_99-101



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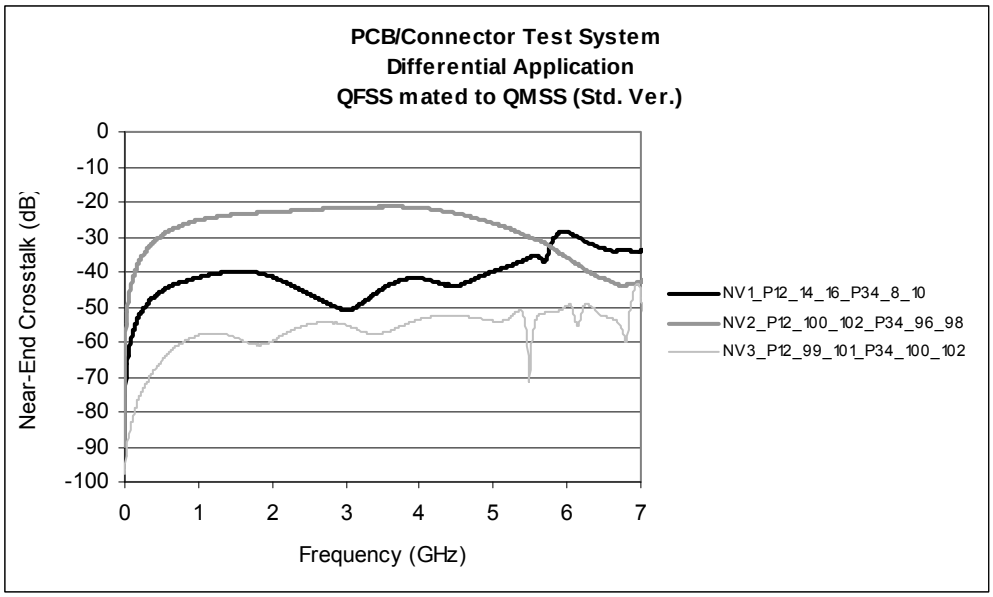
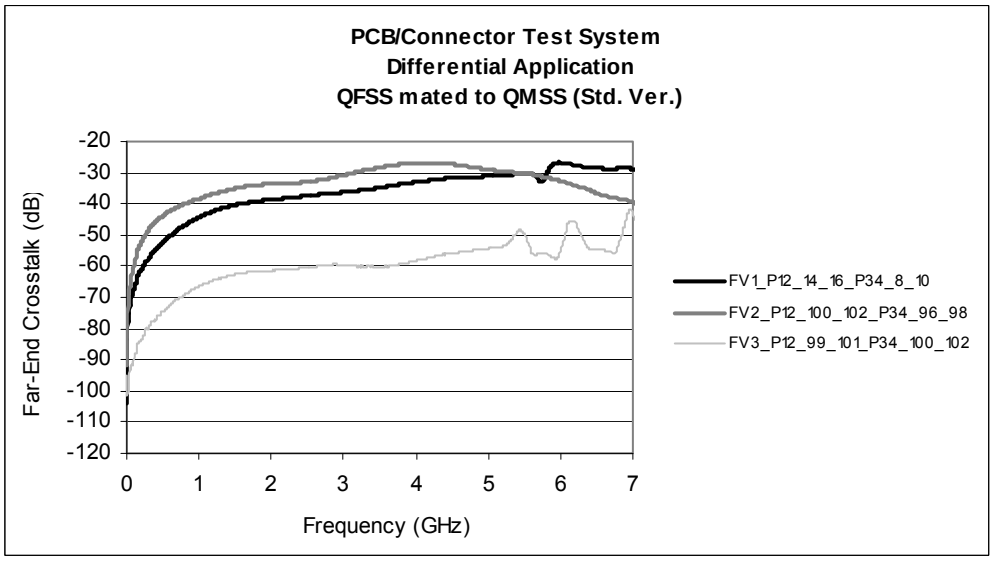
Differential Application – NEXT Configurations

QFSS_100-102 QFSS_96-98
QFSS_14-16 QFSS_8-10
QFSS_99-101 QFSS_100-102



Differential Application – FEXT Configurations

QFSS_100-102 QMSS_96-98
QFSS_14-16 QMSS_8-10
QFSS_99-101 QMSS_100-102



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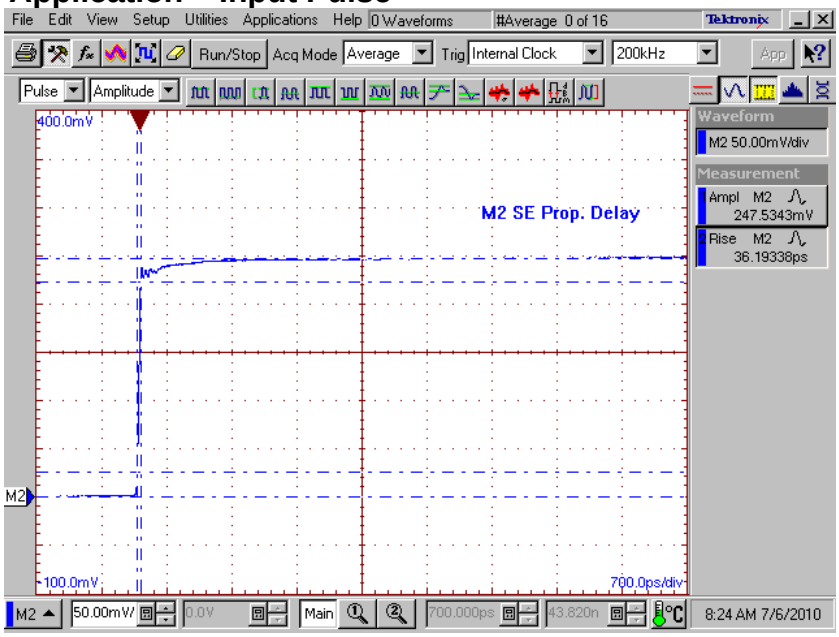
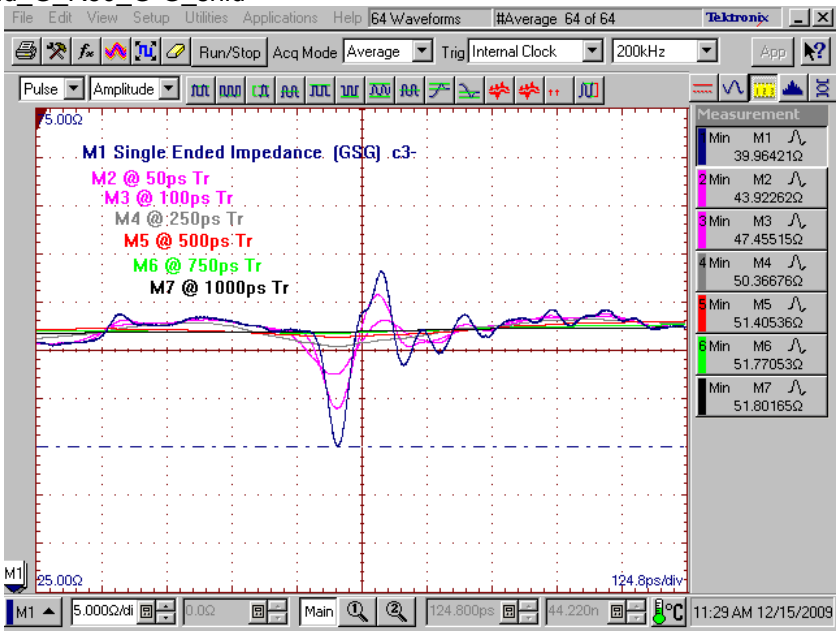
Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse



Single-Ended Application – Impedance, Case I

Test Point 3, shld_G_R50_G-G_shld



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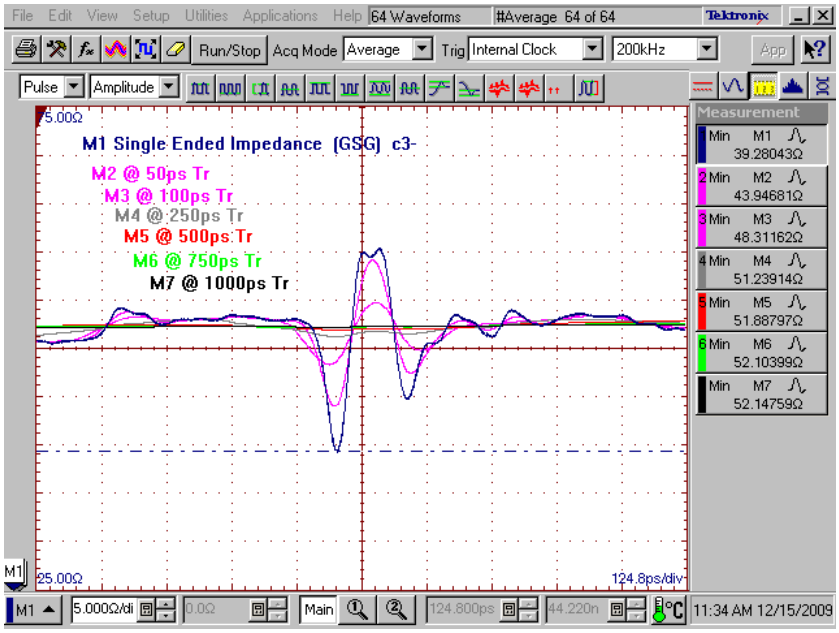
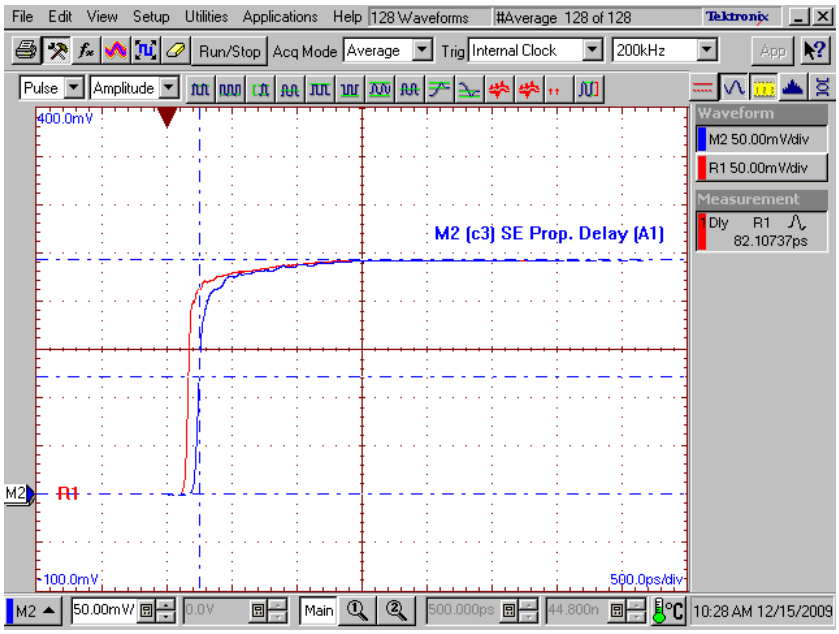
Single-Ended Application – Impedance, Case II

Test Point 15, shld_R50_G_R50_G_shld



Single-Ended Application – Propagation Delay, Case I

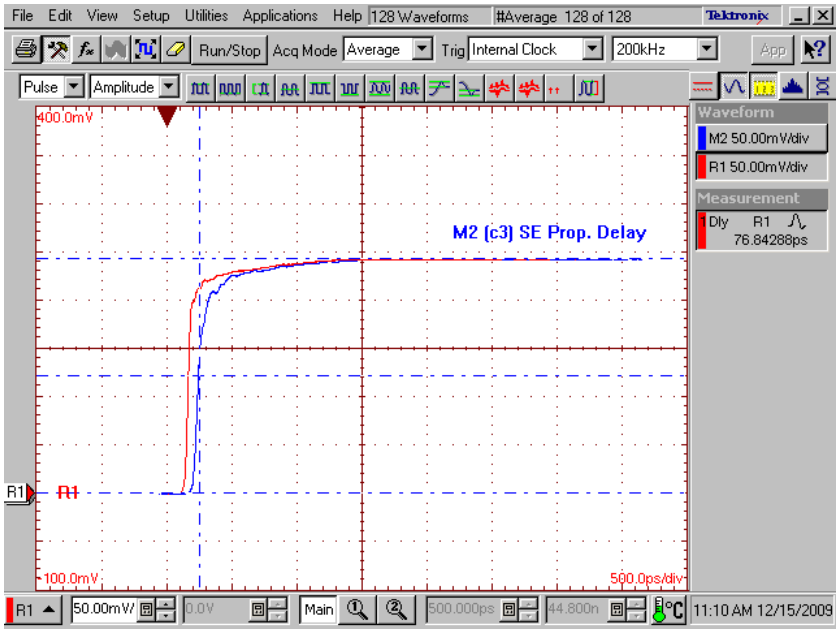
Test Point 3, shld_G_R50_G-G_shld



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

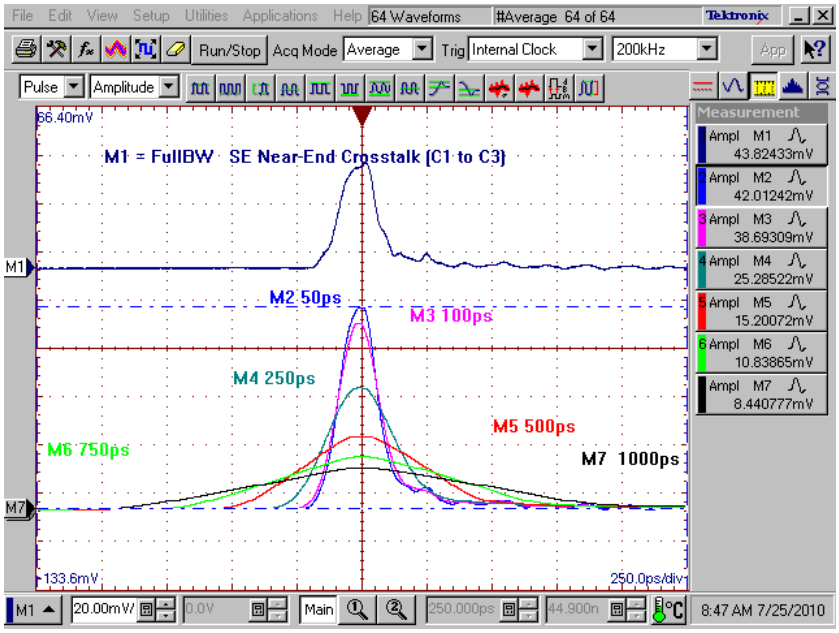
Single-Ended Application – Propagation Delay, Case II

Test Point 15, shld_R50_G_R50_G_shld



Single-Ended Application – NEXT, "Worst Case" Configuration

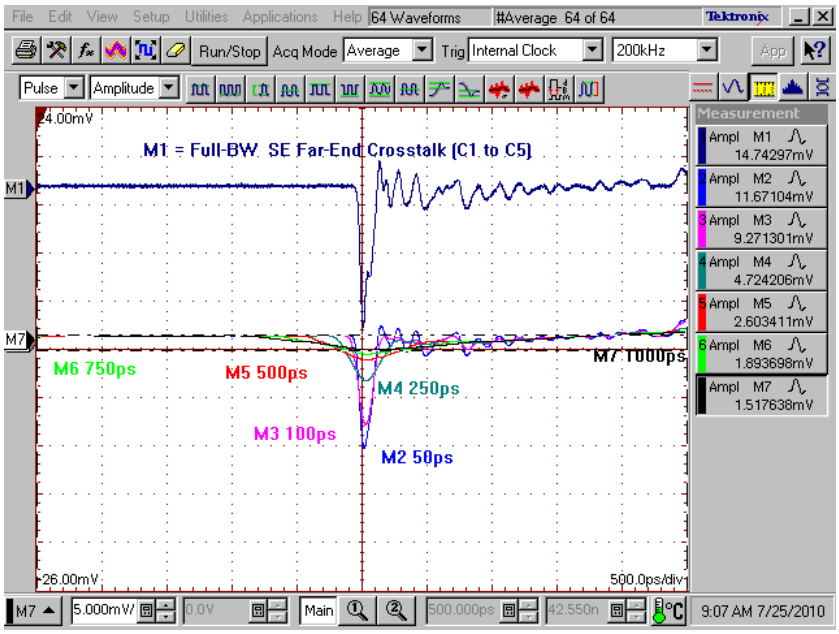
QFSS_59 QFSS_61



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

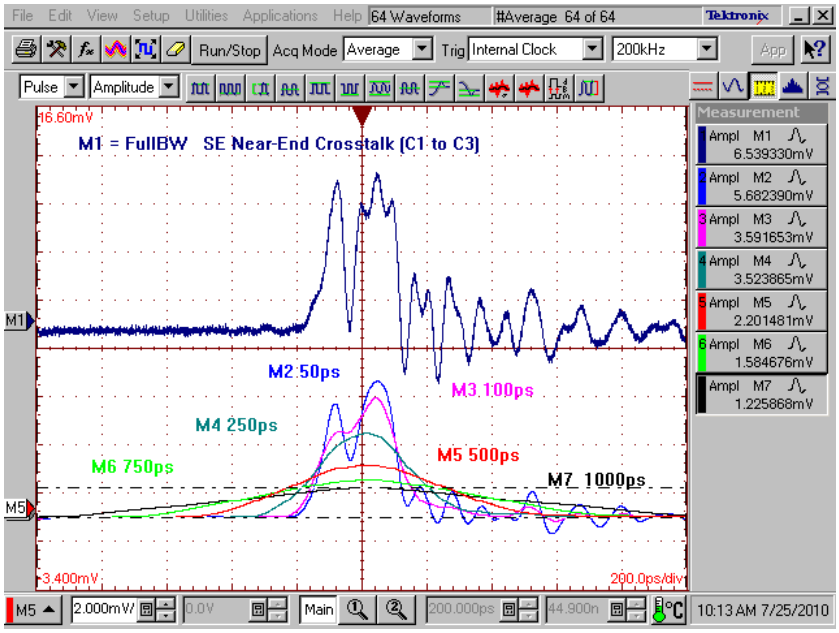
Single-Ended Application – FEXT, "Worst Case" Configuration

QFSS_59 QMSS_61



Single-Ended Application – NEXT, "Best Case" Configuration

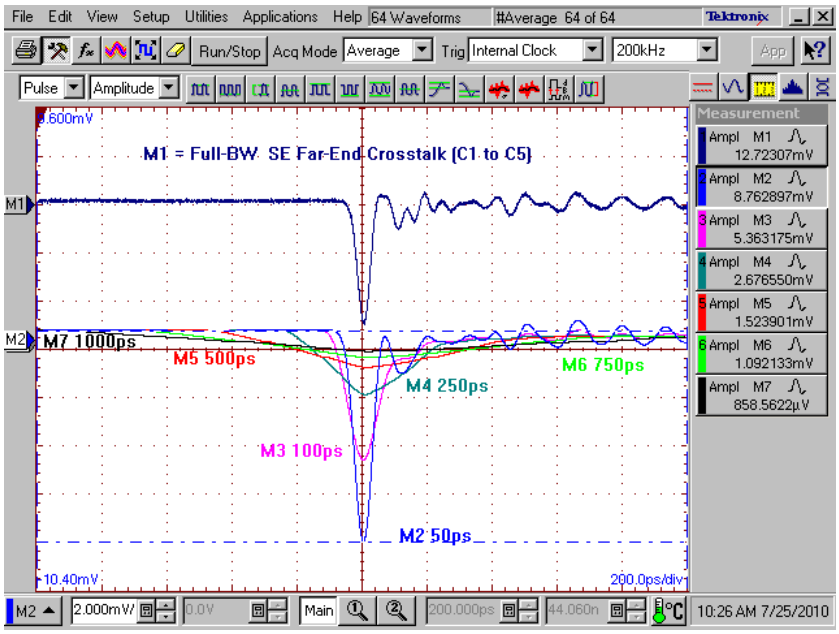
QFSS_91 QFSS_95



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

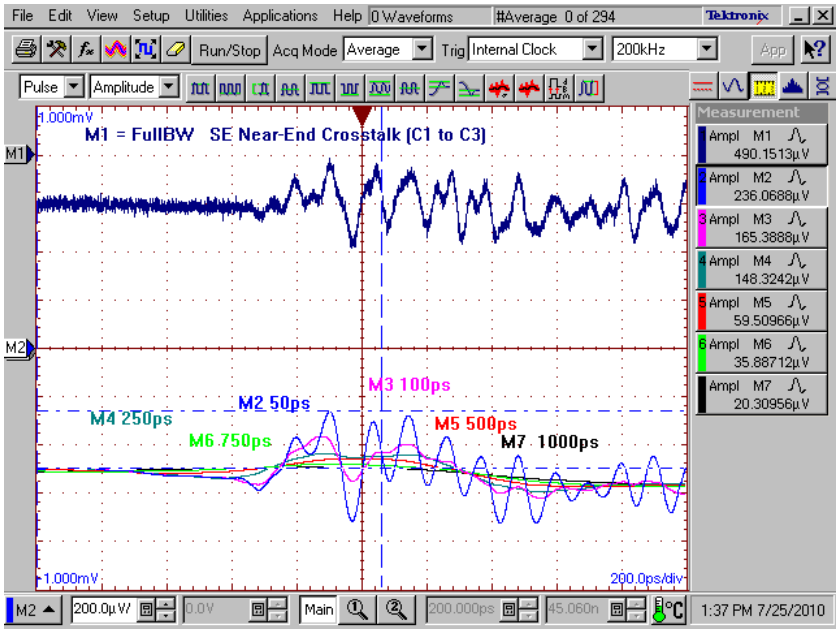
Single-Ended Application – FEXT, "Best Case" Configuration

QFSS_91 QMSS_95



Single-Ended Application – NEXT, "Across Row" Configuration

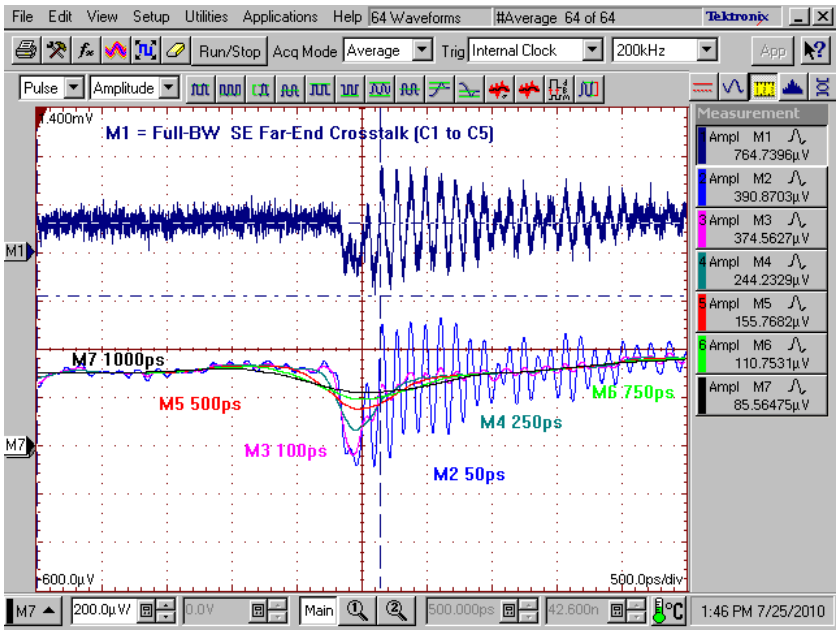
QFSS_91 QFSS_92



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

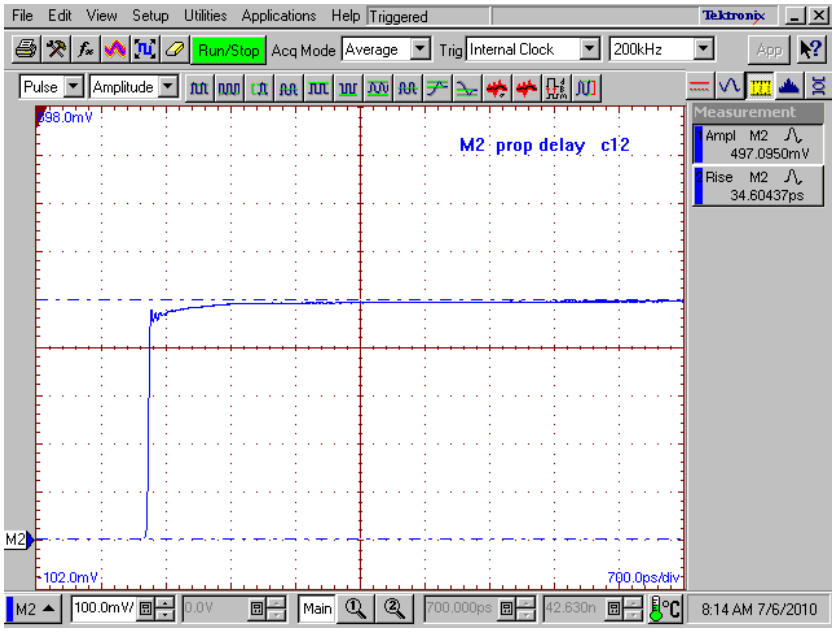
Single-Ended Application – FEXT, "Across Row" Configuration

QFSS_91 QMSS_92



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

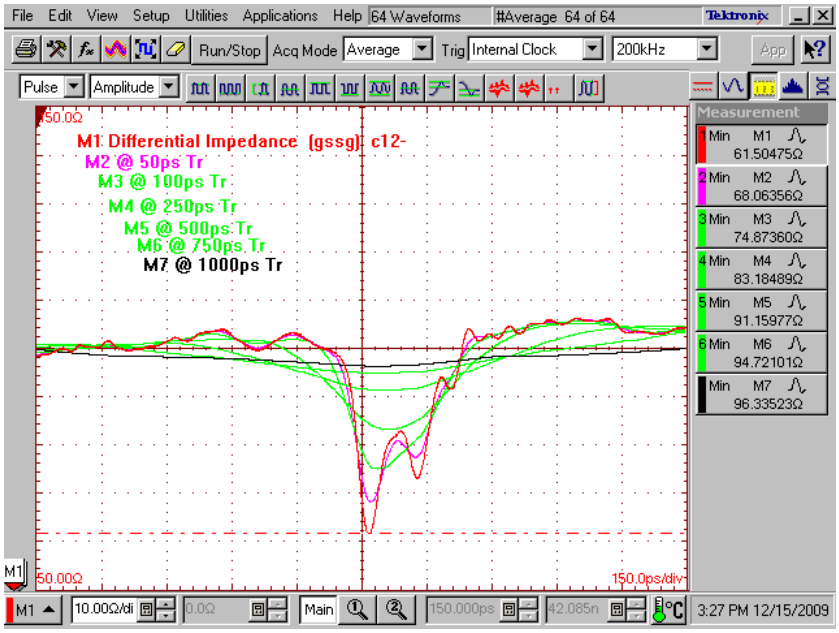
Differential Application – Input Pulse



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

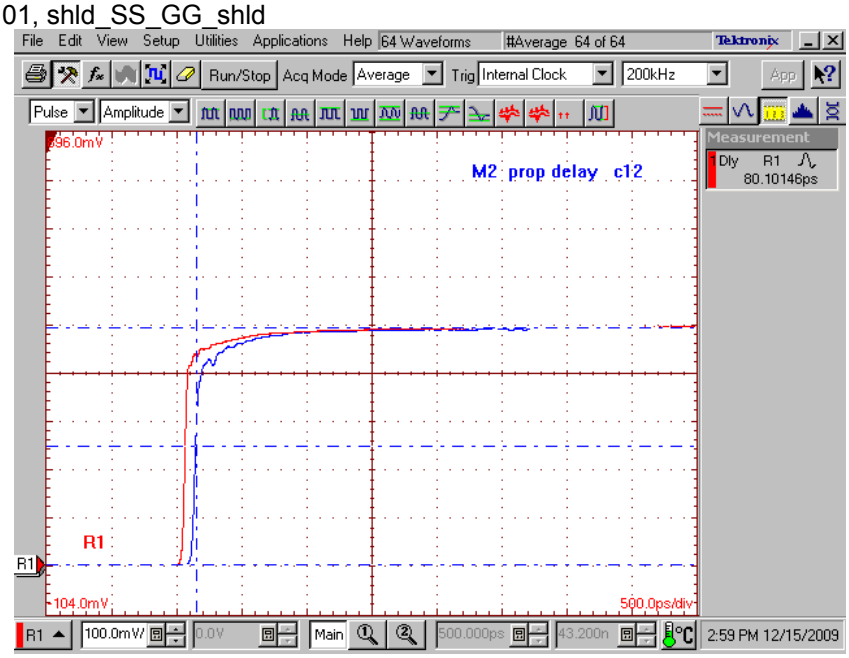
Differential Application – Impedance

Test Point 99-101, shld_SS_GG_shld



Differential Application – Propagation Delay

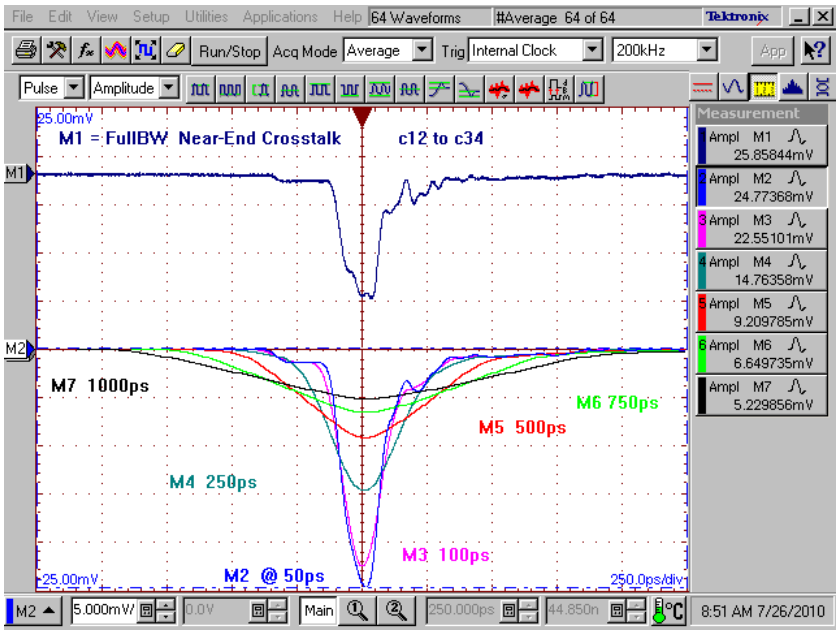
Test Point 99-101, shld_SS_GG_shld



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

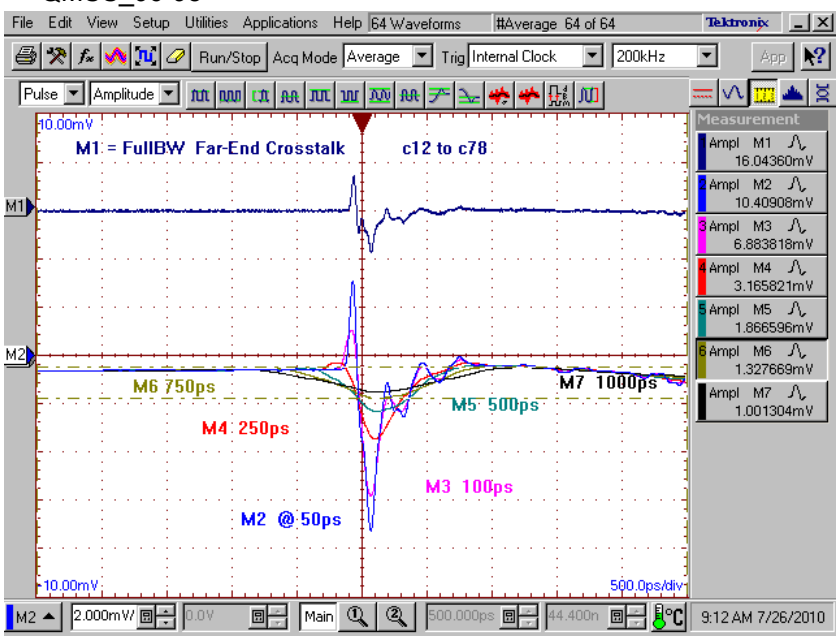
Differential Application – NEXT, "Worst Case" Configuration

QFSS_100-102 QFSS_96-98



Differential Application – FEXT, "Worst Case" Configuration

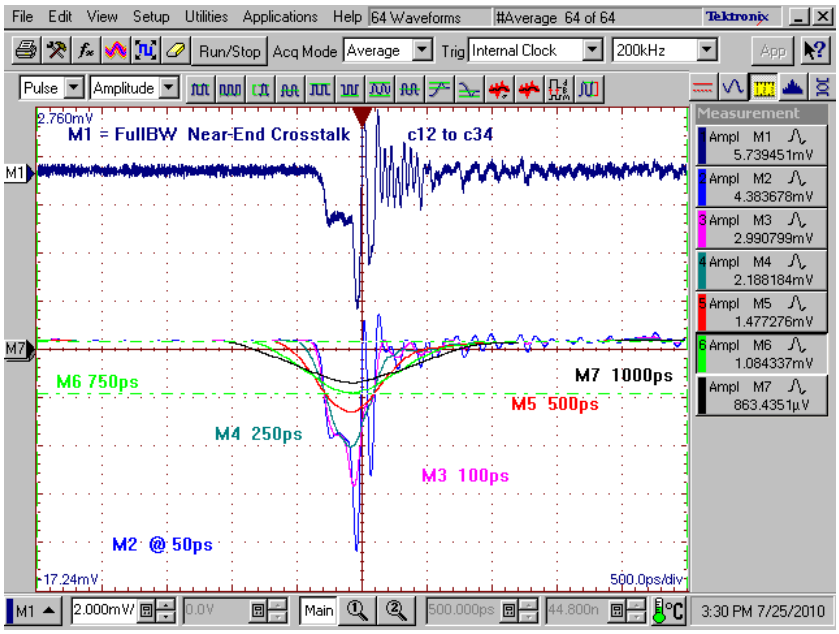
QFSS_100-102 QMSS_96-98



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

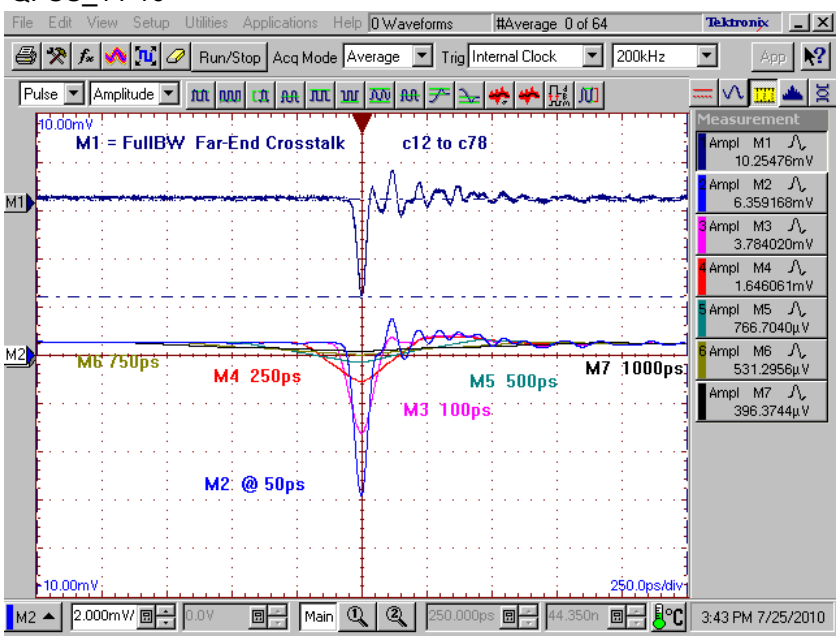
Differential Application – NEXT, "Best Case" Configuration

QFSS_14-16 QFSS_14-16



Differential Application – FEXT, "Best Case" Configuration

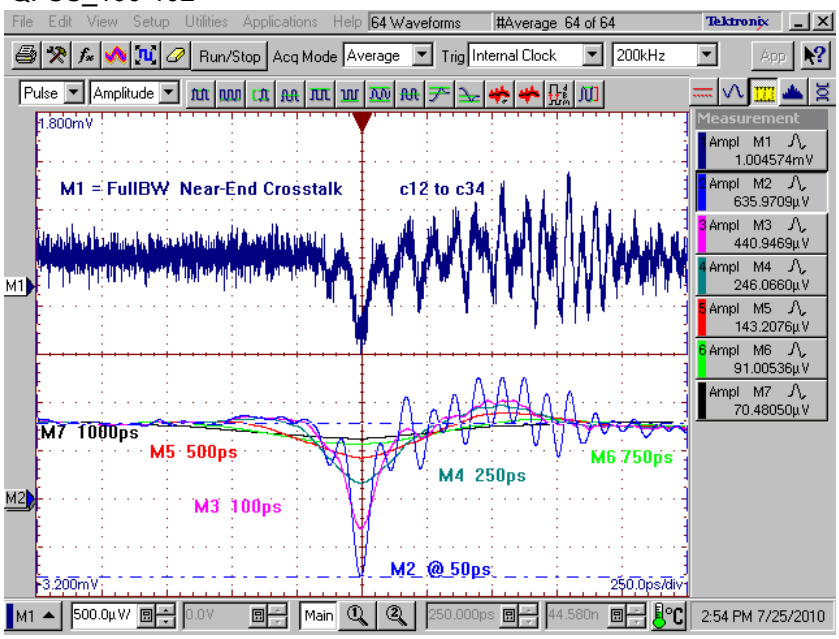
QFSS_14-16 QFSS_14-16



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

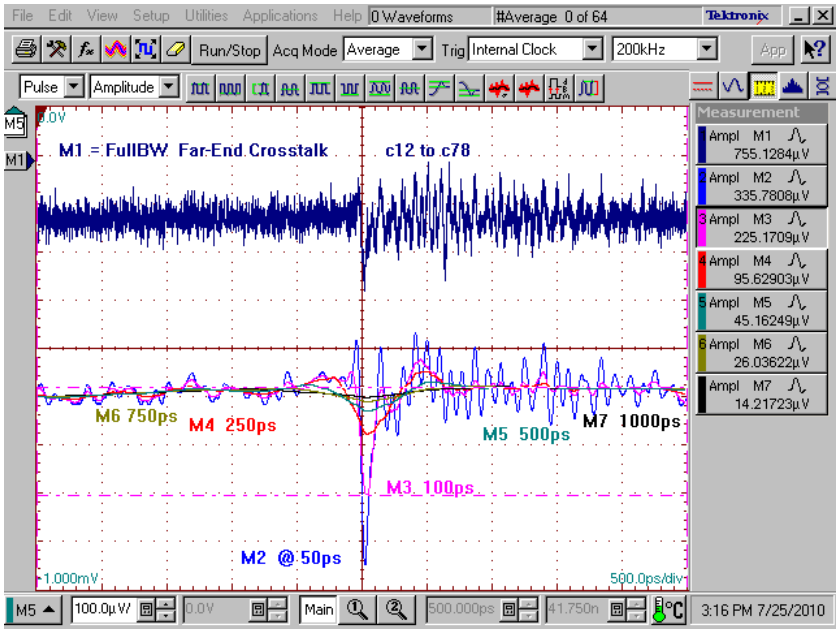
Differential Application – NEXT, "Across Row" Configuration

QFSS_99-101 QFSS_100-102



Differential Application – FEXT, "Across Row" Configuration

QFSS_99-101 QMSS_100-102



Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

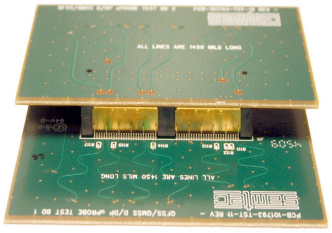
Appendix C – Product and Test System Descriptions

Product Description

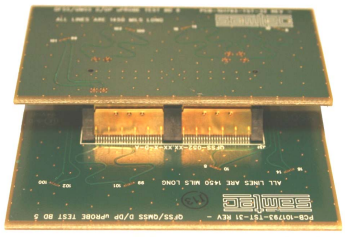
Q2 is a shielded two row surface mount connector with polarized mating. Test fixtures utilize the QFSS-052-01-L-D-A shielded socket connector and the QMSS-052-01-L-D-A shielded terminal connector. In addition, the standard Q2 version features a GSSSSG shielding configuration where every fifth terminal pin is a shield ground. When mated an 11mm (.433") stack height exists between the connector mounting surfaces. Terminal centerlines are spaced at a 0.635mm (.025") pitch.

Test System Description

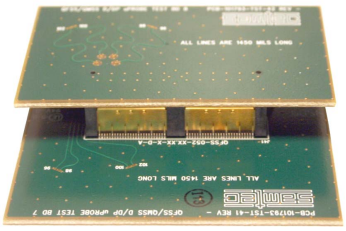
Test fixtures are composed of 4-layer FR-406 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. When mated electrical continuity exists between socket side and terminal side like numbered launch points. TRL *(PCB1010793-TST-98)* type and TDA *(PCB1010793-TST-99)* type calibration boards' are utilized in the characterization of the standard Q2 shielded connector. All data and waveforms presented are results from a socket side launch. Page 25 depicts assembled test fixtures. The standard shielded Q2



SE Signaling – Boards 1& 2



Diff. Signaling – Boards 5 & 6

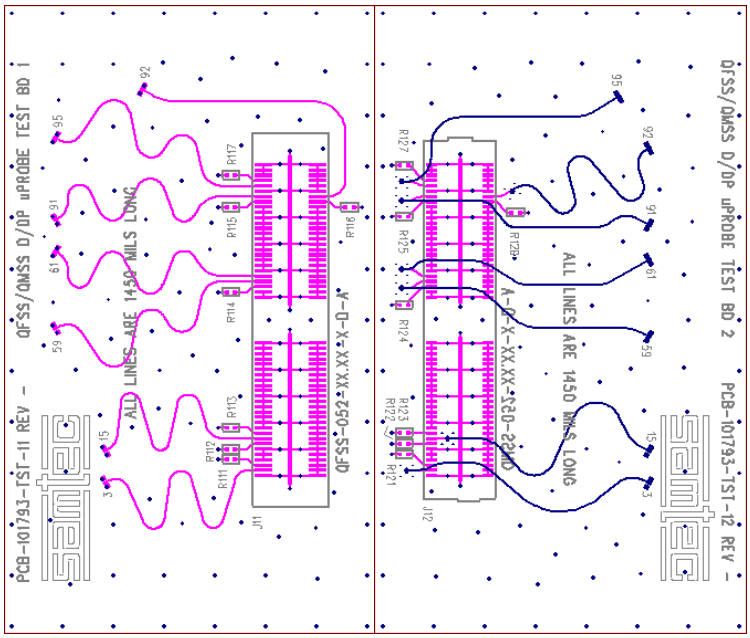


Diff. Signaling – Boards 7 & 8

GSSSSG configured connector test system mates as follows;

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

PCB-101793-TST, Single-Ended Signal Mapping, Set I



Fixture Identity – Standard GSSSSG Configuration

Board No.	PCB-101793-TST-11	Socket:	QFSS-052-01-L-D -A
	PCB-101793-TST-12	Terminal:	QMSS-052-01-L-D -A

Transmission and Reflection Test Parameters:

Insertion Loss, Return Loss, Impedance, Propagation Delay

Tx, port 1=QFSS_3, Rx, port 3=QMSS_3, Case I
Tx, port 1=QFSS_15, Rx, port 3=QMSS_15, Case II

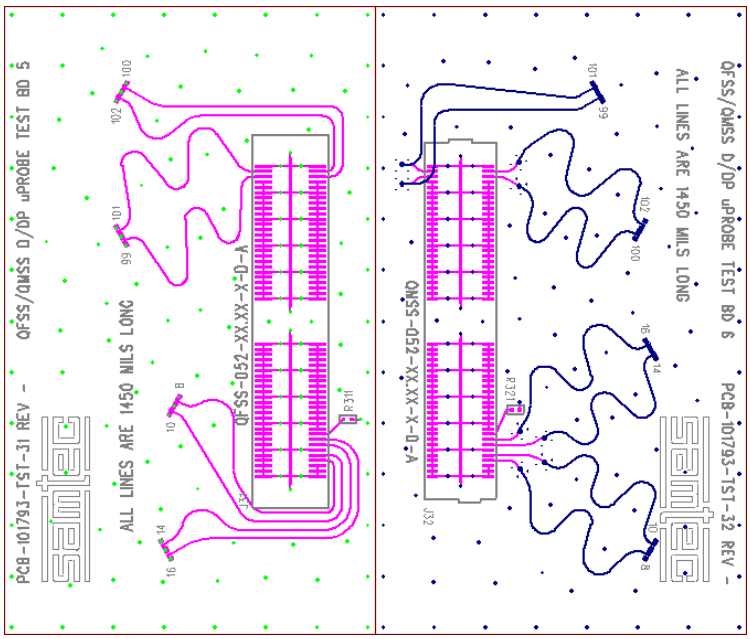
Crosstalk Frequency & Time Domain Response Parameters, NEXT, FEXT

Signal to Ground Ratio

Case 1 2:1, S:G	Near-End Aggressor: Far-End Aggressor:	QFSS_59 QFSS_59	Victim: Victim:	QFSS_61 QMSS_61
Case 2 1:1, S:G	Near-End Aggressor: Far-End Aggressor:	QFSS_91 QFSS_91	Victim: Victim:	QFSS_95 QMSS_95
Case 3 1:1, S:G	Near-End Aggressor: Far-End Aggressor:	QFSS_91 QFSS_91	Victim: Victim:	QMSS_92 QMSS_92

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

PCB-101793-TST, Differential Pair Signal Mapping, Set III



Fixture Identity – Standard GSSSSG Configuration

Board No.	PCB-101793-TST-31	Socket:	QFSS-052-01-L-D -A
	PCB-101793-TST-32	Terminal:	QMSS-052-01-L-D -A

Transmission and Reflection Test Parameters:

Insertion Loss, Return Loss, Impedance, Propagation Delay

Tx, port1+2-=QFSS_99-101, Rx, port3+4-=QMSS_99-101

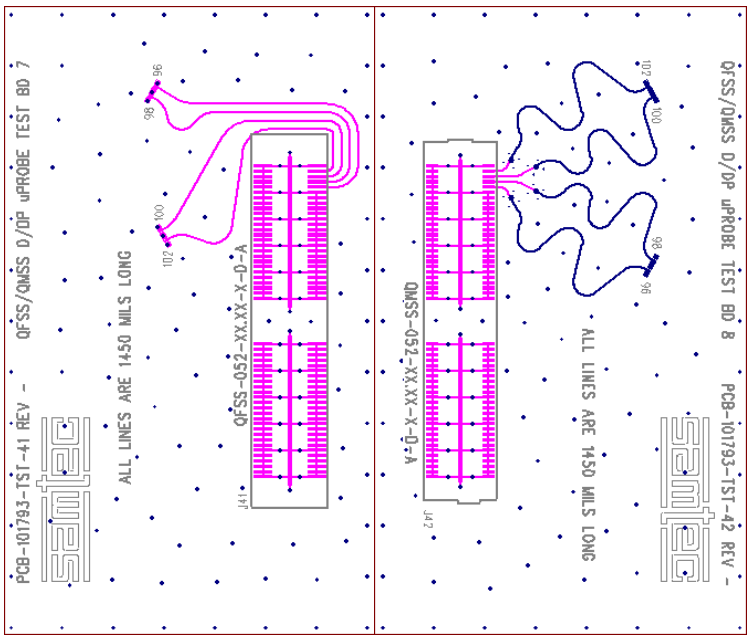
Crosstalk Frequency & Time Domain Response Parameters, NEXT, FEXT

Signal to Ground Ratio

Case 1 2:1, S:G	Near-End Aggressor: Far-End Aggressor:		Victim: Victim:	
Case 2 1:1, S:G	Near-End Aggressor: Far-End Aggressor:	QFSS_14-16 QFSS_14-16	Victim: Victim:	QFSS_8-10 QMSS_8-10
Case 3 1:1, S:G	Near-End Aggressor: Far-End Aggressor:	QFSS_99-101 QFSS_99-101	Victim: Victim:	QFSS_100-102 QMSS_100-102

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

PCB-101793-TST, Differential Pair Signal Mapping, Set IV



Fixture Identity – Standard GSSSSG Configuration

Board No.	PCB-101793-TST-41	Socket:	QFSS-052-01-L-D -A
	PCB-101793-TST-42	Terminal:	QMSS-052-01-L-D -A

Transmission and Reflection Test Parameters:

Insertion Loss, Return Loss, Impedance, Propagation Delay

Tx, Rx,

Crosstalk Frequency & Time Domain Response Parameters, NEXT, FEXT

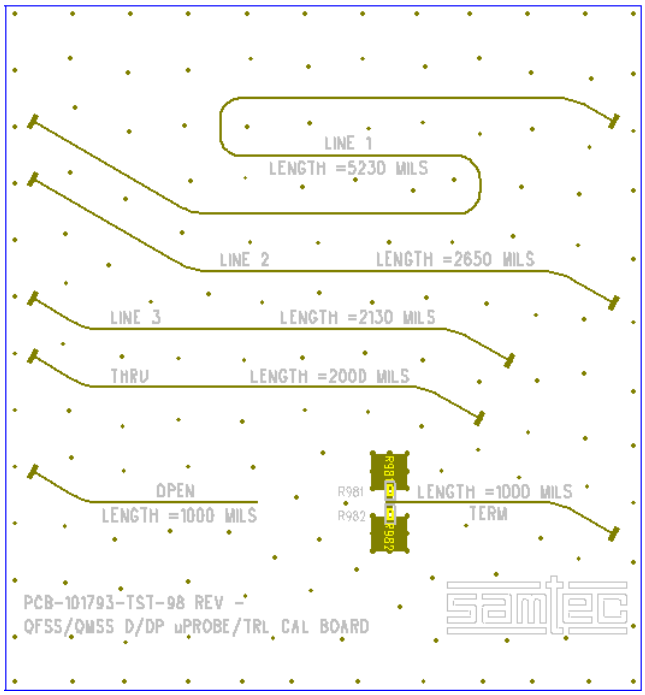
Signal to Ground Ratio

Case 1 2:1, S:G	Near-End Aggressor: Far-End Aggressor:	QFSS_100-102 QFSS_100-102	Victim: Victim:	QFSS_96-98 QMSS_96-98
Case 2 1:1, S:G	Near-End Aggressor: Far-End Aggressor:		Victim: Victim:	
Case 3 1:1, S:G	Near-End Aggressor: Far-End Aggressor:		Victim: Victim:	

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

TRL De-Embedding Calibration Board

Through-Reflect-Line Standards:



Line 1, 5230mils, Δ Delay = 477.9pSec
Bandwidth 175 MHz to 865 MHz

Line 2, 2650mils, Δ Delay = 96.7pSec
Bandwidth 860 MHz to 4363MHz

Line 3, Δ Delay = 19.7pSec
Bandwidth 4275MHz to 20000MHz

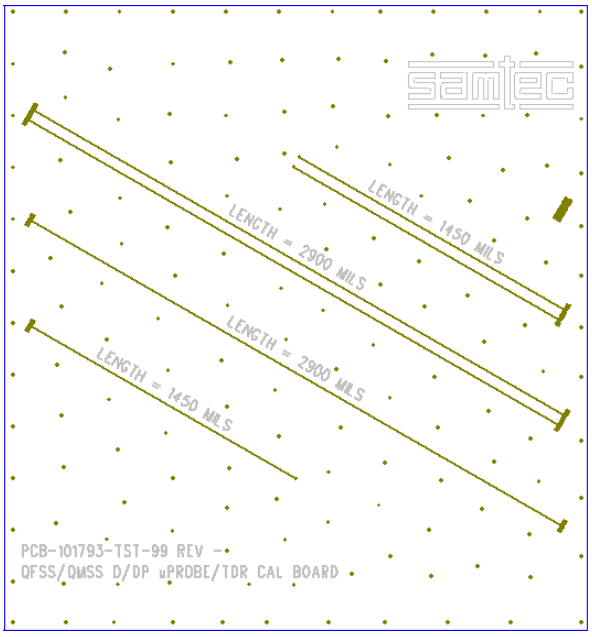
Thru, 2000mils, Delay = 0pSec
Bandwidth DC to 20000MHz

Open, 1000mils
Bandwidth DC to 20000MHz

Load, 1000mils
Bandwidth DC to 200MHz

Δ Delay = Thru – Line #

TDA Micro-Probe Calibration Board



Propagation Delay Thru Length
Differential, 2900 mils

Propagation Delay Thru Length
Single-Ended, 2900 mils

TDA Step Waveform
Transmission/Reflection Standard
Reference PCB101793_TST-99 Cal Board

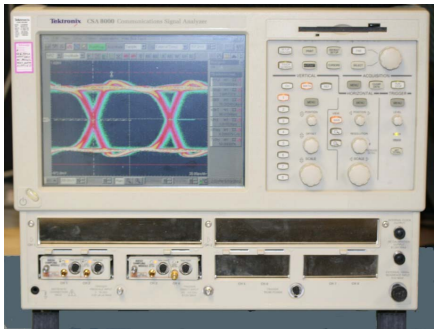
Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

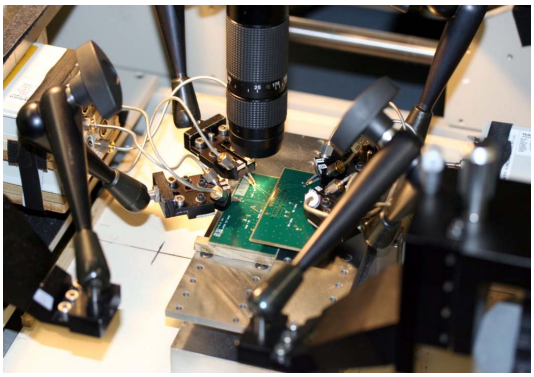
Appendix D – Test and Measurement Setup

Characterization instruments are the Agilent 5230A 4-port PNA analyzer and the Tektronix CSA8000 Communication Signal Analyzer utilizing four Tektronix 80E04 TDR/Sampling Heads. Test sample probing employs a Keyence Video Microscopy system, a Giga Test Labs probing station and Picoprobe 40GHz capable microprobes. Picoprobes' four hundred and fifty micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available on both the probe table and articulating micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a ≥18 dB return loss, and an isolation of 38 dB providing high-bandwidth and low parasitic measurement results. Combined, the above technology provides a stable measurement environment along with the electrical accuracies for obtaining precise calibrations and signal launch capabilities.

Currently the data captured is real time (CSA8000) which is post-processed to s-parameter results employing TDA IConnect modeling software. However, either instrument capabilities allow for automated capturing, post-processing and graphical waveform representation in both domains. In a move towards full s-parameter reporting, future SI characterization reports will include frequency based PNA generated s-parameters utilizing the advantage of SOLT or TRL calibration accuracy. This series of tests incorporates PNA generated s-parameters and utilizes TRL calibration techniques. By employing these TRL calibration techniques, PCB effects previously inclusive are theoretically de-embedded from measurements. Data results for this test will include effects from the mated connector, the PCB footprint and approximately 100mils of signal trace. Overall connector performance should improve based on the elimination of lossy PCB effects. For now, Appendix E retains TDA IConnect procedures and adds initial procedures for a TRL type calibration. Until full implementation of the ADS formats, timing based measurements such as, Impedance, Propagation Delay and Digital Crosstalk continue to be generated by the CSA8000 test system. Frequency based measurements such as, Insertion Loss; Return Loss and RF Crosstalk results are generated utilizing the PNA analyzer and TRL type calibration.

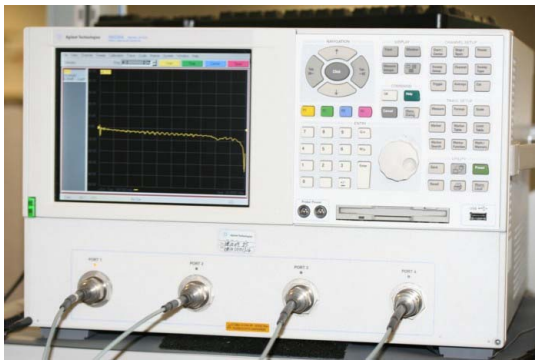
CSA8000 Time Domain Test Setup

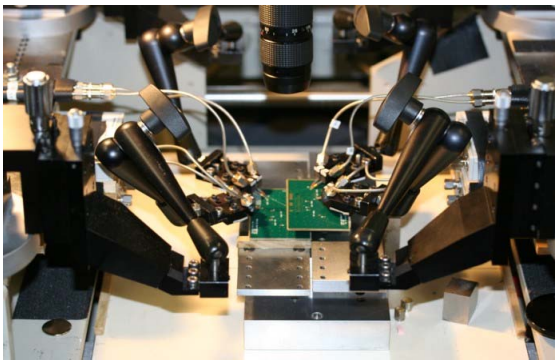




Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

N5230A Frequency Domain (S-Parameter) Test Setup





Test Instruments

QTY	Description
1	Agilent N5230A PNA 300KHz to 20 GHz
1	Tektronix CSA8000 Communication Signal Analyzer
4	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Probe Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
4	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG
1	GGB Industries CS-9 Calibration Substrate (SOLT standards)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

QTY	Description
8	Pasternack Enterprises 2.9mm Semi-Rigid (.086) 6" Cable Assemblies (4)
4	MegaPhase CM40-K1K2-48 Chip Set Cables (40GHz)
4	Tektronix 1 Meter Module Extenders

Calibration Kits

QTY	Description
1	GGB Industries, Picoprobe CS – 9 Calibration Substrate

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded.

Sample Preparation

Determine signal launch and monitoring test points by referencing the detailed pin-out maps provided in Appendix E. Pinout map names are;

TRL Microprobe Calibration Board, TRL
TDA Microprobe Calibration Board, **TDA**
PCB Fixture Sets **I**, **III**, **IV**

It is good practice to terminate all non-active signal lines immediately adjacent to the designated active or quiet signal lines under test.

Frequency Domain Procedures

TDA IConnect S-Parameter Extraction & Processing*

Frequency data extraction involves a two-step process. The first step creates the TDR based waveform relationships utilizing a Tektronix CSA8000 time based instrument. The second step involves the conversion of these time-based waveforms into s-parameter format using the TDA Systems IConnect software tool. TDA Systems labels time related conversion waveforms as the *Step* and *DUT* waveform references. This section establishes the setup procedures for defining the *Step* and *DUT* reference for conversion to frequency s-parameters presented in this report.

***Note:** A partial compliment of TDA IConnect S-parameter data is available. Data was generated for comparison to data generated using TRL calibration methods.

Series: QMSS/QFSS
Description: Shielded Q2 Socket/Terminal Strip, GSSSSG Standard Shield Configuration, 0.635mm (.025") Pitch, 11mm (.433") Stack Height

CSA8000 Setup

Listed below is the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. Functional settings such as window length, number of points and averaging capability determines the instruments frequency boundaries. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process. The single channel pulsed source processes s-parameters in single-ended format. A dual channel differential pulsed source processes s-parameters in differential format.

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss (TDA conversion)

STEP Waveform - determine TD waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Complete the transmission path by inserting a negligible length of transmission standard between the system test probes. Calibration or waveform referencing utilizes a six pad cal structure for each of the probe touchdowns (ie; se thru = 3 pads or diff thru = 6 pads). Reference the calibration board **TDA**, and use the 1mm (0.390") length calibration reflect/transmission structure for TDA step waveform characterization.

DUT Waveform - determine TD waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the TDA reflection/transmission standard and record the measurement. Reference PCB fixture set **I** & **III** for Insertion Loss configurations.

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Return Loss (TDA conversion)
STEP Waveform – determine TD waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. Calibration or waveform referencing utilizes three pads for each probe touchdown (ie; se reflect = 3 pads or diff reflect = 6 pads). Reference **TDA** calibration board and use the 1mm (0.390") length calibration reflect/transmission standard for TDA step waveform characterization.
DUT Waveform – determine waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the reflection standard. In this condition cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. Reference PCB fixture set **I** & **III** for Return Loss configurations.
Near-End Crosstalk (TDA conversion)
STEP Waveform – Use Return Loss (RL) step waveform.
DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent near-end signal line. Reference PCB fixture set **I**, **III**, & **IV** for NEXT configurations.

Far-End Crosstalk (TDA conversion)
STEP Waveform - Use Insertion Loss (IL) step waveform.
DUT Waveform - determine waveform by driving specified signal type and monitoring coupled energy levels at the configurations adjacent far-end signal line. Reference PCB fixture set **I**, **III**, & **IV** for FEXT configurations.

PNA S-Parameters /TRL Calibration
Valid S-Parameter measurements require a frequency driven source utilizing TRL calibration capabilities. These requirements are met using model N5230A PNA as the source instrument and **TRL** based on-board PCB standards.

N5230A PNA Setup
Frequency Sweep: Linear, 300 KHz to 20 GHz, Date Points: 1601, RBW: 1KHz, Cal Type: (TRL/μprobe) Full 4-port: Defined Calibration Kit ID: 41 – Dual Microprobe, Location: Calibration/Advanced Modify Cal Kit/ ID: 41, TRL Calibration Standards: PCB101793-**TST-98**.

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TRL Calibration Procedures

1. Perform SOLT calibration at the end of test port cables (E-cal or Mech. Cal)
2. Enable PNA S21 Phase format
3. Connect port 1 to one end of the Thru Standard and port 2 to the opposite end
4. Connect port 3 to one end of the Line 1 Standard and port 4 to the opposite end
5. Save Thru Standard phase response to memory
6. Perform DATA *(line 1)* divided by MEMORY *(thru standard)*
7. Verify low & high end frequency at 30° and 150°
8. Enable PNA S21 Smith Chart format
9. Scroll electrical delay function until response is parallel with the horizontal X-axis
10. Record difference in delay of line 1 to Thru Standard delay
11. Repeat steps 4 through 10 for line 2, then line 3, recording the difference in delay for each.
12. Define PCB101793-TST TRL standards definitions in a PNA calibration kit
13. Perform 20 step calibration procedure utilizing the PNA Calibration Wizard
14. Record/Save Calibration Kit Filename: **PCB101793-4P_TRL-CAL-STD_ON-BOARD_probes terminated**

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Time Domain Procedures

Utilize the Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) method for digital type pulse measurements. Impedance and propagation delay characterization utilize TDR measurement methods. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to characterize the SUT.

Impedance(TDR)

Energize the SUT's signal line(s) with a TDR pulse. The far-end of the energized signal lines are terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω termination) or use quality cables and adapters located at the far-end of the inserted SUT function as the systems 50Ω single-ended and/or 100Ω differential matching impedance. Reference PCB fixture sets **I** & **III** for Impedance configurations.

Propagation Delay (TDT)

This test reports differential or single ended signal delay as the measured difference of propagation between a combined electrical length of the input/output signal pads and traces (35 ± 5 ps edge rate) and the device under test (DUT) plus a referenced electrical length of the signal pads and signal traces ($PD^{pads/traces}$- $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$). The recorded delay is the signal delay of the connector only. $PD^{pads/traces}$ is the nomenclature representing the electrical length of PCB signal pads & traces equal to physical lengths of PCB pads & traces entering and leaving the device under test (DUT). The PD^{DUT} + $PD^{pads/traces}$ variable is the mated DUT fixture. Measure the risetime of $PD^{pads/traces}$ waveform & $\mathbf{PD^{DUT}}$ + $PD^{pads/traces}$ waveforms. Record the 50% amplitude of each rising edge. The distance in time between the rising edges is the propagation delay of the device under test (DUT). Reference calibration board **TDA** for signal trace lengths. Reference PCB fixture sets **I** & **III** for Propagation Delay configurations.

Near-End Crosstalk (TDT)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the near-end for magnitudes of coupled energy. Terminate adjacent signal lines not under test in the test systems characteristic impedance. Reference PCB fixture sets **I**, **III**, & **IV** for crosstalk configurations.

Far-End Crosstalk (TDT)

Energize the pre-determined signal line(s) with the appropriate signal type. Monitor the configurations adjacent quiet signal line at the far-end for magnitudes of coupled energy. Terminate adjacent signal lines not under test into the test systems characteristic impedance. Reference PCB fixture sets **I**, **III**, & **IV** for crosstalk configurations.

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Appendix F – Glossary of Terms

ADS – Advanced Design Systems
BC – Best Case crosstalk configuration
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
EC6 – Edge Card with a .635mm signal pad pitch
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
HDV – High Density Vertical
EC8 – Signal Launch Edge Card with a 0.8 mm signal pad pitch
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
TRL – Through, Reflect & Line (3) Standards + Line Match
WC – Worst Case crosstalk configuration
Z – Impedance (expressed in ohms)