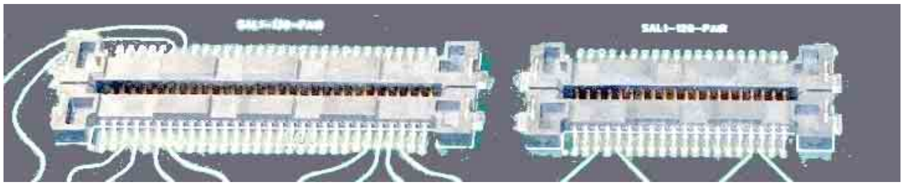
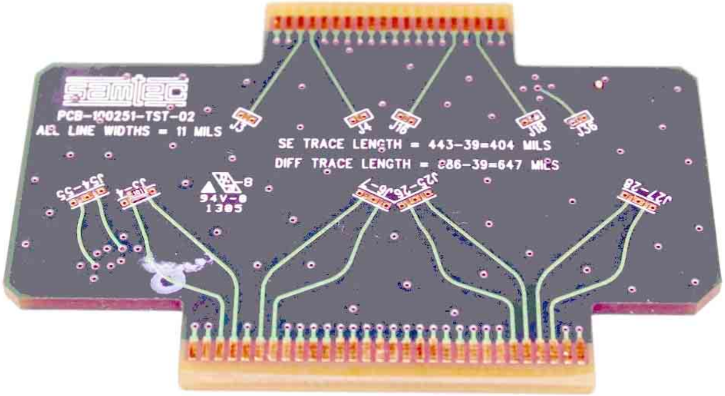
High Speed Characterization Report

SAL1-1xx-01-S-S-A (QTY=2)



Mated With



Edge Card Socket

Description:
Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

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Report Revision: 6/13/2005

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

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Connector Overview

SAL1 high speed micro plane 1.0mm (.0394”) pitch interfaces mount in pairs and provide a top or bottom edge card entry for easy signal routing. The interface accepts either 1.60mm (.062”) or 2,40mm (.093”) thickness edge cards. The edge card can be mated with the SAL1 either from the top or the bottom. The data in this report is applicable only to top entry mount utilizing a 1.60mm (.062”) thick edge card.

Connector System Speed Rating

1.60mm (.062”) Edge Card to Micro Plane Interface,1.0mm Pitch, Top Entry, Right Angle

Signaling	Speed Rating
Single-Ended:	**8.5 GHz / 17 Gbps**
Differential:	**9.0 GHz / 18 Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board’s trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/ 15 Gbps.

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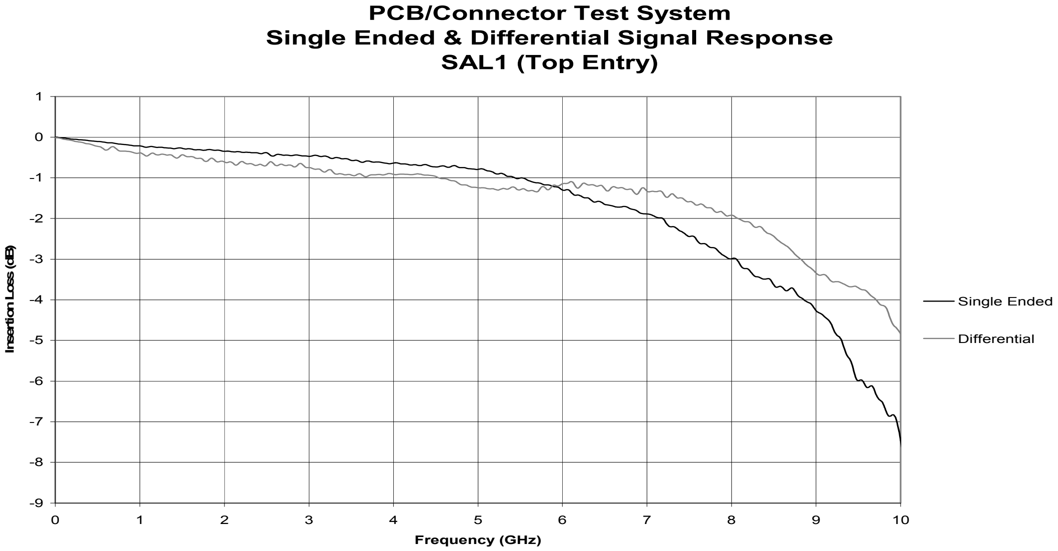
Frequency Domain Data Summary

Table 1 - Single-Ended Connector System Performance

Test Parameter	Configuration	
Insertion Loss	GSG	**-3dB @ 8.06GHz**
Return Loss	GSG	≤ -5 dB to 8.06GHz
Near-End Crosstalk	GAQG	≤ -5dB to 8.06GHz
	GAGQG	≤ -15dB to 8.06GHz
	Xrow, GAG to GQG	≤ -35dB to 8.06GHz
Far-End Crosstalk	GAQG	≤ -8dB to 8.06GHz
	GAGQG	≤ -15dB to 8.06GHz
	Xrow, GAG to GQG	≤ -32dB to 8.06GHz

Table 2 - Differential Connector System Bandwidth

Test Parameter	Configuration	
Insertion Loss	GSSG	**-3dB @ 8.82 GHz**
Return Loss	GSSG	≤ -5dB to 8.82 GHz
Near-End Crosstalk	GAAQQG	≤ -18dB to 8.82 GHz
	GAAGQQG	≤ -30dB to 8.82 GHz
	Xrow, GAAG to GQQG	≤ -40dB to 8.82 GHz
Far-End Crosstalk	GAAQQG	≤ -25dB to 8.82 GHz
	GAAGQQG	≤ -32dB to 8.82 GHz
	Xrow, GAAG to GQQG	≤ -40dB to 8.82 GHz



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Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω)

Signal Risetime	30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	63.4	54.7	51.7	51.4	51.2	51.0	50.9
Minimum Impedance	39.3	44.7	47.5	49.0	49.8	50.1	50.2

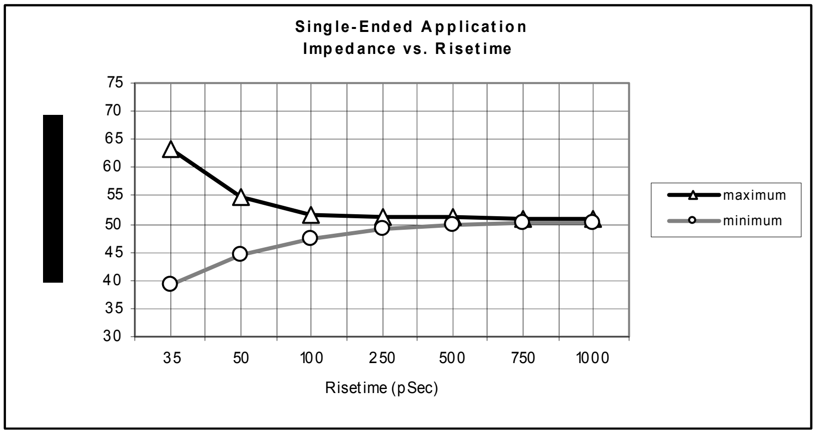

Table 4 - Differential Impedance (Ω)

Signal Risetime	30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	104.2	103.8	103.3	102.7	102.5	102.1	101.8
Minimum Impedance	71.4	81.8	86.9	91.9	95.6	97.3	98.2

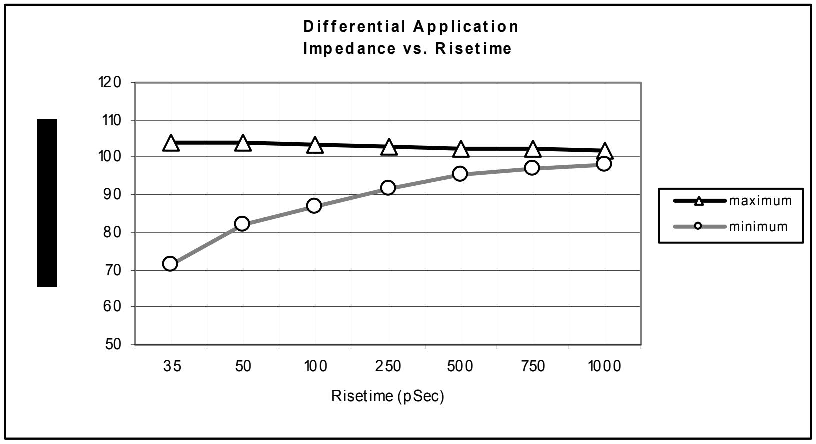

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Table 5 - Single-Ended Crosstalk (%)

Input (t_r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAQG	13.5	11.9	8.9	4.4	2.4	1.7	1.3
	GAGQG	3.6	3.2	2.4	1.1	< 1.0	< 1.0	< 1.0
	Xrow^{se}	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
FEXT	GAQG	7.2	5.6	3.5	1.5	< 1.0	< 1.0	< 1.0
	GAGQG	3.9	3.1	1.9	< 1.0	< 1.0	< 1.0	< 1.0
	Xrow^{se}	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0

Table 6 - Differential Crosstalk (%)

Input (t_r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAAQQG	3.3	2.8	2.1	1.2	< 1.0	< 1.0	< 1.0
	GAAGQQG	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
	Xrow^{diff}	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
FEXT	GAAQQG	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
	GAAGQQG	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
	Xrow^{diff}	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0

Table 7 - Propagation Delay (Mated Connector)

Single-Ended	62.0 ps
Differential	52.0 ps

Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from the test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

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For this connector, the following configurations were evaluated:

Single-Ended Impedance**:**

- GSG (ground-signal-ground)

Single-Ended Crosstalk**:**

- Electrical “worst case”: GAQG (ground-active-quiet-ground)
- Electrical “best case”: GAGQG (ground-active-ground-quiet-ground)
- Across row: Xrow^{se} (from one row of terminals to the other row across the edge card ground plane)

Differential Impedance**:**

- GSSG (Ground-positive signal-negative signal-ground)

Differential Crosstalk**:**

- Electrical “worst case”: GAAQQG (ground-active-active-quiet-quiet-ground)
- Electrical “best case”: GAAGQQG (ground-active-active-ground-quiet-quiet-ground)
- Across row:Xrow^{diff} (from one row of terminals to the other row across the edge card ground plane)

In all cases in this report, contacts assigned ground designations are continuous throughout the system under test. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals, might be encountered, as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of an interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, rise times were measured at 10%-90% signal levels.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT's frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 30 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 30 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

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Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

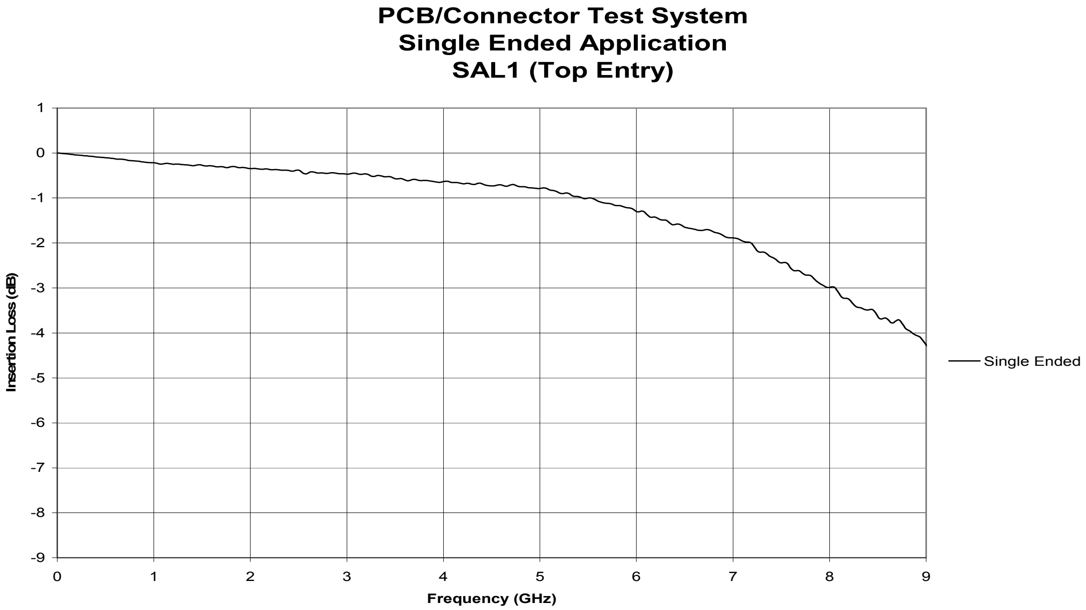
Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

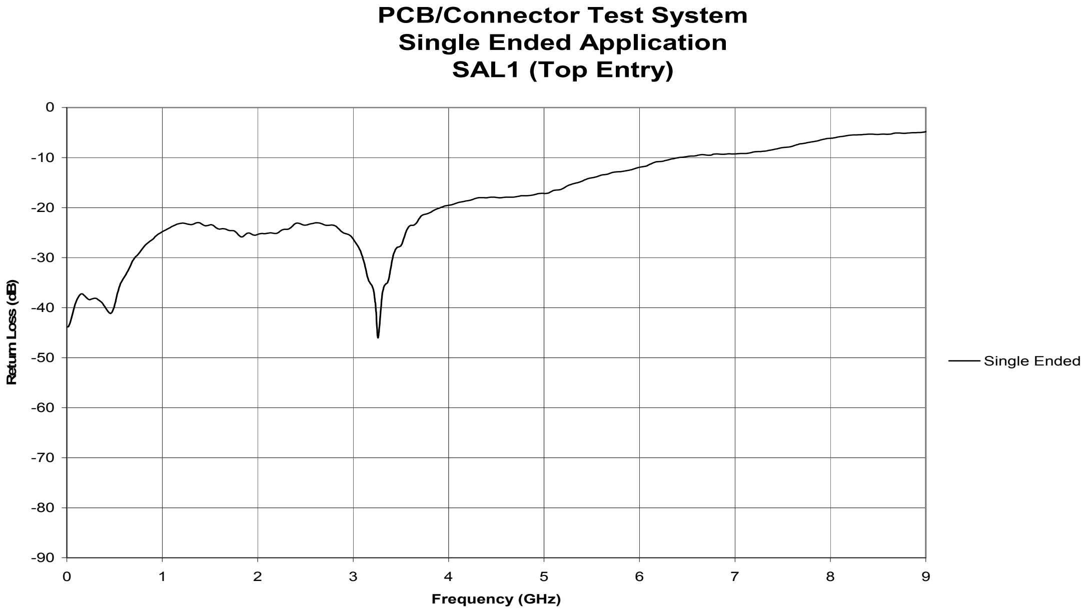
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss

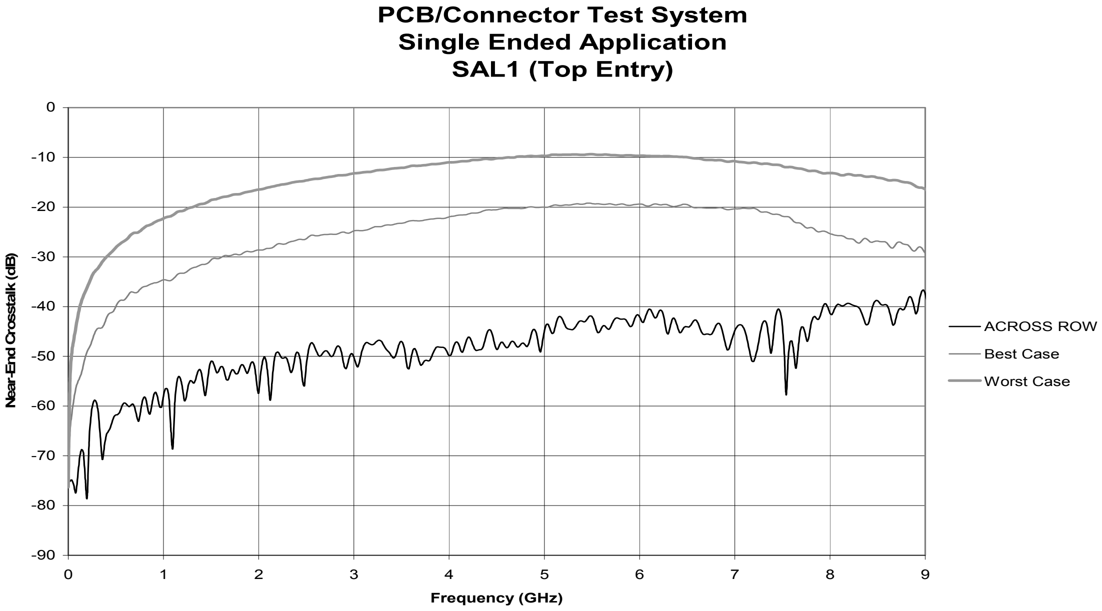


Single-Ended Application – Return Loss

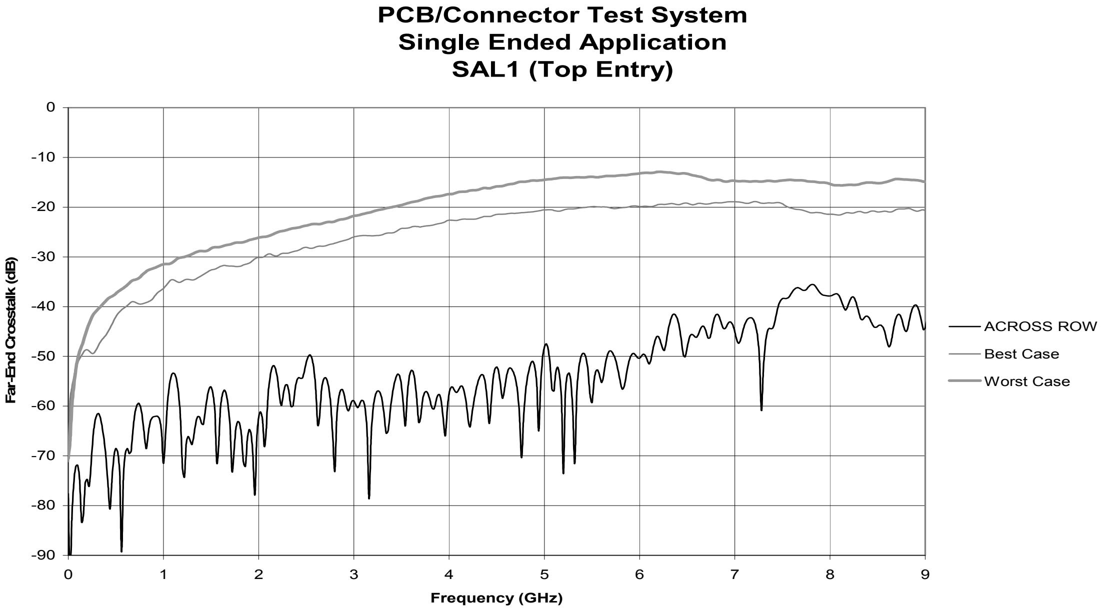


Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Single-Ended Application – NEXT

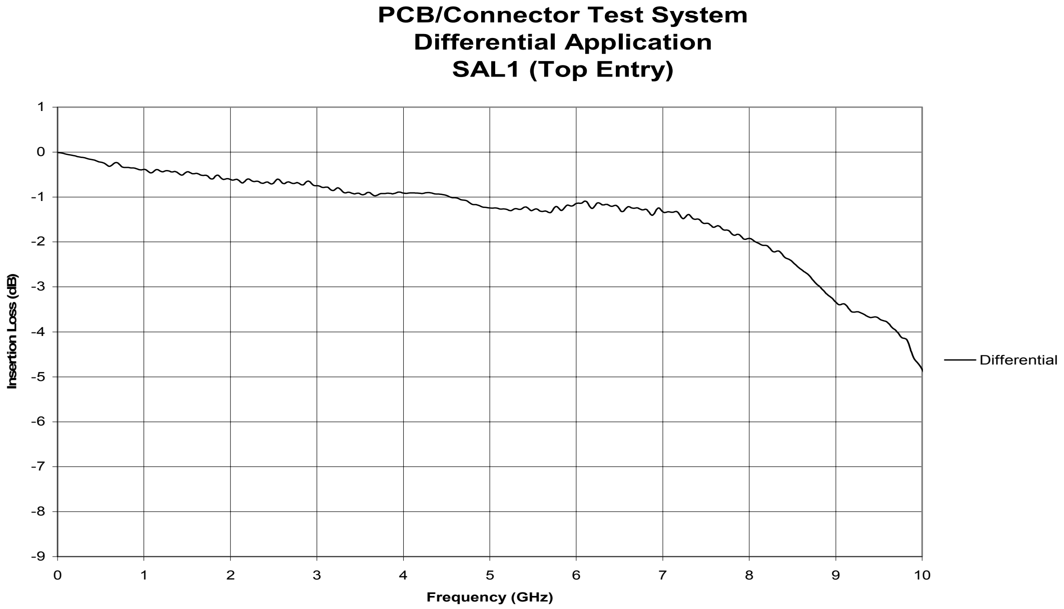


Single-Ended Application – FEXT

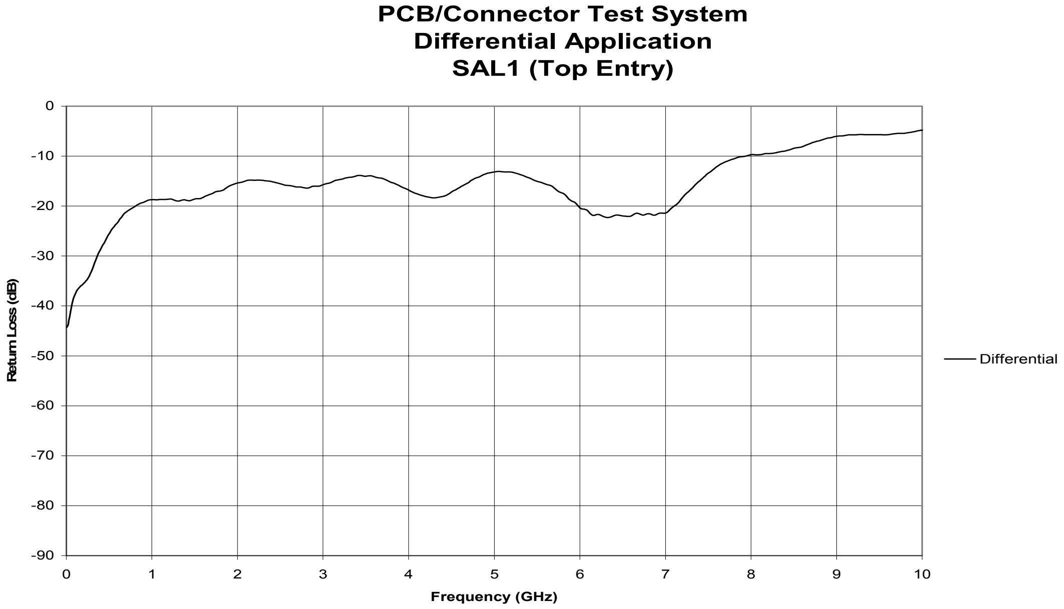


Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Differential Application – Insertion Loss

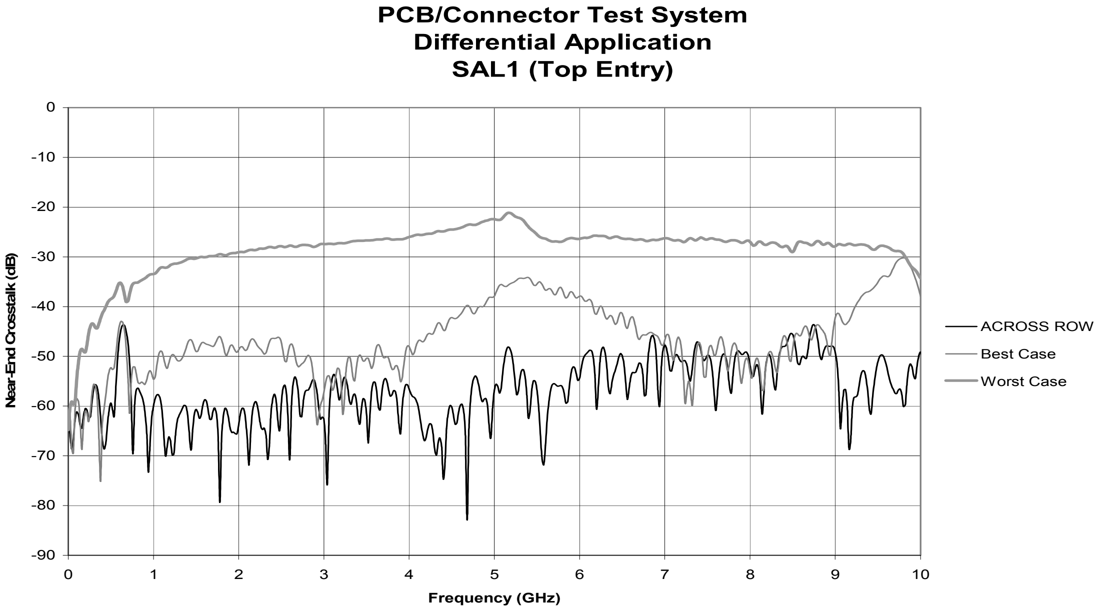


Differential Application – Return Loss

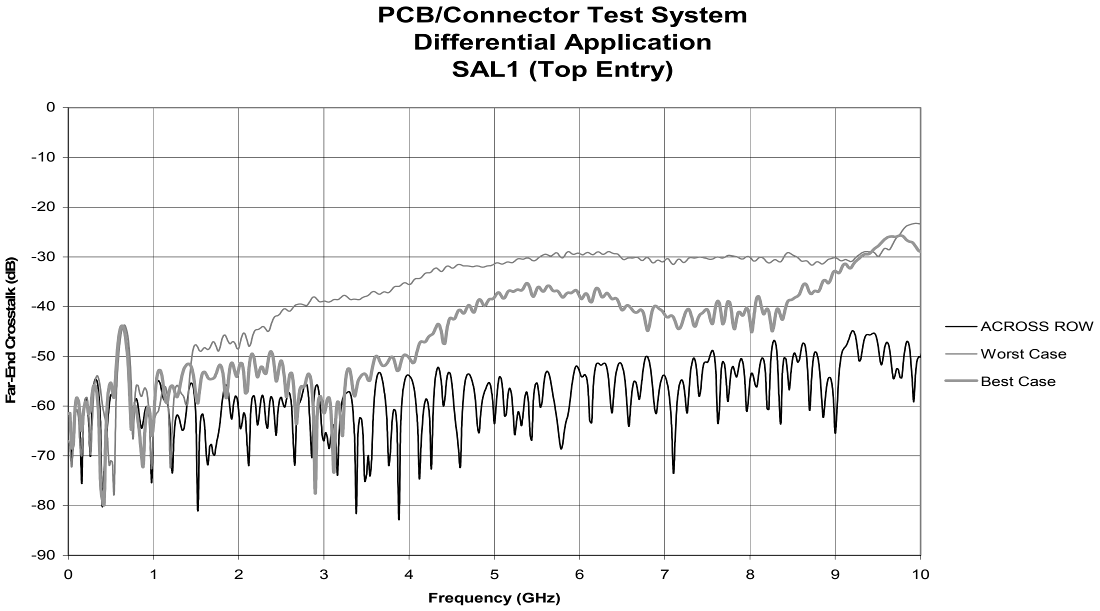


Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Differential Application – NEXT

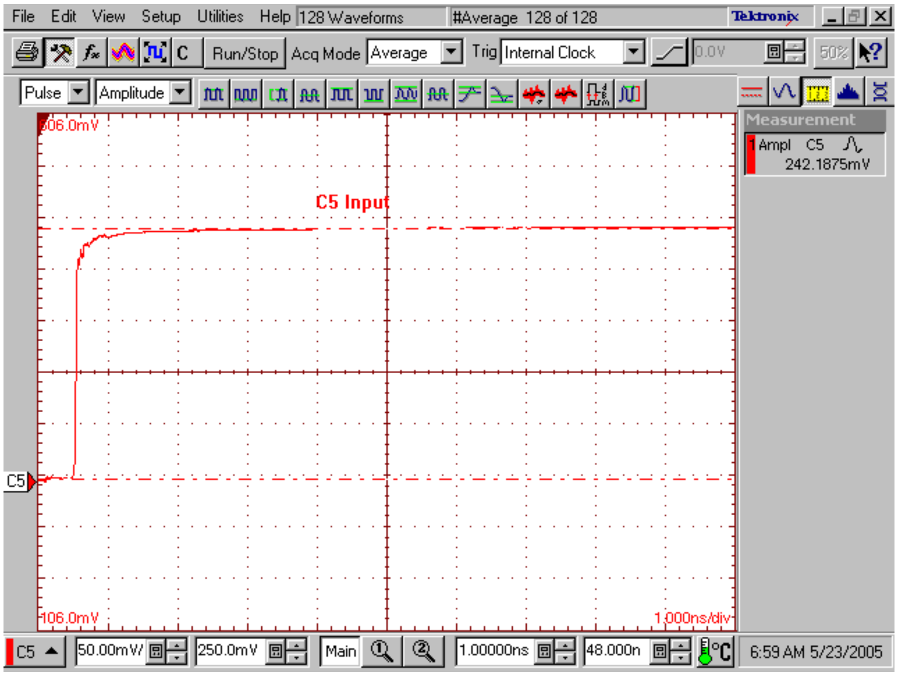


Differential Application – FEXT



Appendix B – Time Domain Response Graphs

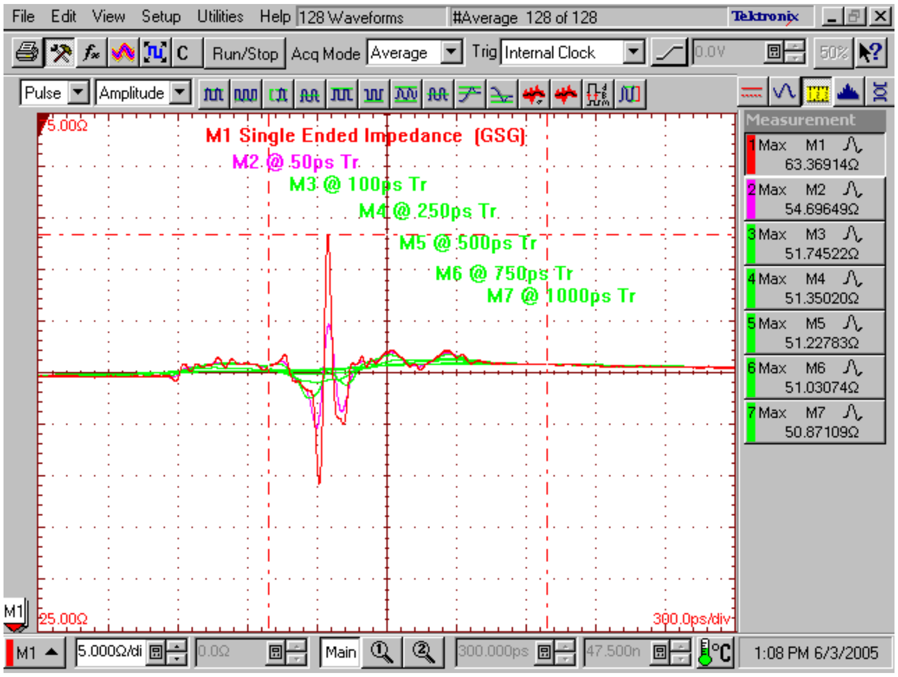
Single-Ended Application – Input Pulse



Ampl C5 242.1875mV

C5 50.00mV/ 250.0mV 1.00000ns 48.000n

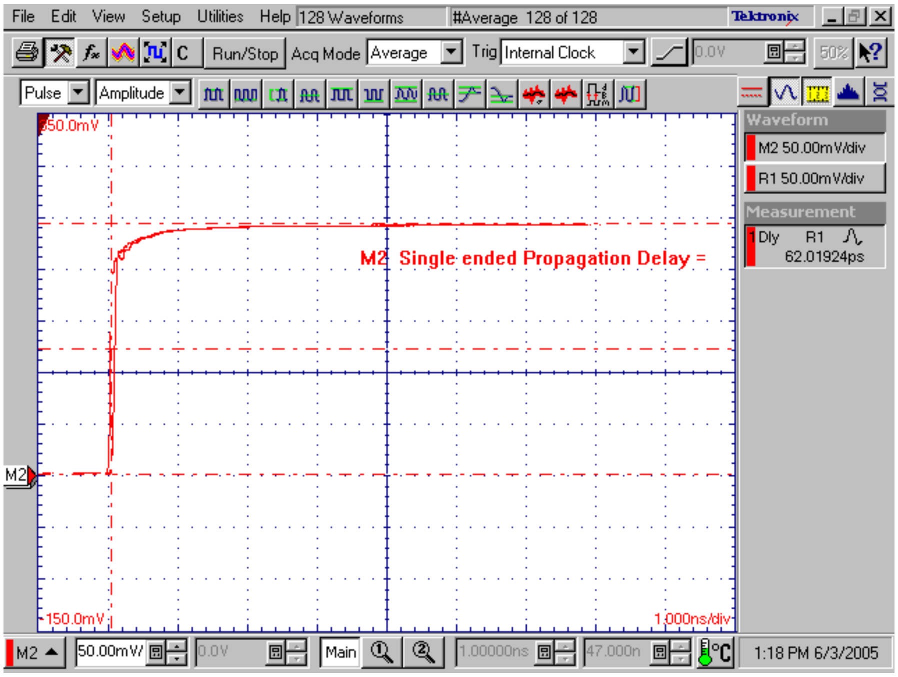
Single-Ended Application – Impedance



M1 Single Ended Impedance (GSG)
M2 @ 50ps Tr
M3 @ 100ps Tr
M4 @ 250ps Tr
M5 @ 500ps Tr
M6 @ 750ps Tr
M7 @ 1000ps Tr

Measurement
1 Max M1 63.36914Ω
2 Max M2 54.69649Ω
3 Max M3 51.74522Ω
4 Max M4 51.35020Ω
5 Max M5 51.22783Ω
6 Max M6 51.03074Ω
7 Max M7 50.87109Ω

Single-Ended Application – Propagation Delay



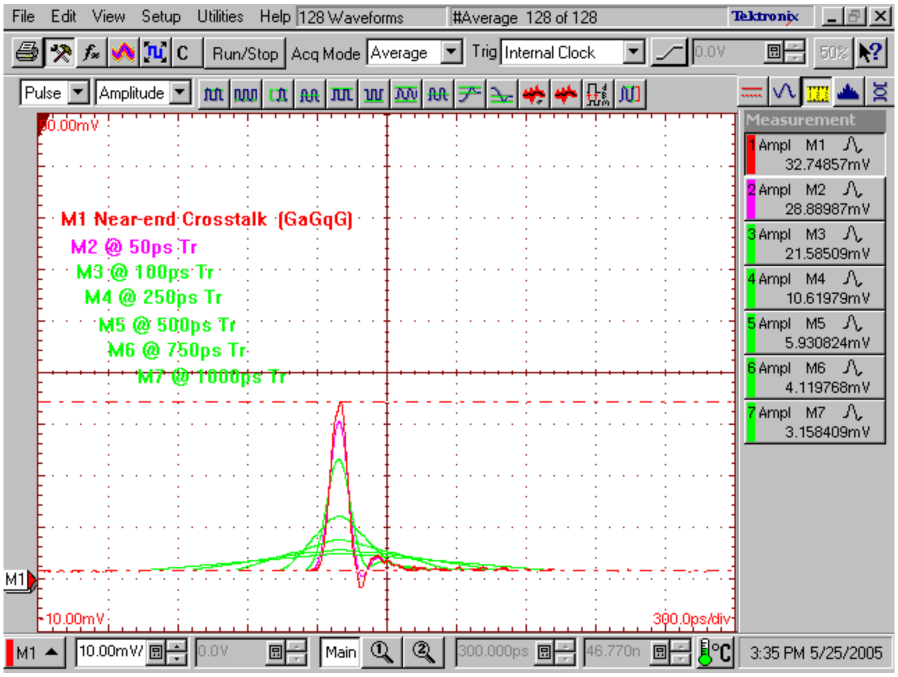
M2 Single ended Propagation Delay =

Waveform
M2 50.00mV/div
R1 50.00mV/div

Measurement
1 Dly R1 62.01924ps

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Single-Ended Application – NEXT, "Worst Case" Configuration

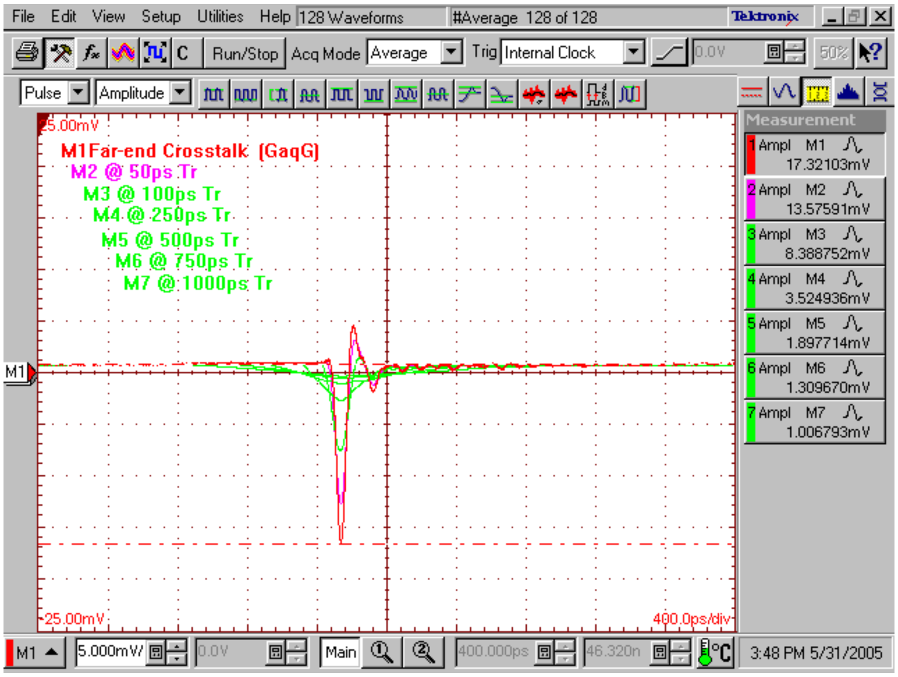


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V
50%

Measurement
1 Ampl M1 32.74857mV
2 Ampl M2 28.88987mV
3 Ampl M3 21.58509mV
4 Ampl M4 10.61979mV
5 Ampl M5 5.930824mV
6 Ampl M6 4.119768mV
7 Ampl M7 3.158409mV

M1 10.00mV/ 0.0V
300.000ps 46.770n
3:35 PM 5/25/2005

Single-Ended Application – FEXT, "Worst Case" Configuration



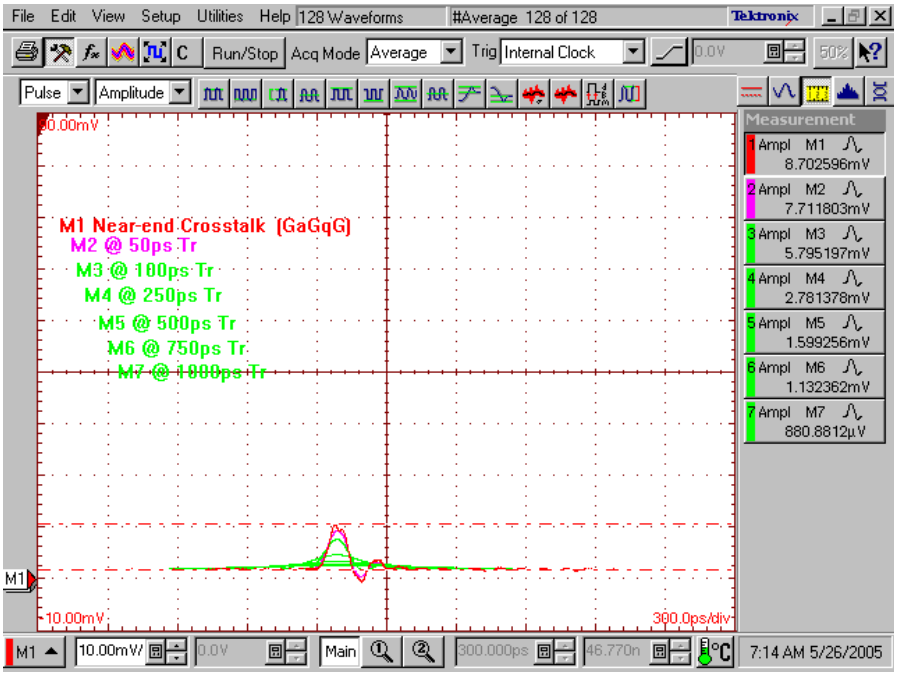
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V
50%

Measurement
1 Ampl M1 17.32103mV
2 Ampl M2 13.57591mV
3 Ampl M3 8.388752mV
4 Ampl M4 3.524936mV
5 Ampl M5 1.897714mV
6 Ampl M6 1.309670mV
7 Ampl M7 1.006793mV

M1 5.000mV/ 0.0V
400.000ps 46.320n
3:48 PM 5/31/2005

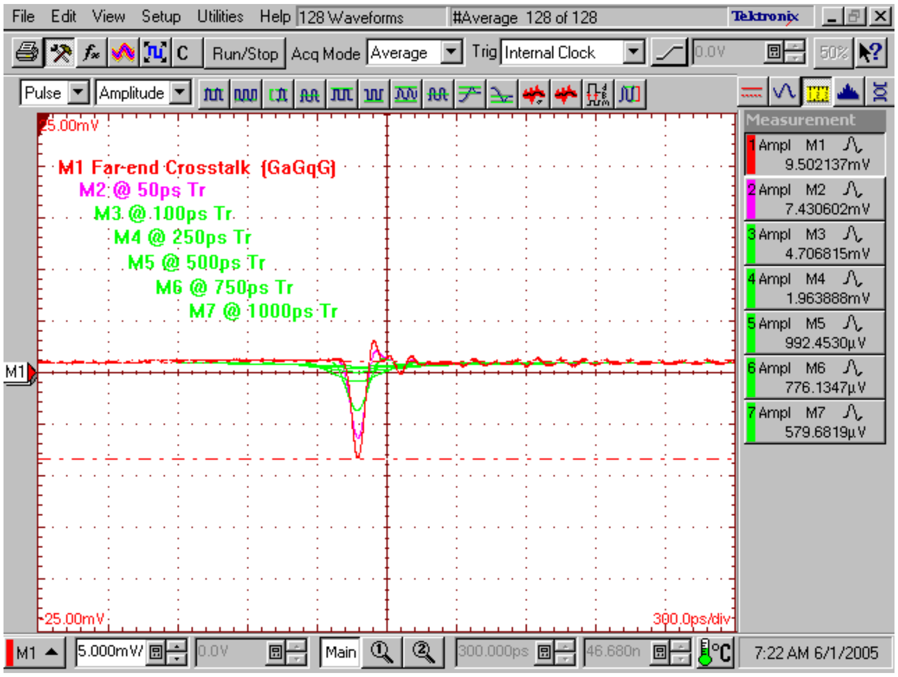
Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Single-Ended Application – NEXT, "Best Case" Configuration



128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
1 Ampl M1 8.702596mV
2 Ampl M2 7.711803mV
3 Ampl M3 5.795197mV
4 Ampl M4 2.781378mV
5 Ampl M5 1.599256mV
6 Ampl M6 1.132362mV
7 Ampl M7 880.8812µV
M1 10.00mV/ 0.0V
300.000ps 46.770n
7:14 AM 5/26/2005

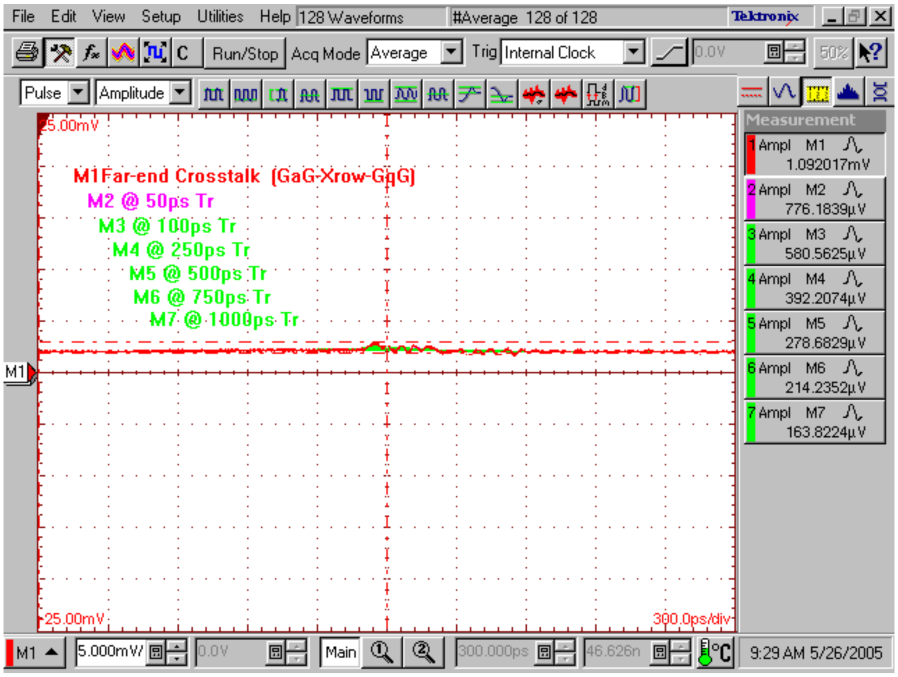
Single-Ended Application – FEXT, "Best Case" Configuration



128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
1 Ampl M1 9.502137mV
2 Ampl M2 7.430602mV
3 Ampl M3 4.706815mV
4 Ampl M4 1.963888mV
5 Ampl M5 992.4530µV
6 Ampl M6 776.1347µV
7 Ampl M7 579.6819µV
M1 5.000mV/ 0.0V
300.000ps 46.680n
7:22 AM 6/1/2005

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Single-Ended Application – NEXT, "Across Row" Configuration

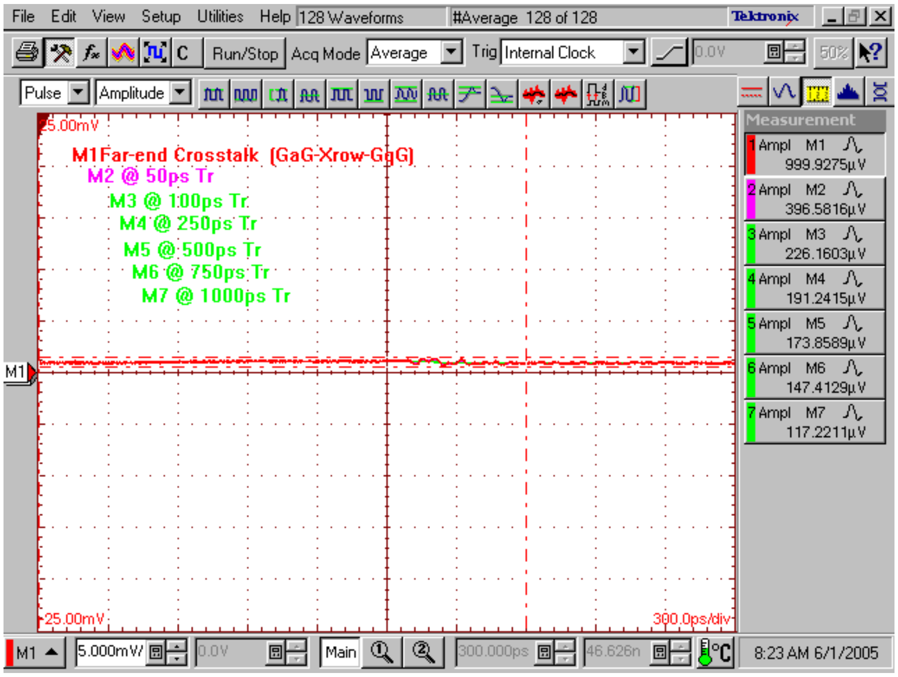


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock

1 Ampl M1 1.092017mV
2 Ampl M2 776.1839µV
3 Ampl M3 580.5625µV
4 Ampl M4 392.2074µV
5 Ampl M5 278.6829µV
6 Ampl M6 214.2352µV
7 Ampl M7 163.8224µV

M1 5.000mV/
9:29 AM 5/26/2005

Single-Ended Application – FEXT, "Across Row" Configuration



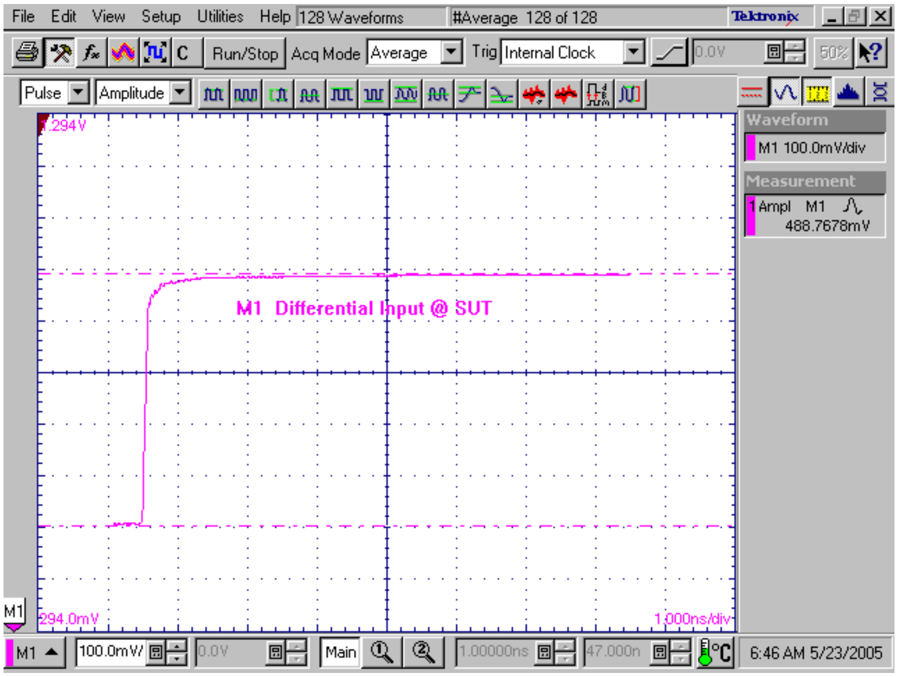
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock

1 Ampl M1 999.9275µV
2 Ampl M2 396.5816µV
3 Ampl M3 226.1603µV
4 Ampl M4 191.2415µV
5 Ampl M5 173.8589µV
6 Ampl M6 147.4129µV
7 Ampl M7 117.2211µV

M1 5.000mV/
8:23 AM 6/1/2005

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

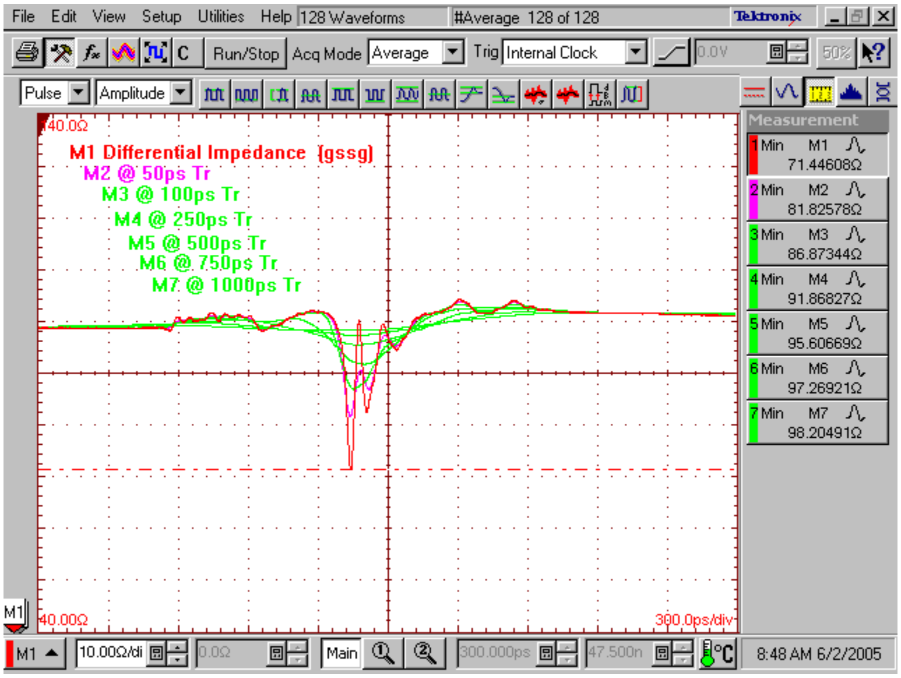
Differential Application – Input Pulse



128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V
50%
1.294V
M1 Differential Input @ SUT
294.0mV
1.000ns/div
M1 100.0mV/div
Ampl M1 488.7678mV
M1 100.0mV/
0.0V
1.00000ns
47.000n
6:46 AM 5/23/2005

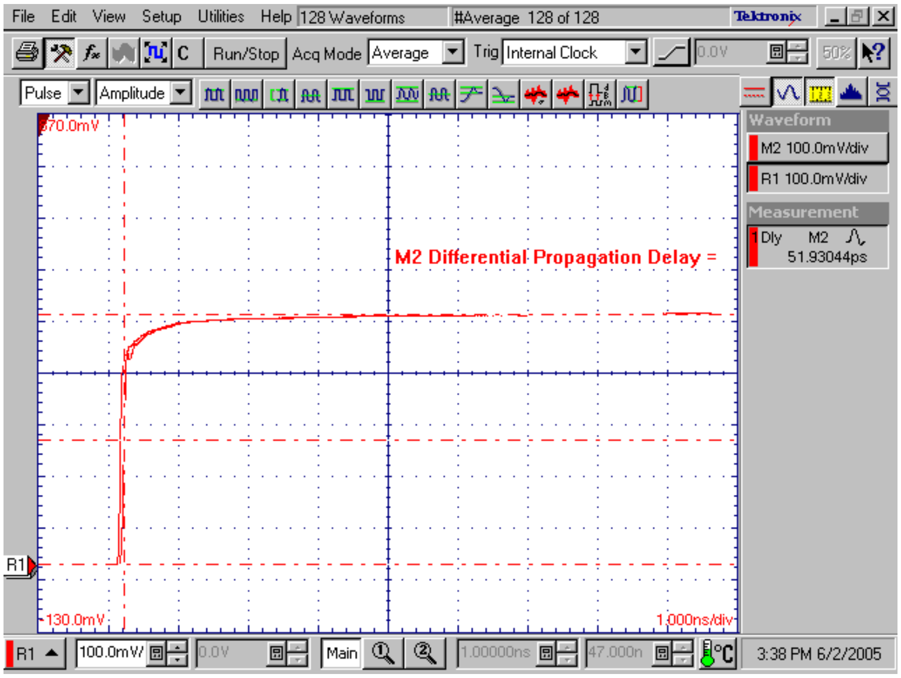
Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Differential Application – Impedance



Measurement
1 Min M1 71.44608Ω
2 Min M2 81.82578Ω
3 Min M3 86.87344Ω
4 Min M4 91.86827Ω
5 Min M5 95.60669Ω
6 Min M6 97.26921Ω
7 Min M7 98.20491Ω

Differential Application – Propagation Delay



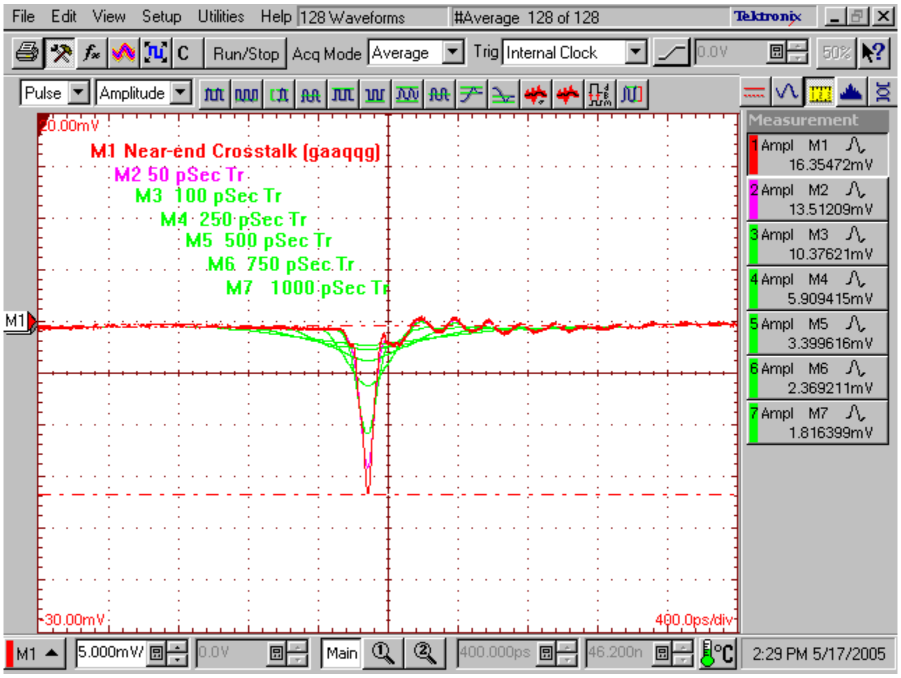
M2 Differential Propagation Delay =

Waveform
M2 100.0mV/div
R1 100.0mV/div

Measurement
1 Dly M2 51.93044ps

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Differential Application – NEXT, "Worst Case" Configuration

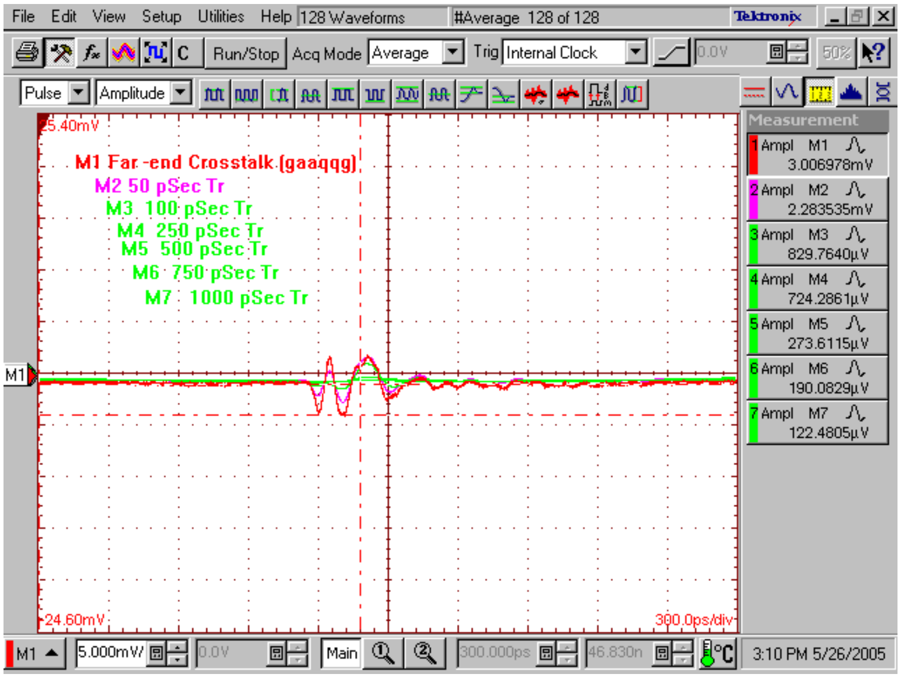


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V
50%

1 Ampl M1 16.35472mV
2 Ampl M2 13.51209mV
3 Ampl M3 10.37621mV
4 Ampl M4 5.909415mV
5 Ampl M5 3.399616mV
6 Ampl M6 2.369211mV
7 Ampl M7 1.816399mV

M1 5.000mV/ 0.0V
400.000ps 46.200n
2:29 PM 5/17/2005

Differential Application – FEXT, "Worst Case" Configuration

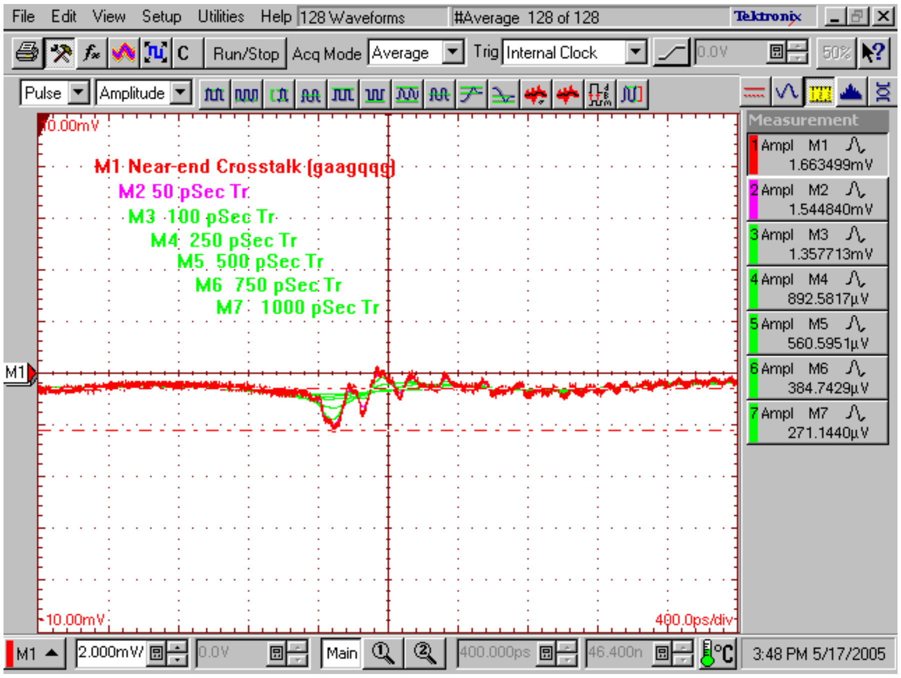


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V
50%

1 Ampl M1 3.006978mV
2 Ampl M2 2.283535mV
3 Ampl M3 829.7640µV
4 Ampl M4 724.2861µV
5 Ampl M5 273.6115µV
6 Ampl M6 190.0829µV
7 Ampl M7 122.4805µV

M1 5.000mV/ 0.0V
300.000ps 46.830n
3:10 PM 5/26/2005

Differential Application – NEXT, "Best Case" Configuration

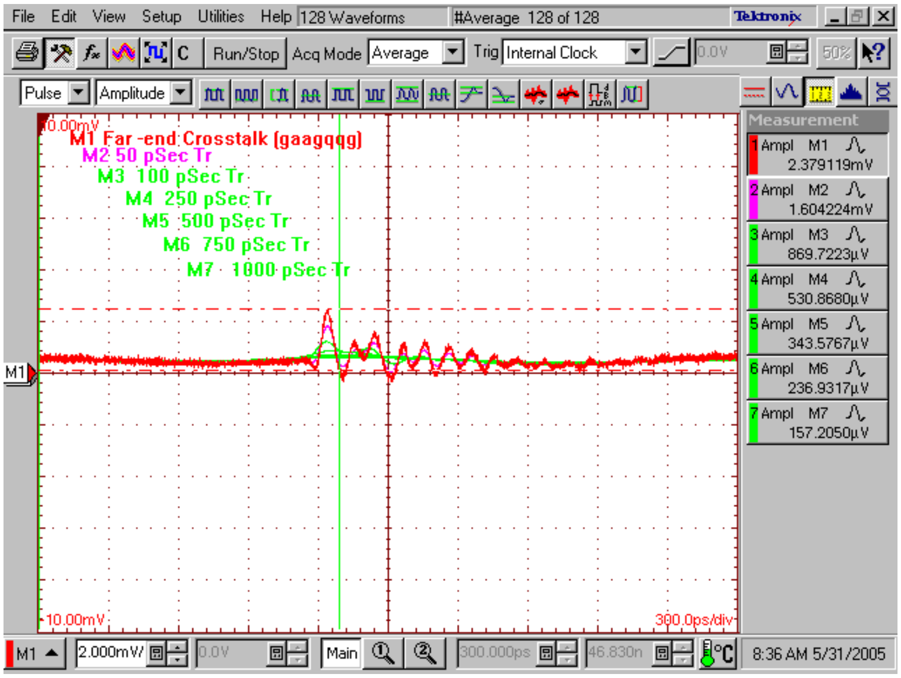


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock

1 Ampl	M1	1.663499mV
2 Ampl	M2	1.544840mV
3 Ampl	M3	1.357713mV
4 Ampl	M4	892.5817µV
5 Ampl	M5	560.5951µV
6 Ampl	M6	384.7429µV
7 Ampl	M7	271.1440µV

M1 2.000mV/ 0.0V Main 400.000ps 46.400n 3:48 PM 5/17/2005

Differential Application – FEXT, "Best Case" Configuration



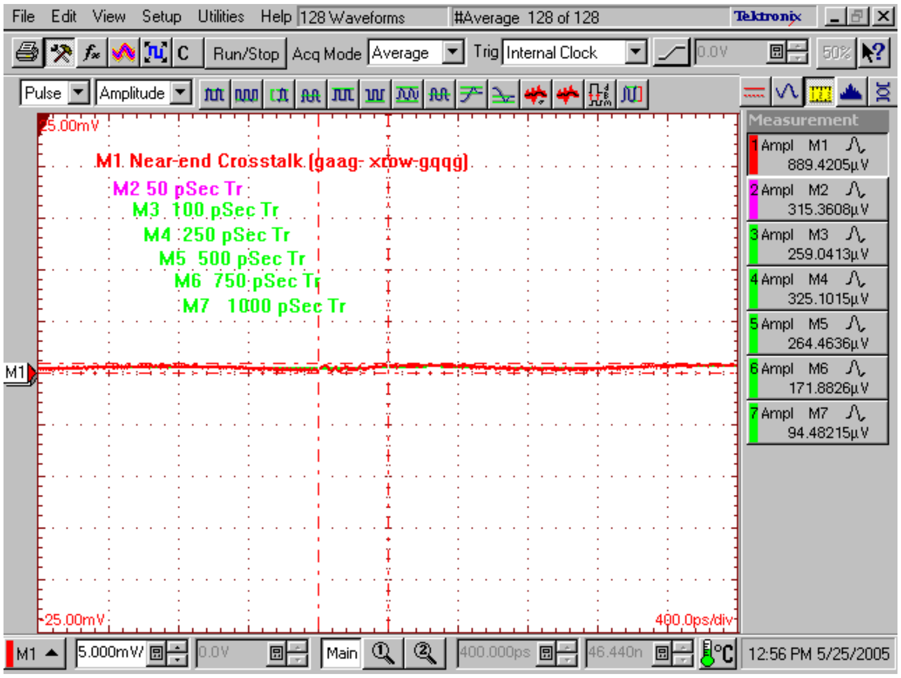
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock

1 Ampl	M1	2.379119mV
2 Ampl	M2	1.604224mV
3 Ampl	M3	869.7223µV
4 Ampl	M4	530.8680µV
5 Ampl	M5	343.5767µV
6 Ampl	M6	236.9317µV
7 Ampl	M7	157.2050µV

M1 2.000mV/ 0.0V Main 300.000ps 46.830n 8:36 AM 5/31/2005

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

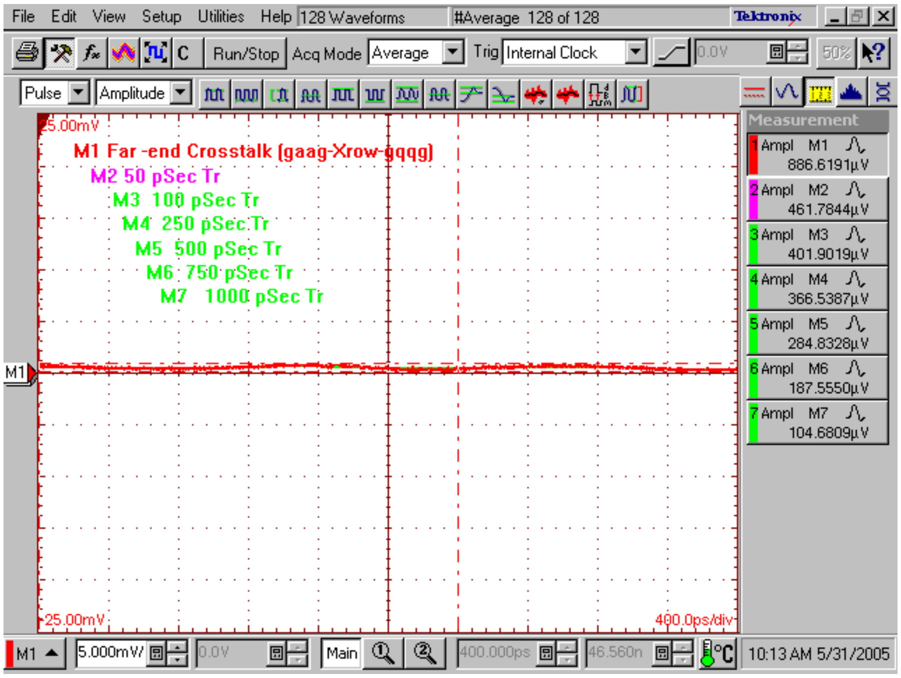
Differential Application – NEXT, “Across Row” Configuration



M1 Near-end Crosstalk (gaag- xrow-gqqg)
M2 50 pSec Tr
M3 100 pSec Tr
M4 250 pSec Tr
M5 500 pSec Tr
M6 750 pSec Tr
M7 1000 pSec Tr

#Average 128 of 128
Acq Mode Average
Trig Internal Clock
Amplitude
1 Ampl M1 889.4205µV
2 Ampl M2 315.3608µV
3 Ampl M3 259.0413µV
4 Ampl M4 325.1015µV
5 Ampl M5 264.4636µV
6 Ampl M6 171.8826µV
7 Ampl M7 94.48215µV
5.000mV/
12:56 PM 5/25/2005

Differential Application – FEXT, “Across Row” Configuration



M1 Far -end Crosstalk (gaag-Xrow-gqqg)
M2 50 pSec Tr
M3 100 pSec Tr
M4 250 pSec Tr
M5 500 pSec Tr
M6 750 pSec Tr
M7 1000 pSec Tr

#Average 128 of 128
Acq Mode Average
Trig Internal Clock
Amplitude
1 Ampl M1 886.6191µV
2 Ampl M2 461.7844µV
3 Ampl M3 401.9019µV
4 Ampl M4 366.5387µV
5 Ampl M5 284.8328µV
6 Ampl M6 187.5550µV
7 Ampl M7 104.6809µV
5.000mV/
10:13 AM 5/31/2005

Appendix C – Product and Test System Descriptions

Product Description

Product samples were the SAL1 high speed micro plane interface and a dual signal PCB100251-02 edge card. Connector interface part numbers utilized were the SAL1-130-01-S-S-A and SAL1-120-01-S-S-A.

The connector structure consists of a row of either 20 or 30 contacts and is mounted in pairs. Mounting orientation can be either edge card top entry or edge card bottom entry. The data presented in this report is specific to top entry and utilizes a 1.60mm (.062”) thick impedance optimized dual signal type edge card (Figure 1).

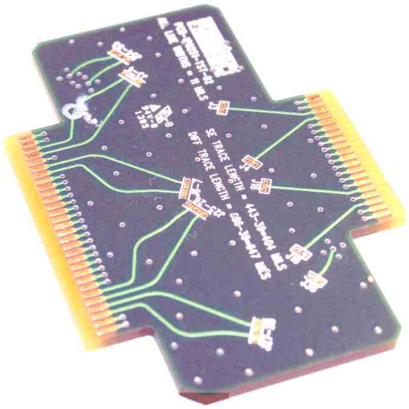


Figure 1 Dual Signal Type Edge Card

Test System Description

The test fixture (Figure 2) depicts the edge card top entry and edge card bottom entry connector orientations. This report is concerned with edge card top entry and SI results are obtained from the two connectors pictured on the left. The left most connector (SAL1-130) provides differential signal integrity results while the adjacent connector (SAL1-120) is for testing single ended characteristics.

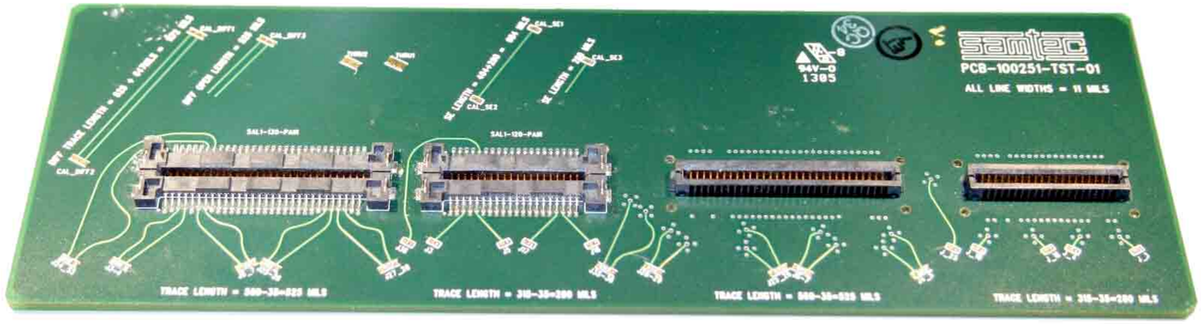


Figure 2 SAL1 Series Fixture, (a) two left connectors = top entry (b) two right connectors = bottom entry

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Single-Ended Top Entry Test Fixture
Edge card top entry (Figure 3) is on the same side as the connector surface mount terminals (SMT). Signal traces can be observed running directly to the edge card contact and SAL1 SMT. Test points J16, J18, and J36 are edge card signal paths provided for monitoring the transmission, reflection, and GAQG best case and across row configuration crosstalk characteristics. Test Points J3 and J4 are signal paths for characterizing worse case crosstalk only.

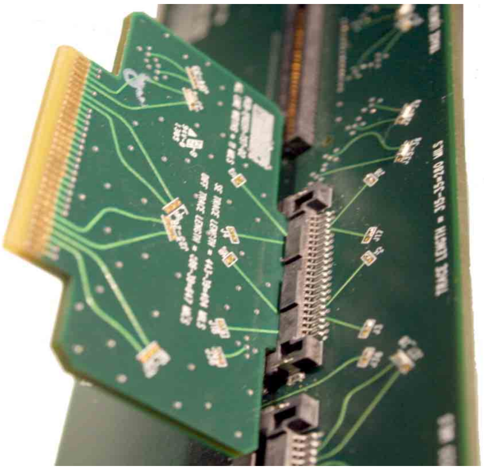


Figure 3 Single Ended Top Entry

Differential Top Entry Fixture
Edge card top entry (Figure 4) is on the same side as the connector surface mount terminals (SMT). Paired signal traces can be observed running directly to the edge card contact and SAL1 SMT. Test points J6-7, J3-4, and J54-55 are edge card signal paths provided for monitoring the transmission, reflection, and GAAGQQG best case and across row configuration crosstalk characteristics. Test Points J27-28 and J25-26 are signal paths for characterizing worse case crosstalk only.

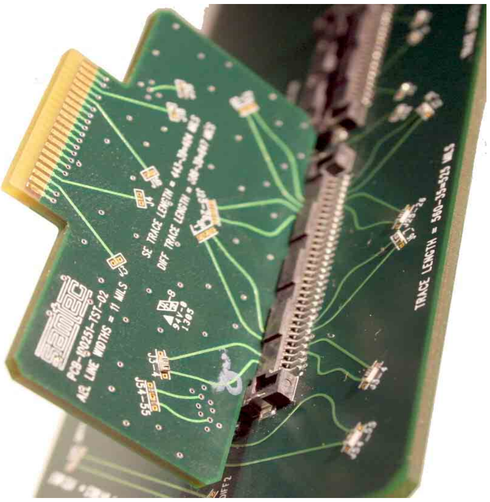


Figure 4 Differential Top Entry

Test point junction identifiers do not necessarily correspond from the edge card to the SAL1 PCB connector fixture. However, when the edge card is inserted, all signal paths will have a corresponding through path to the PCB connector fixture. Signals can be launched or received from either the socket (edge card) or header (PCB connector) side of the test fixture. All data and waveforms presented in the report are results from a socket side signal launch.

Appendix D – Test and Measurement Setup

Test instruments are a Tektronix CSA8000 Communication Signal Analyzer Mainframe and the Agilent 8720ES Vector Network Analyzer. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. For this series of tests, four of the eight TDR/Sampling Head capability is used *(Figure 5)*. The 8720ES serves as a supporting test instrument for verification or troubleshooting results obtained from the TDA Systems IConnect Software package. IConnect is a TDR based measurement software tool used in generating frequency domain related responses from high speed interconnects.

The probe stations illuminated video microscopy system, microprobe positioners, and 40GHz capable probes provide both the mechanical properties and electrical characteristics for obtaining the precise signal launch and calibrations that are critical in obtaining accurate high speed measurements. The 450 micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a < 18 dB return loss, and an isolation of 38 dB to 40 GHz. Test cables and interconnect adapters are high quality and insure high-bandwidth and low parasitic measurements. *(Figure 6)*

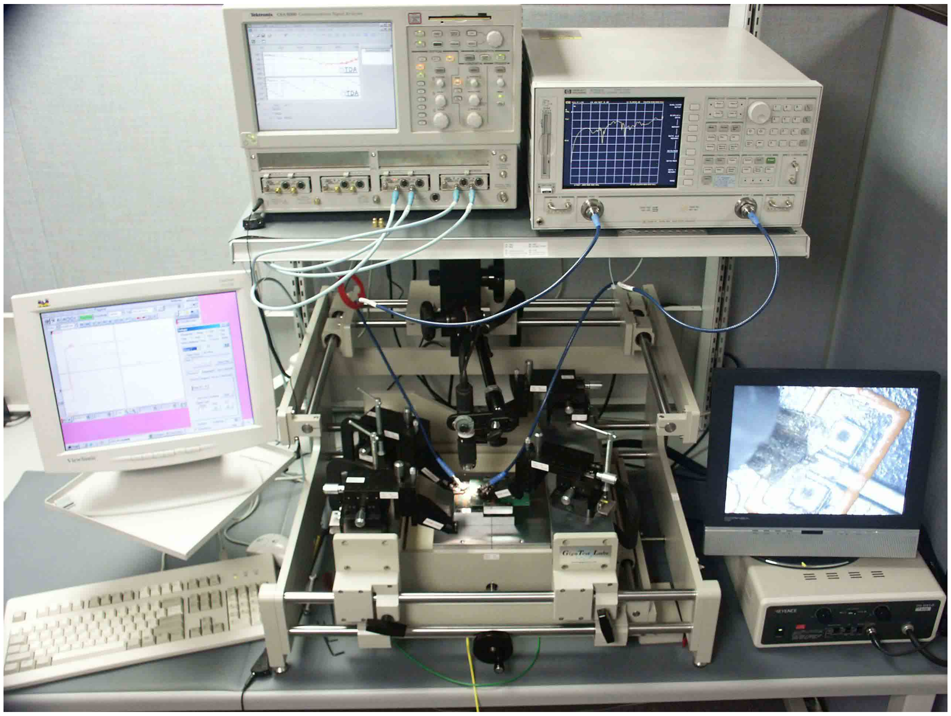


Figure 5 – Probe Station Measurements Capability

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Test Instruments

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
3	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Tektronix 80E03 Dual Channel 20 GHz Sampling Module

Measurement Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
2	Picoprobe by GGB Ind. Model 40A GSG (single ended applications)
2	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X

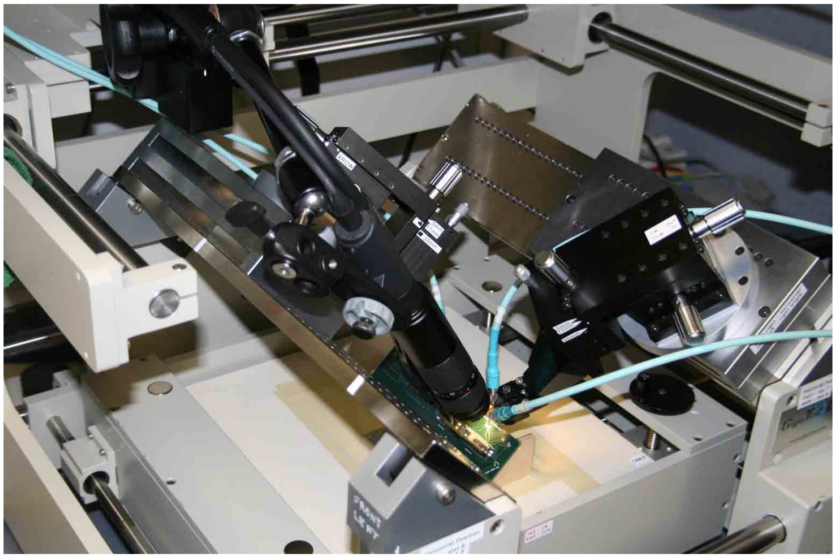


Figure 5 Right Angle Test Setup

Test Cables & Adapters

QTY	Description
4	Micro-Coax Cable Assembly 48” 3.5mm Male to 3.5mm Female, 26.5 GHz (IL = .33 dB@ 10 GHz)
2	Pasternack Precision Adapters, 2.9 mm Male to 2.9(K) Male, Max. VSWR 1.40 @ 40GHz
2	Pasternack Precision Adapters, 3.5 mm Male to 2.9(K) Male, Max.VSWR 1.25 @ 34GHz

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Related time and frequency test parameter data recorded for this report were gathered simultaneously.

Frequency (S-Parameter) Domain Procedures

Frequency data extraction involves two steps that first measure the frequency related time domain waveform followed by post-processing of the time domain waveforms into loss and crosstalk response parameters versus frequency. The first step utilizes the Tektronix CSA8000 time based instrument to capture frequency related single-ended or differential signal types propagating through an appropriately prepared SUT. The second step involves a correlation of the time based waveforms using the TDA Systems IConnect software tool to post-process these waveforms into frequency response parameters. TDA Systems labels these frequency related waveform relationships as the *Step* and *DUT* reference. This report establishes the setup procedures for defining the *Step* and *DUT* reference for frequency parameters of interest. Once established, the *Step* and *DUT* references are post-processed in IConnect's S-parameter computations window.

CSA8000 Setup

Listed below are the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. These frequency boundaries are determined by a time domain instruments functional settings such as window length, number of points and averaging capability. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process.

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss

SUT Preparation – Use path J16 to J5 *(Figure 3)* for top entry through measurements and J6_7 to J6_7 *(Figure 4)* for differential through measurements. Adjacent inactive transmission paths are terminated 50Ω to GND single-ended or 100Ω differentially.

Step Reference - Establish this waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. A transmission path can be completed by inserting a negligible length of transmission standard between the microwave probes. *(**Note:** Calibration standards are located on the Samtec PCB=100251-01 fixture)*

DUT Reference - Establish this waveform by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the transmission standard *and record* measurement

Return Loss

SUT Preparation – – Use J16 to J5 as the single ended impedance matched path and J6_7 to J6_7 as the differential impedance matched path. Adjacent inactive transmission paths are terminated 50Ω to GND single-ended or 100Ω differentially.

Step Reference - Establish the waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including the open standard.

DUT Reference - Establish the waveform by making a TDT (matched) reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Cables and adapters located on the far-end of the inserted SUT provide the resistive load impedance that closely matches the test systems input impedance condition of 50Ω single-ended or 100Ω differential.

Near-End Crosstalk (NEXT*)*

SUT Preparation - Establish 50Ω to GND terminations at single-ended probe paths J3, J5, J17, J18 & J36 and either 50Ω to GND or 100Ω across differential paths at probe paths J27_28, J25_26, J6_7, J3_4, &, J54_55 of the PCB-100256-01 fixture *(Figure 2)*. Dependent on the coupling configuration under test, terminate all single ended and differential probing paths on the PCB100251-02 fixture *(Figure 1, edge card)* that are not being actively driven or monitored.

Step Reference - Establish this waveform by making an active measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard.

DUT Reference - Establish these waveforms by driving an active signal line (i.e.; J16) and recording the TDR coupled energy at the adjacent near-end (i.e.; J18). Repeat measurement procedures to establish the waveforms for worse case and across row (xrow) coupling conditions for both signal types.

Far-End Crosstalk (FEXT)

SUT Preparation - - Establish 50Ω to GND terminations at single-ended probe pads J4, J18 & J36 and either 50Ω to GND or 100Ω across differential paths at probe pads J25_26, J3_4 & J54_55 on the PCB-100251-02 fixture *(Figure 1)*. Establish 50Ω to GND terminations at single-ended probe pads J18, J5 & J36 and either 50Ω to GND or 100Ω across differential paths at probe pads J27_28, J6_7 & J54_55 on the PCB-100251-01 fixture *(Figure 2)*. Dependent on the coupling configuration under test, terminate the single ended and differential probing paths on the PCB100251-01 & PCB100251-02 fixtures *(Figures 1&2)* that are not being actively driven or monitored.

Step Reference - Establish this waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. The transmission path is completed by inserting a negligible length of transmission standard *(Figure 4)* between the microwave probes.

DUT Reference - Establish these waveforms by driving an active signal line (i.e.; J16) and recording the TDR coupled energy at the adjacent far-end (i.e., J3). Repeat procedures to establish the waveforms for worse case and across riser card (xrow) coupling conditions for both signal types.

Series: SAL1 (Qty=2)
Description: Perpendicular Board-to-Board, 1.0mm Pitch, Edge Card Top Entry

Time Domain Procedures

Measurements involving digital type pulses are performed utilizing either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. For this series of tests, TDR methods are employed for the impedance and propagation delay measurements. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to accurately and fully characterize the SUT.

Impedance

The signal line(s) of the SUT's signal configuration is energized with a TDR pulse. The far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited.

Propagation Delay

This connector series uses the fastest edge rate (30ps) of the TDR impedance waveform to measure propagation delay. . Differential or single ended signal delay is the measured difference of propagation between the known signal trace length delay and the delay of the mated SUT. The measurement is a one-way propagation result. Termination of the adjacent signal lines into the test systems characteristic impedance eliminate alternate current paths providing for better measurement accuracy.

Crosstalk

An active pulsed waveform is transmitted through a selected SUT signal line. The adjacent quiet signal lines are monitored for the coupled energy at the near-end and far-end. Active and quiet lines not being monitored are terminated in the test systems characteristic impedance. Signal lines adjacent to the quiet lines remain terminated on both ends throughout the test sequence. Failing to terminate the active near or far end, quiet lines, or in some cases, signal lines adjacent to the quiet line may have an effect on amplitude and shape of the coupled energy.

Appendix F – Glossary of Terms

BC – Best Case crosstalk configuration
DP – Differential Pair signal configuration
DUT – Device under test; TDA IConnect reference waveform
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SUT – System under test
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worse Case crosstalk configuration
Xrow^{se} – Cross ground/ power bar crosstalk, single-ended signal
Xrow^{diff} – Cross ground/ power bar crosstalk, differential signal
Z – Impedance (expressed in ohms)