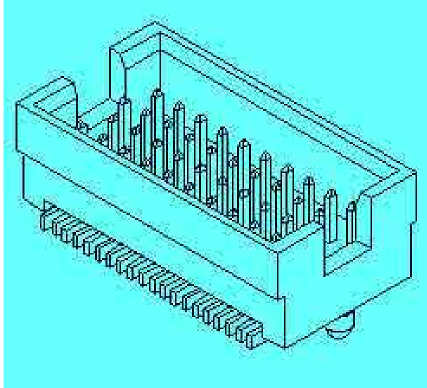
High Speed Characterization Report

TOLC-110-32-S-Q-L-C



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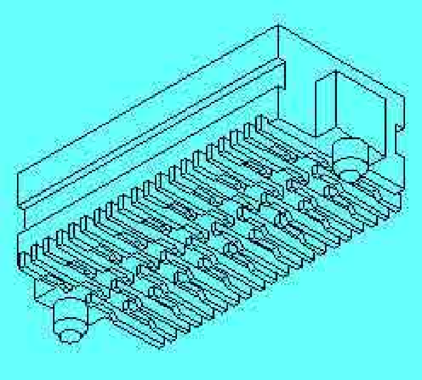

SOLC-110-02-S-Q-L-C

Description:

Quad Row, Surface Mount, Board-to-Board Connector Series, 1.27mm Pitch, 12mm (0.472”) Stack Height

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Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

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Connector Overview

SOLC/TOLC Series interfaces are available as a 1.27mm (.050") square pitch quad row connector system. The staggered row system results in a surface mount 0.635mm (.025") terminal pitch. The quad series is available with up to 50 contacts per row and has standard board-to-board spacings of 6.35mm (0.250) and 12mm (0.472). The data in this report is applicable only to the 12mm (0.472) board-to-board stack height version.

Connector System Speed Rating

SOLC/TOLC Series, Quad Row,1.27mm (.050") pitch, 12mm (0.472") Stack Height

Signaling	Speed Rating
Single-Ended:	**5.5 GHz / 11 Gbps**
Differential:	**5.5 GHz / 11 Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board's trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/ 15 Gbps.

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Frequency Domain Data Summary

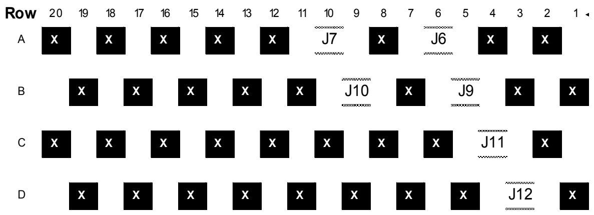
Table 1 - Single-Ended Connector System Performance

Test Parameter	Source	Victim	
Insertion Loss	port1=J6; port2=J35		**-3dB @ 5.16 GHz**
Return Loss	port1=J6; port2=J35		≤ -5 dB to 5.16 GHz
Near-End Crosstalk	J6 (SE1)	J9 (SE1)	≤ -12dB to 5.16 GHz
	J9 (SE1)	J11 (SE1)	≤ -8dB to 5.16 GHz
	J16 (SE2)	J17 (SE2)	≤ -12dB to 5.16 GHz
	J6 (SE1)	J7 (SE1)	≤ -25dB to 5.16 GHz
Far-End Crosstalk	J6 (SE1)	J37 (SE1)	≤ -8dB to 5.16 GHz
	J9 (SE1)	J39 (SE1)	≤ -22dB to 5.16 GHz
	J16 (SE2)	J44 (SE2)	≤ -25dB to 5.16 GHz
	J6 (SE1)	J36 (SE1)	≤ -18dB to 5.16 GHz

Pin Map (reference Appendix C for full description of test boards)

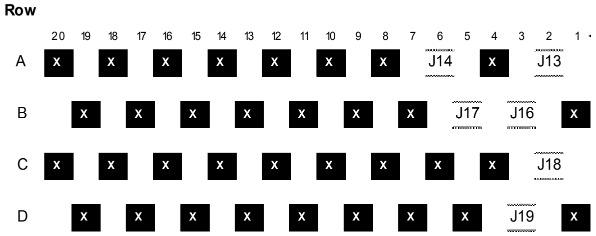
SE1:

SOLC (J1)

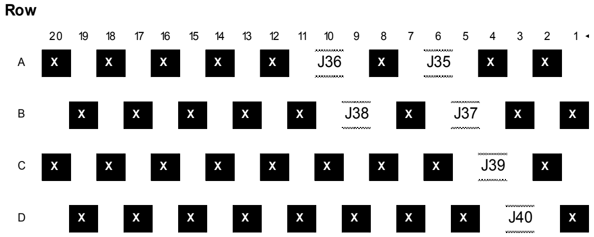


SE2:

SOLC (J8)



TOLC (J2)



TOLC (J3)

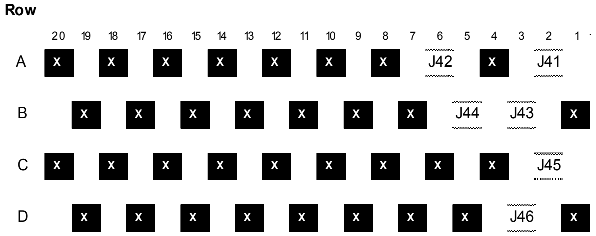


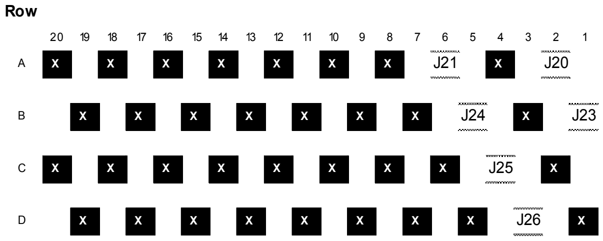
Table 2 - Differential Connector System Performance

Test Parameter	Source	Victim	
Insertion Loss	Port1= J21-J24 Port 2 = J48-J50	[redacted]	**-3dB @ 5.11 GHz**
Return Loss	Port1= J21-J24 Port 2 = J48-J50	[redacted]	≤ -5dB to 5.11 GHz
Near-End Crosstalk	J34-J28 (DP2)	J33-J27 (DP2)	≤ -12dB to 5.11 GHz
	J21-J24 (DP1)	J25-J26 (DP1)	≤ -18dB to 5.11 GHz
	J14-J17 (SE2)	J13-J16 (SE2)	≤ -18dB to 5.11 GHz
	J34-J28 (DP2)	J30-J32 (DP2)	≤ -22dB to 5.11 GHz
	J21-J24 (DP1)	J20-J23 (DP1)	≤ -30dB to 5.11 GHz
Far-End Crosstalk	J34-J28 (DP2)	J53-J55 (DP2)	≤ -15dB to 5.11 GHz
	J21-J24 (DP1)	J51-J52 (DP1)	≤ -25dB to 5.11 GHz
	J14-J17 (SE2)	J41-J43 (SE2)	≤ -22dB to 5.11 GHz
	J34-J28 (DP2)	J58-J60 (DP2)	≤ -18dB to 5.11 GHz
	J21-J24 (DP1)	J47-J49 (DP1)	≤ -28dB to 5.11 GHz

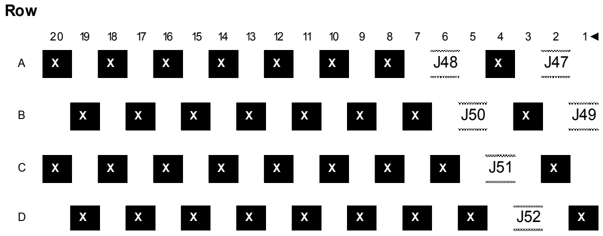
Pin Map (reference Appendix C for full description of test boards)

DP1:

SOLC (J15)

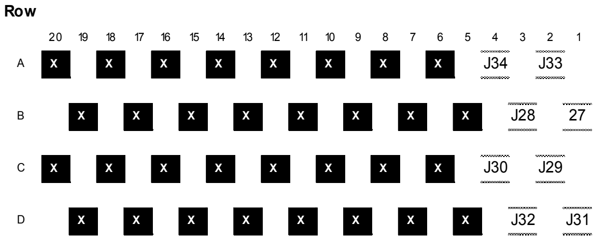


TOLC (J4)

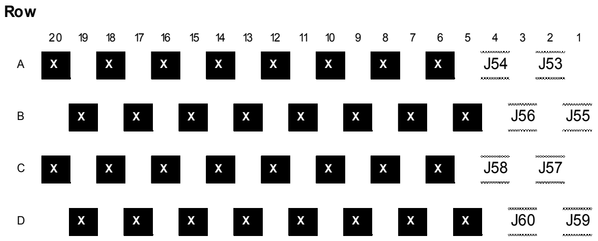


DP2:

SOLC (J22)



TOLC (J5)



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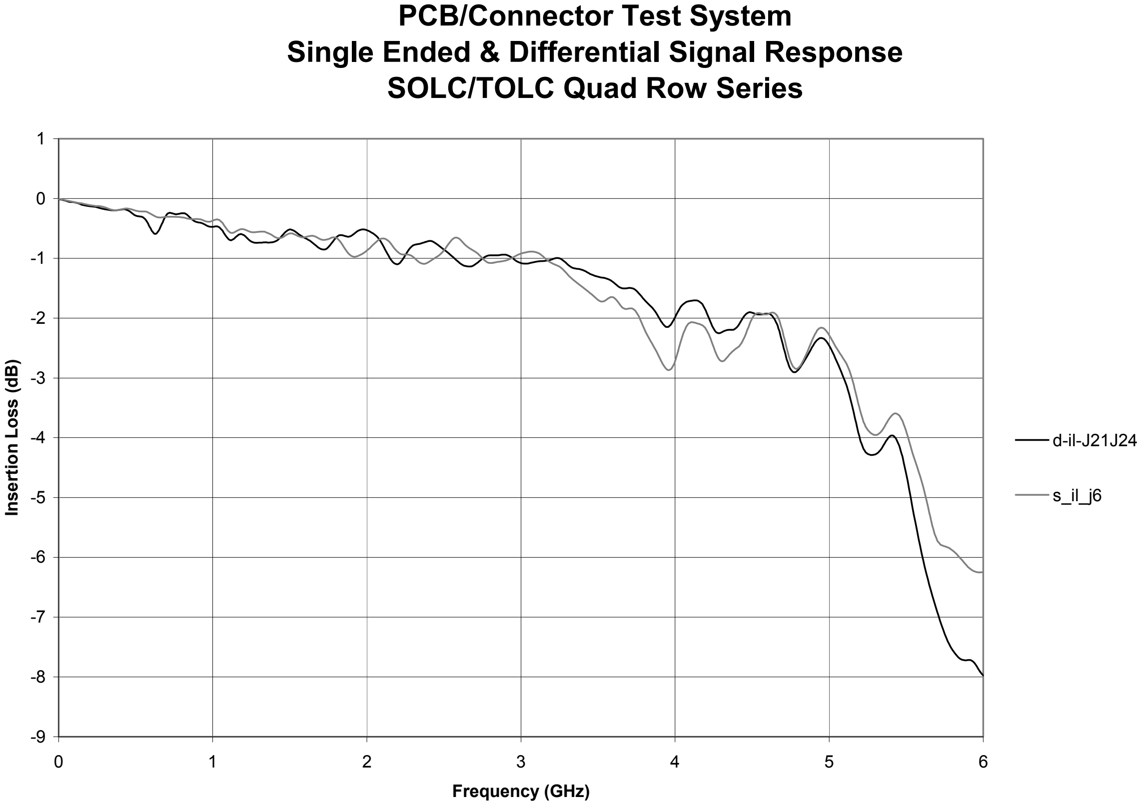
Bandwidth Chart - Single-Ended & Differential Insertion Loss



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Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω)

Signal Risetime	30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	74.7	66.8	58.8	51.8	50.6	50.4	50.2
Minimum Impedance	35.2	39.3	43.5	47.1	49.2	49.7	49.9

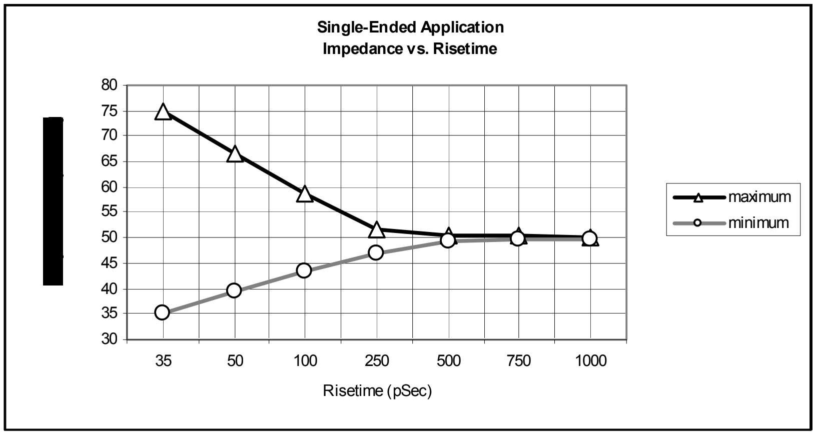
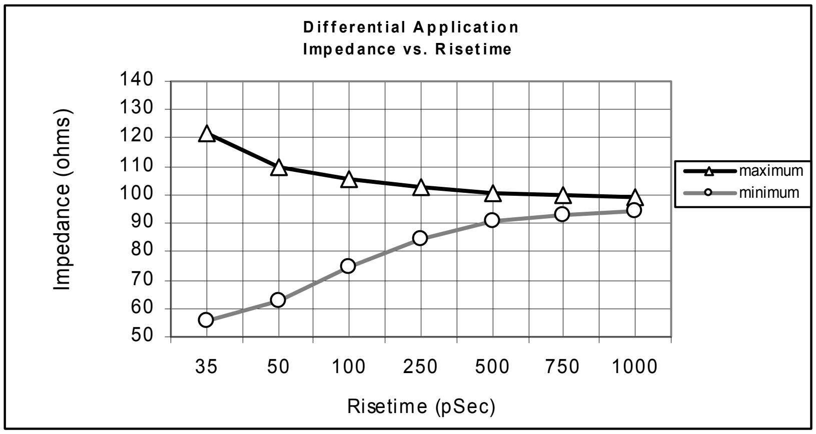


Table 4 - Differential Impedance (Ω)

Signal Risetime	30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	121.5	110.0	105.8	102.4	100.9	99.7	99.4
Minimum Impedance	55.5	62.5	74.3	84.6	90.4	93.1	94.6



Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
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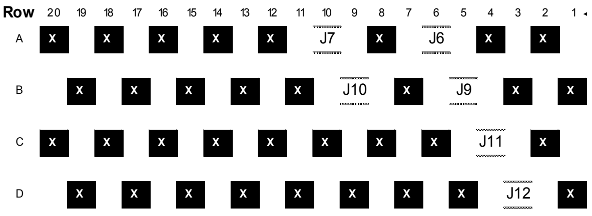
Table 5 - Single-Ended Crosstalk (%)

Input (t_r)	Source	Victim	30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	J6 (SE1)	J9	11.7	8.1	5.9	3.5	3.5	2.5	1.9
	J9 (SE1)	J11	8.8	7.5	6.2	4.0	2.3	1.6	1.3
	J16 (SE2)	J17	8.1	7.2	6.2	3.6	2.0	1.4	1.1
	J6 (SE1)	J7	2.4	1.9	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	J6 (SE1)	J37	7.9	6.0	4.3	1.9	< 1.0%	< 1.0%	< 1.0%
	J9 (SE1)	J39	3.7	2.5	1.9	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	J16 (SE2)	J44	3.4	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	J6 (SE1)	J36	2.2	1.6	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%

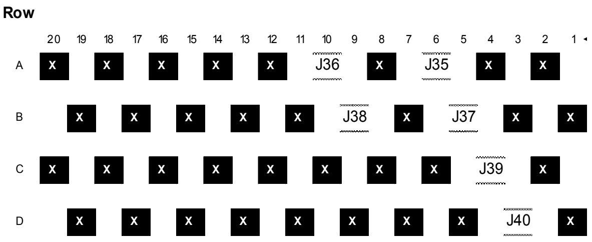
Pin Map (reference Appendix C for full description of test boards)

SE1:

SOLC (J1)

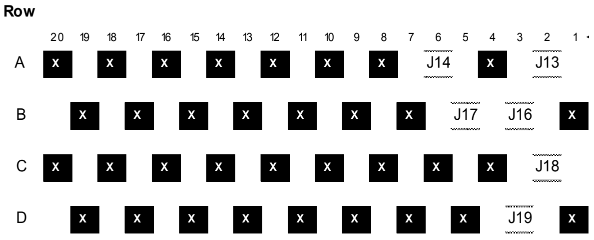


TOLC (J2)



SE2:

SOLC (J8)



TOLC (J3)

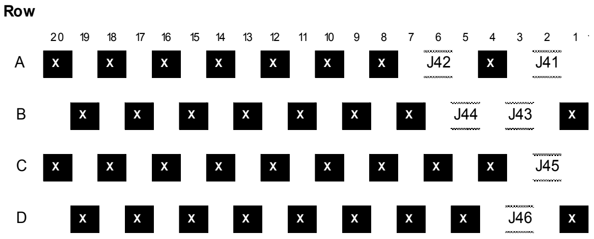
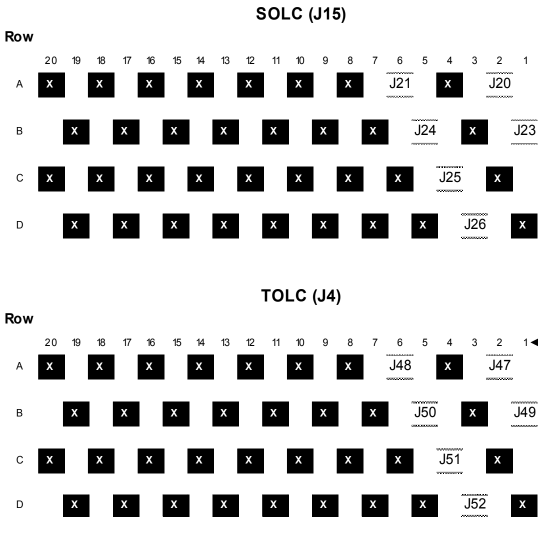


Table 6 - Differential Crosstalk (%)

Input (t_r)	Source	Victim	30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	J34-J28 (DP2)	J33-J27	4.7	3.5	2.9	1.1	< 1.0%	< 1.0%	< 1.0%
	J21-J24 (DP1)	J25-J26	3.6	3.0	2.7	1.5	< 1.0%	< 1.0%	< 1.0%
	J14-J17 (SE2)	J13-J16	3.3	2.8	2.8	1.5	< 1.0%	< 1.0%	< 1.0%
	J34-J28 (DP2)	J30-J32	3.1	2.2	2.1	1.2	< 1.0%	< 1.0%	< 1.0%
	J21-J24 (DP1)	J20-J23	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	J34-J28 (DP2)	J53-J55	6.7	4.6	3.1	1.3	< 1.0%	< 1.0%	< 1.0%
	J21-J24 (DP1)	J51-J52	1.9	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	J14-J17 (SE2)	J41-J43	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	J34-J28 (DP2)	J58-J60	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	J21-J24 (DP1)	J47-J49	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)

DP1:



DP2:

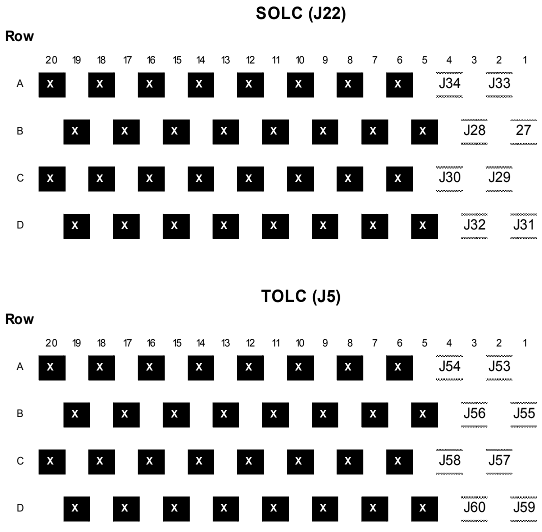


Table 7 - Propagation Delay (Mated Connector)	
Single-Ended	75ps
Differential	78ps

Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from the test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

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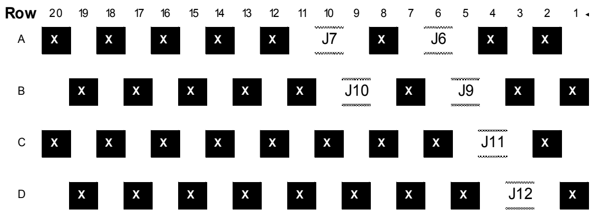
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

For this connector, the following configurations were evaluated (reference Appendix C for full description of test boards):

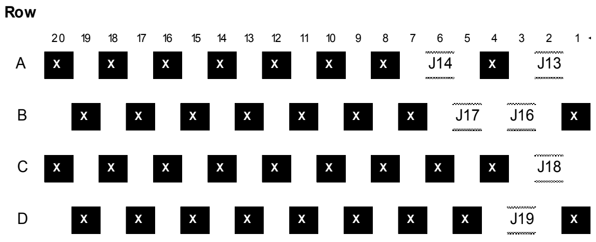
SE1:

SOLC (J1)

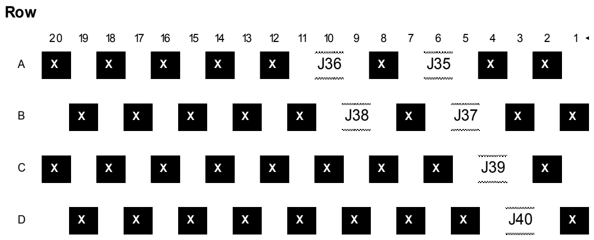


SE2:

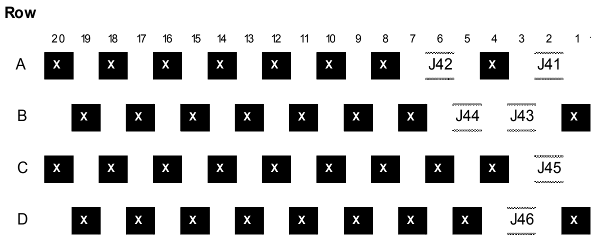
SOLC (J8)



TOLC (J2)



TOLC (J3)



Single-Ended Impedance:

- Well-referenced line (reference SE1)

Single-Ended Crosstalk:

- Well-referenced line; mimics 1:1 S:G ratio (reference SE1)
- 2:1 S:G ratio (reference SE2)

Only one single-ended signal was driven for crosstalk measurements.

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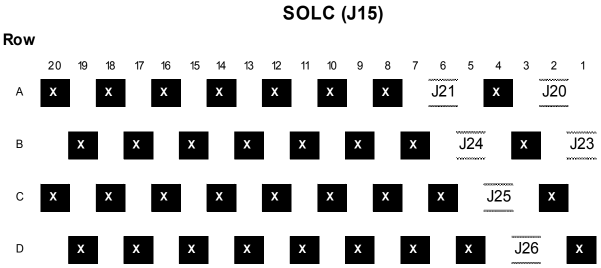
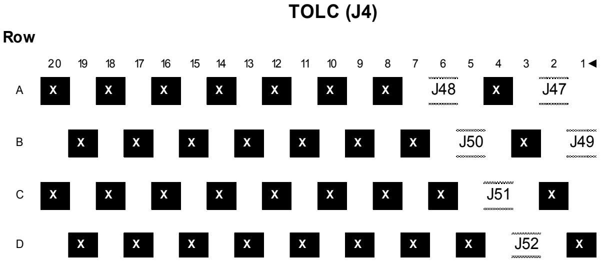
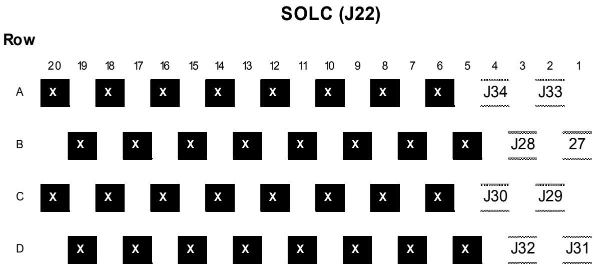
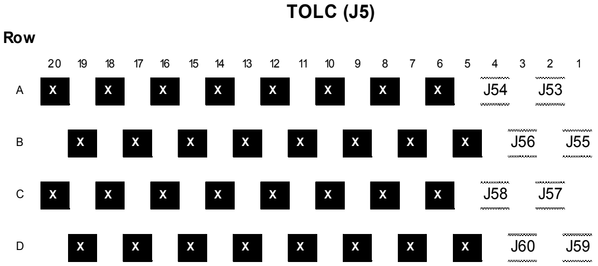
DP1:


SOLC (J15)


TOLC (J4)

DP2:


SOLC (J22)


TOLC (J5)

Differential Impedance**:**

- Well-referenced line (reference DP1)

Differential Crosstalk**:**

- Well-referenced line; mimics 1:1 S:G ratio (reference DP1)
- Higher Signal Density (reference SE2)
- Full-Column Differential (reference DP2)

Only one differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

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Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of an interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, rise times were measured at 10%-90% signal levels.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system’s signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT’s frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 30 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 30 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

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Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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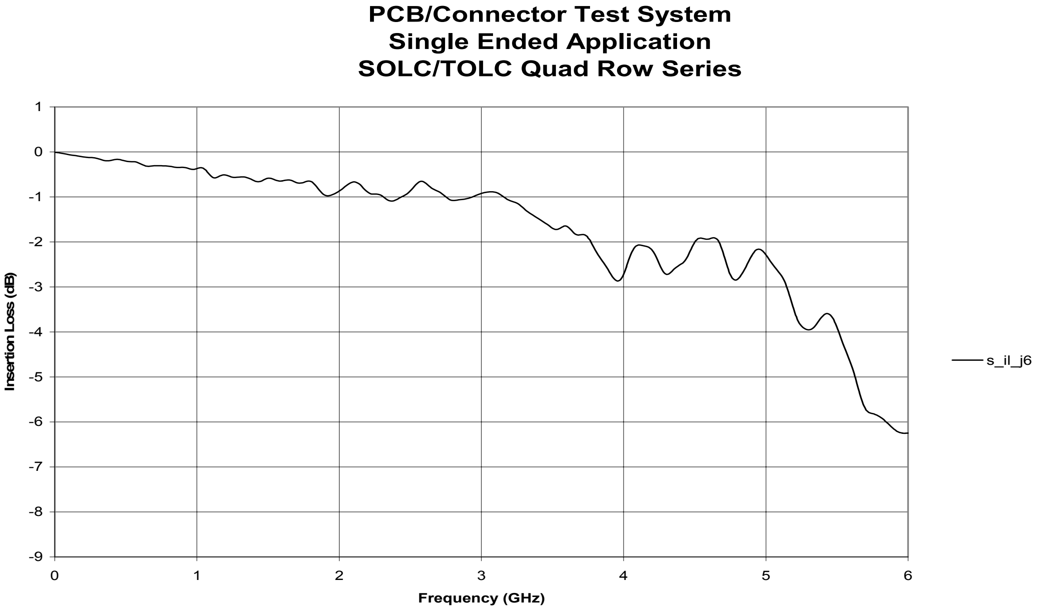
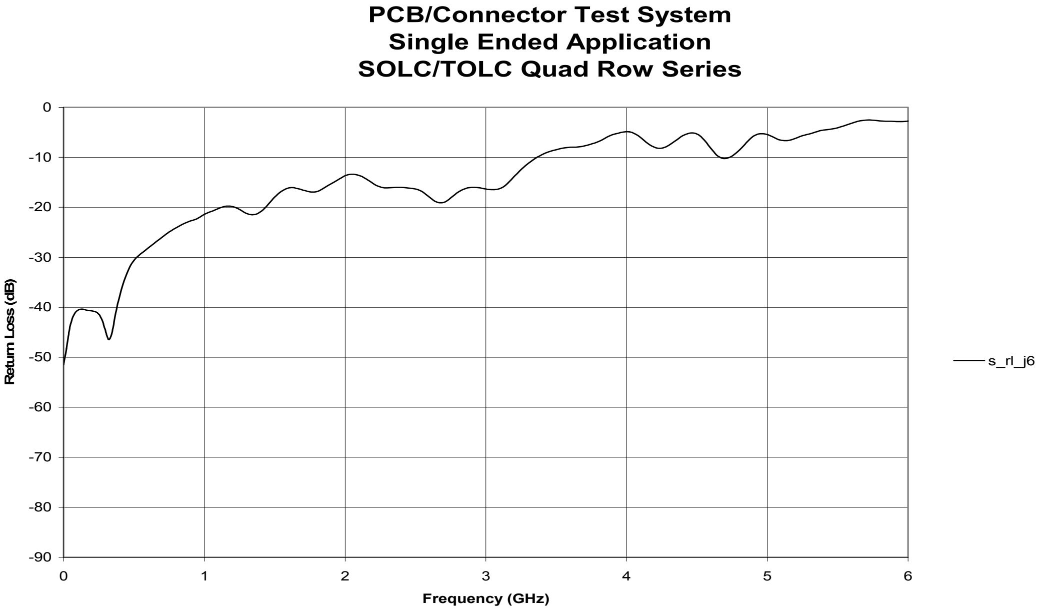
Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss

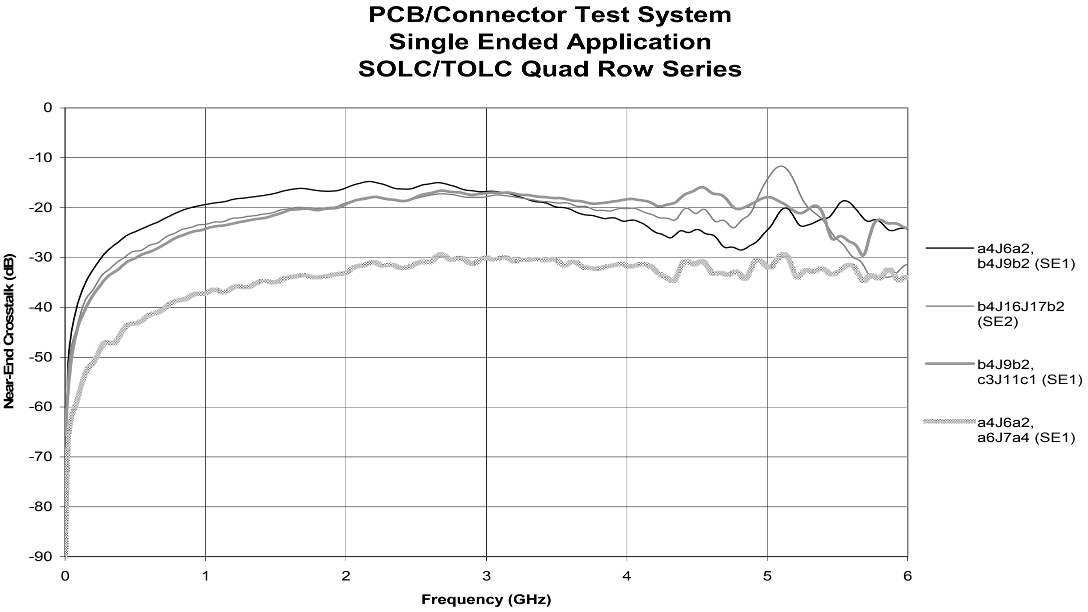


Single-Ended Application – Return Loss

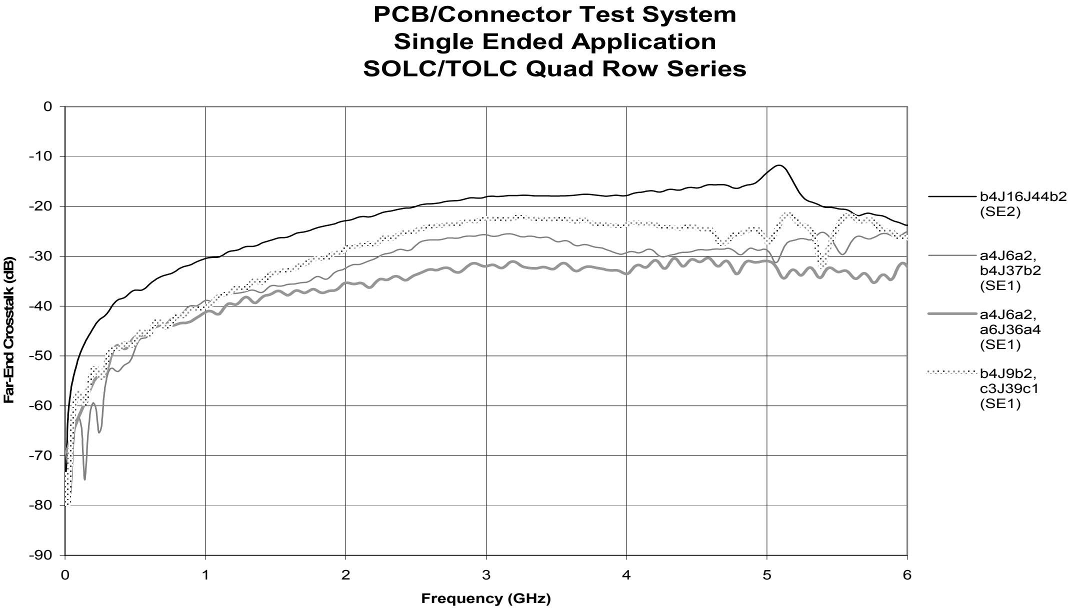


Series: TOLC/SOLC, 1.27mm (0.050") Contact Pitch, 0.64mm (0.025") Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472") Stack Height

Single-Ended Application – NEXT

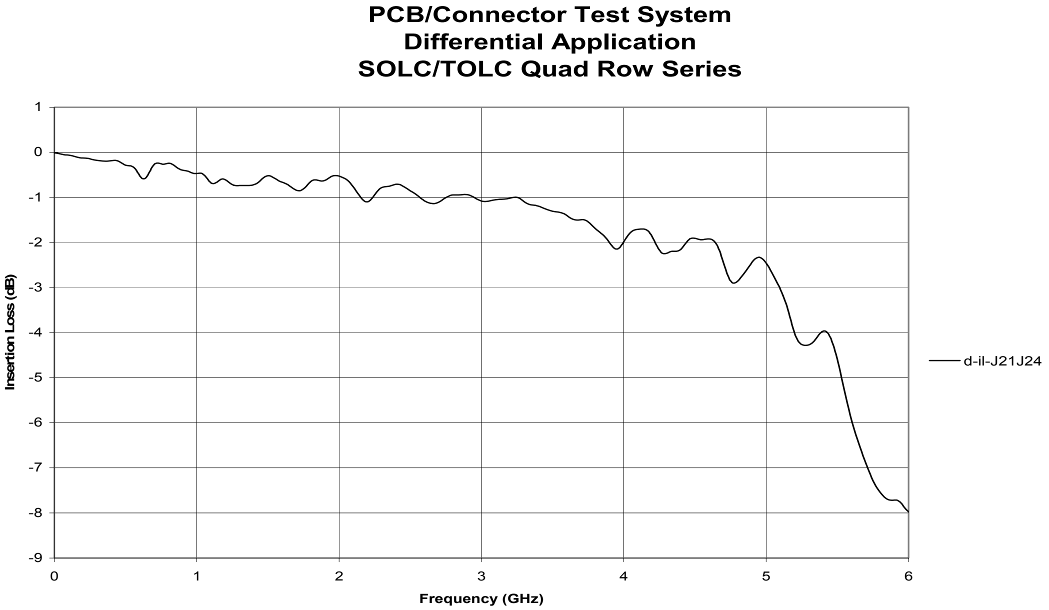


Single-Ended Application – FEXT

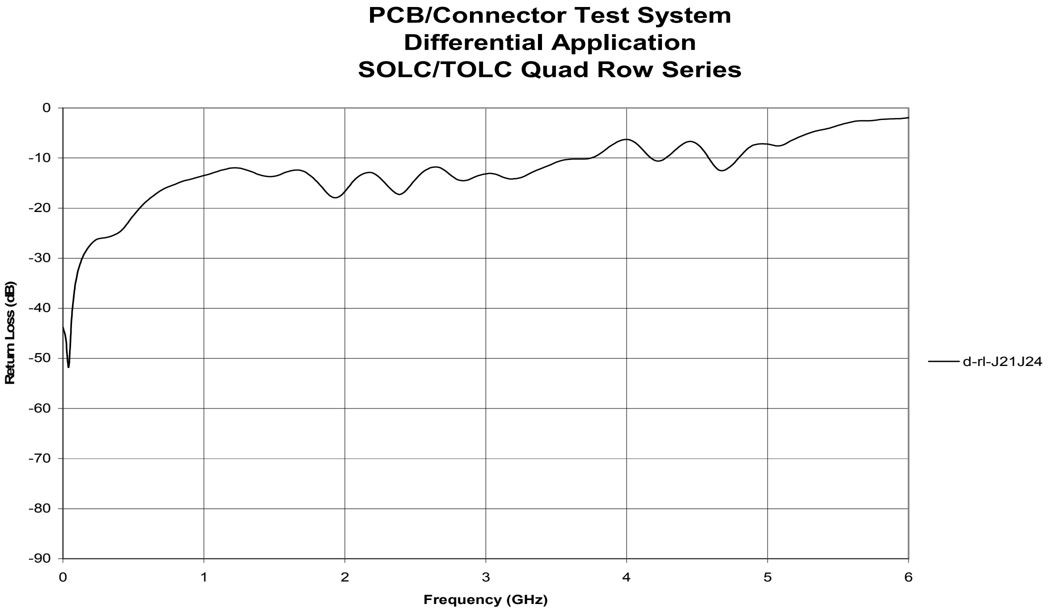


Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Differential Application – Insertion Loss

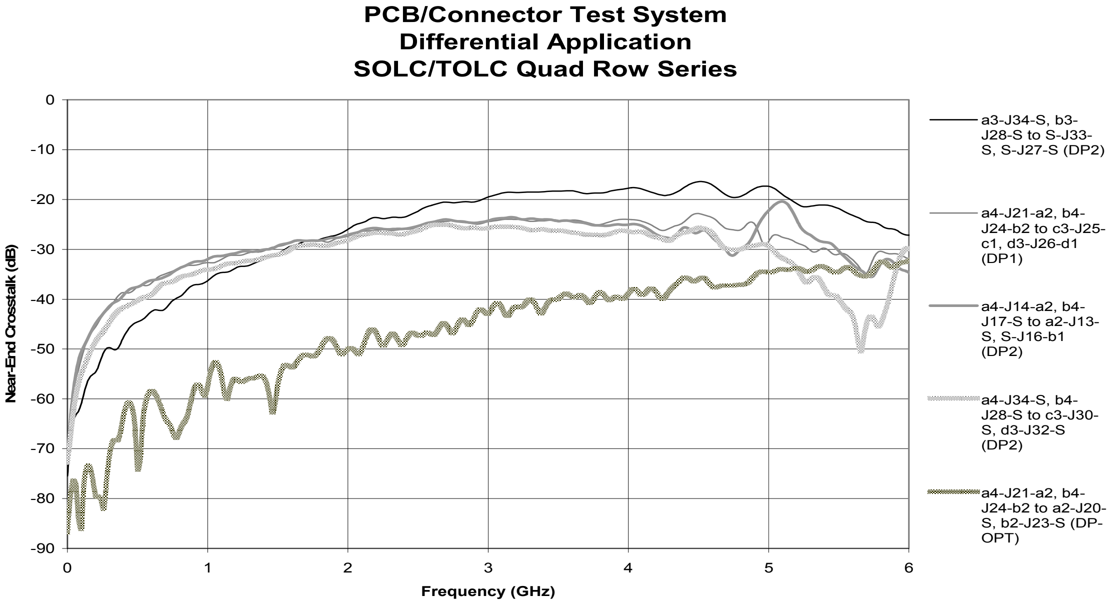

PCB/Connector Test System
Differential Application
SOLC/TOLC Quad Row Series

Differential Application – Return Loss

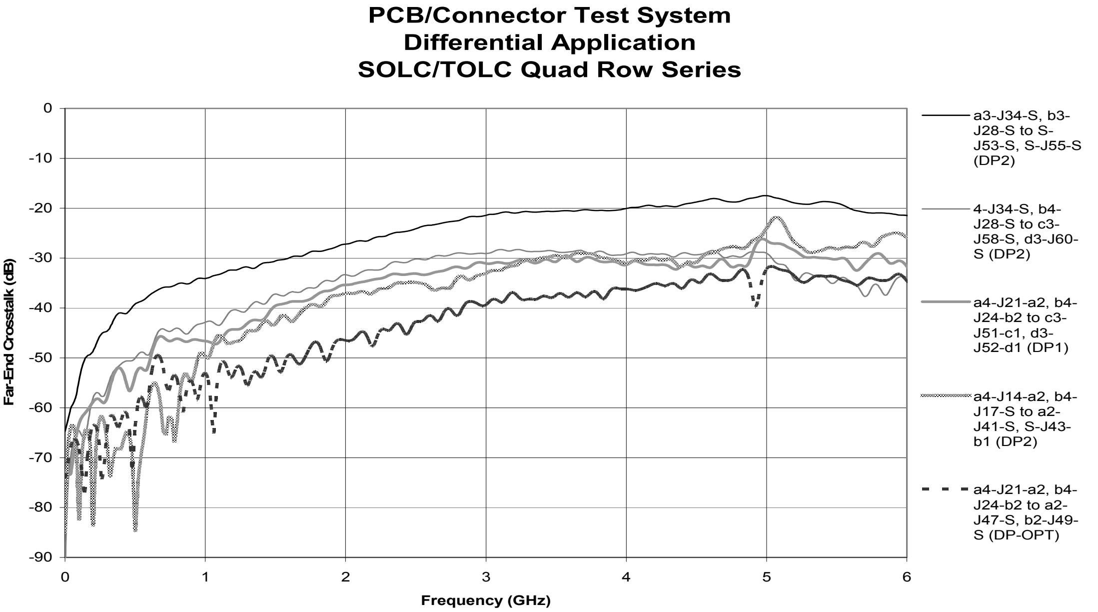

PCB/Connector Test System
Differential Application
SOLC/TOLC Quad Row Series

Series: TOLC/SOLC, 1.27mm (0.050") Contact Pitch, 0.64mm (0.025") Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472") Stack Height

Differential Application – NEXT


PCB/Connector Test System
Differential Application
SOLC/TOLC Quad Row Series

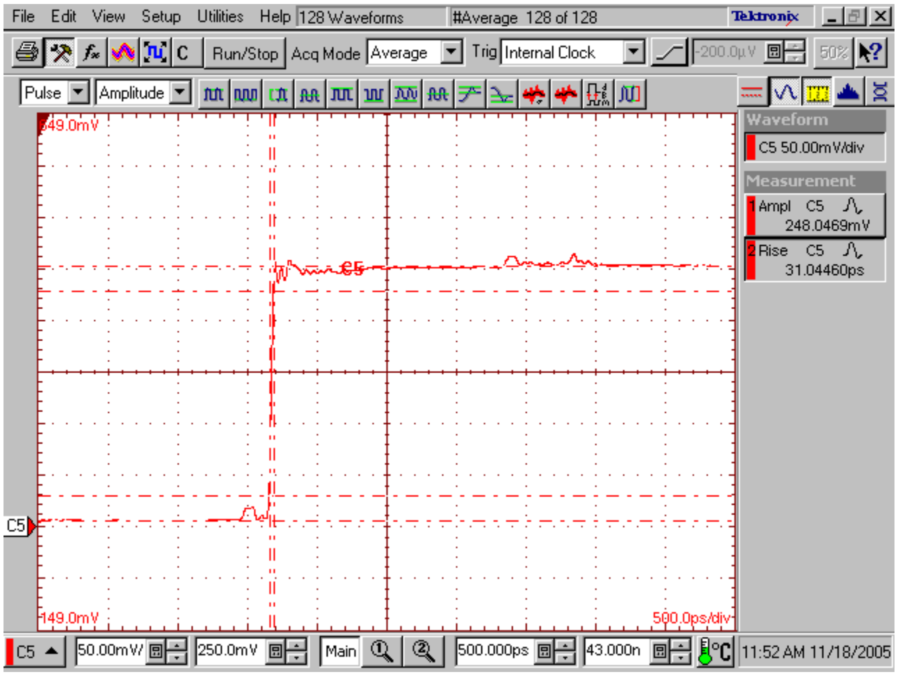
Differential Application – FEXT


PCB/Connector Test System
Differential Application
SOLC/TOLC Quad Row Series

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Appendix B – Time Domain Response Graphs

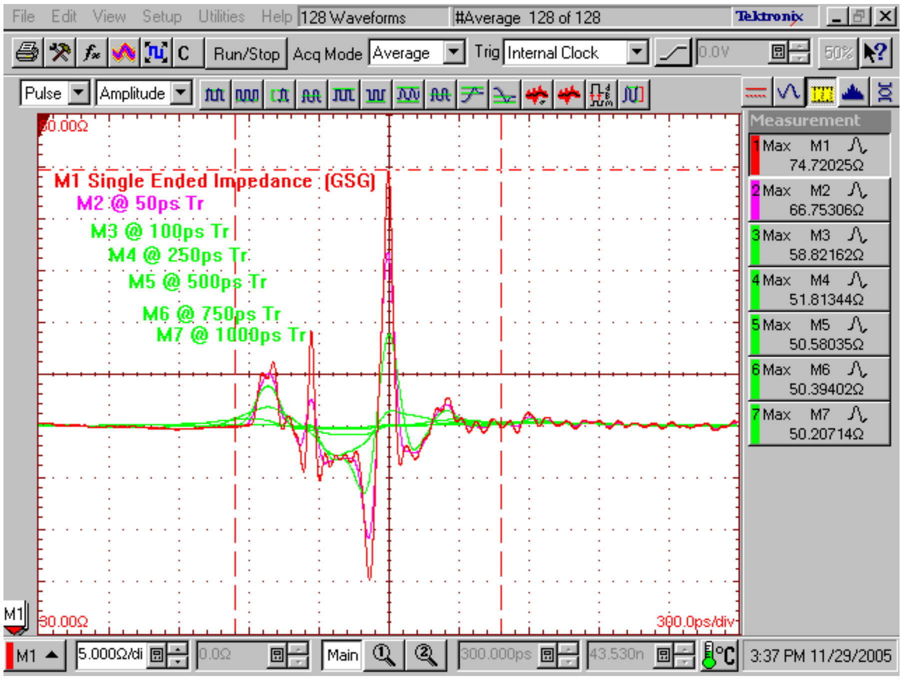
Single-Ended Application – Input Pulse


128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
Waveform
C5 50.00mV/div
Measurement
1 Ampl C5 248.0469mV
2 Rise C5 31.04460ps
C5 50.00mV/ 250.0mV
Main 500.000ps 43.000n
11:52 AM 11/18/2005

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Single-Ended Application – Impedance

Configuration: (Source = SOLC J6)



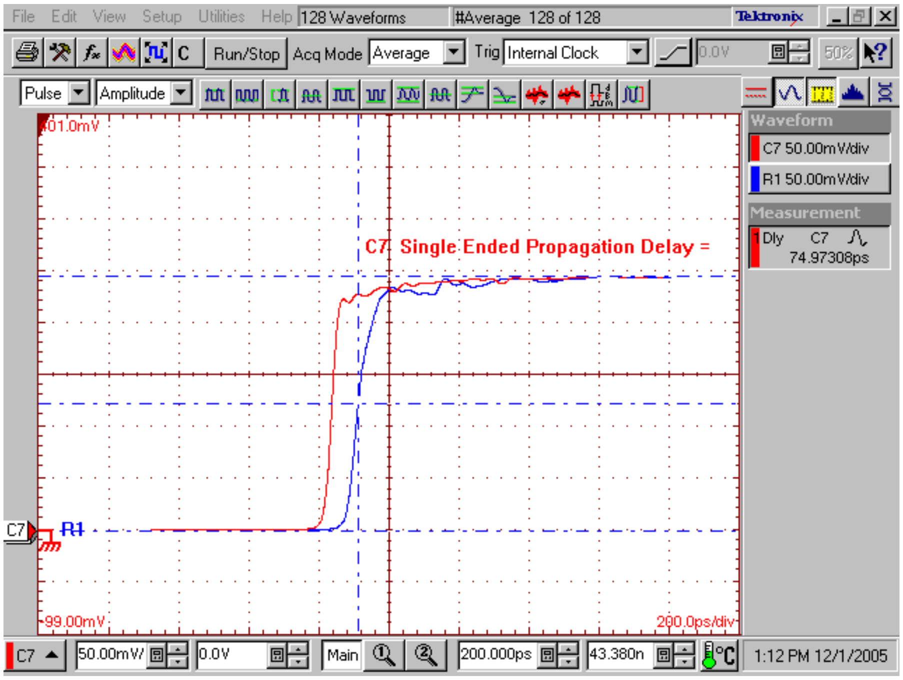
M1 Single Ended Impedance (GSG)
M2 @ 50ps Tr
M3 @ 100ps Tr
M4 @ 250ps Tr
M5 @ 500ps Tr
M6 @ 750ps Tr
M7 @ 1000ps Tr

Measurement
1 Max M1 74.72025Ω
2 Max M2 66.75306Ω
3 Max M3 58.82162Ω
4 Max M4 51.81344Ω
5 Max M5 50.58035Ω
6 Max M6 50.39402Ω
7 Max M7 50.20714Ω

M1 5.000Ω/di 0.0Ω Main 300.000ps 43.530n

Single-Ended Application – Propagation Delay

Configuration: (Source – SOLC J6)



Waveform
C7 50.00mV/div
R1 50.00mV/div

Measurement
1 Dly C7 74.97308ps

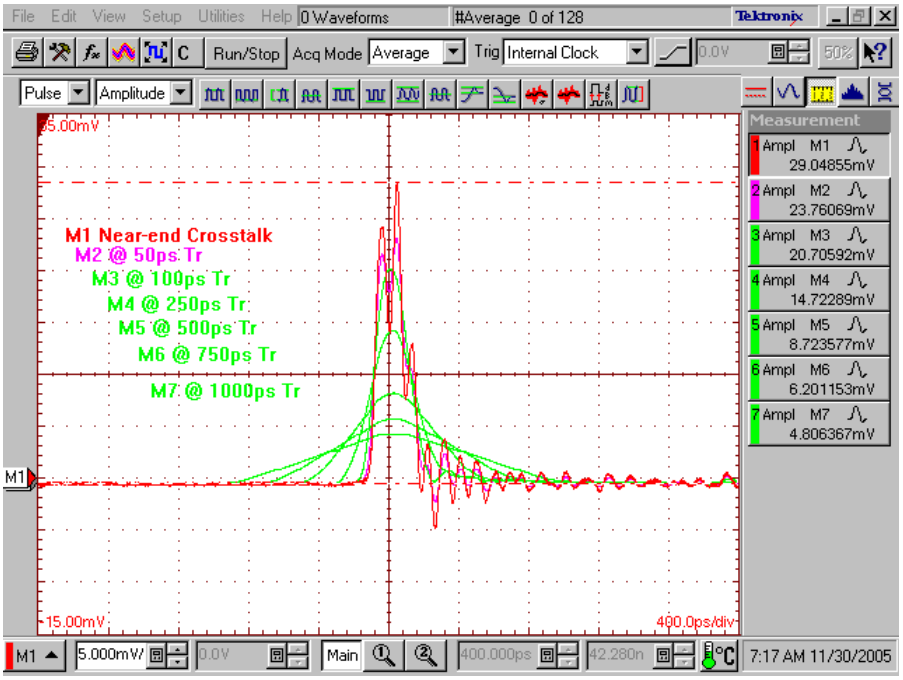
C7 Single Ended Propagation Delay =

C7 50.00mV 0.0V Main 200.000ps 43.380n

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Single-Ended Application – NEXT

Configuration: (SE1: Source = SOLC J6; Victim = SOLC J9)

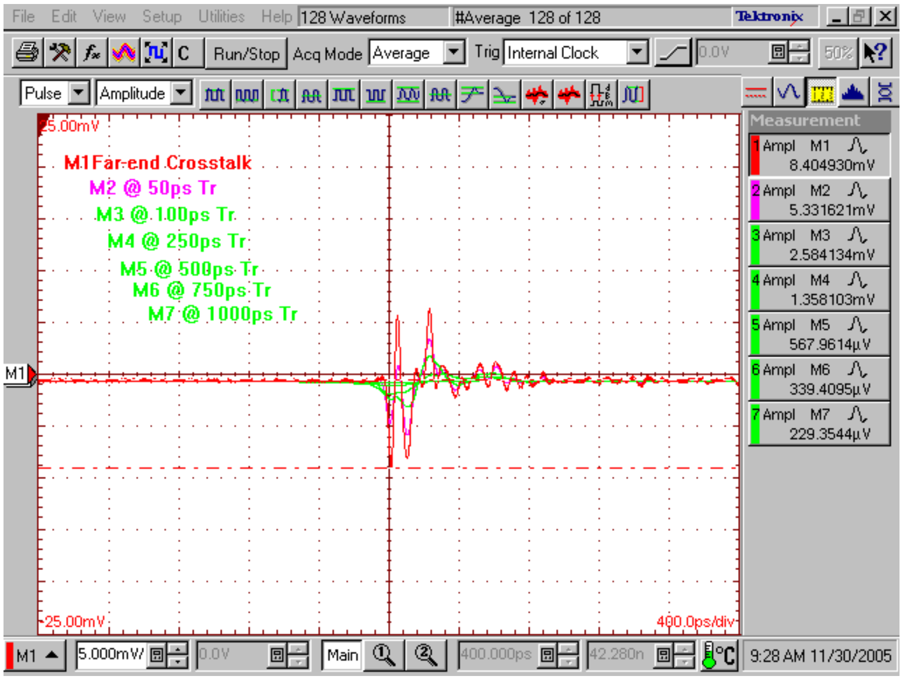


0 Waveforms #Average 0 of 128
Acq Mode Average
Trig Internal Clock
M1 5.000mV/

1 Ampl M1 29.04855mV
2 Ampl M2 23.76069mV
3 Ampl M3 20.70592mV
4 Ampl M4 14.72289mV
5 Ampl M5 8.723577mV
6 Ampl M6 6.201153mV
7 Ampl M7 4.806367mV

Single-Ended Application – FEXT

Configuration: (SE1: Source = SOLC J6; Victim = TOLC J37)



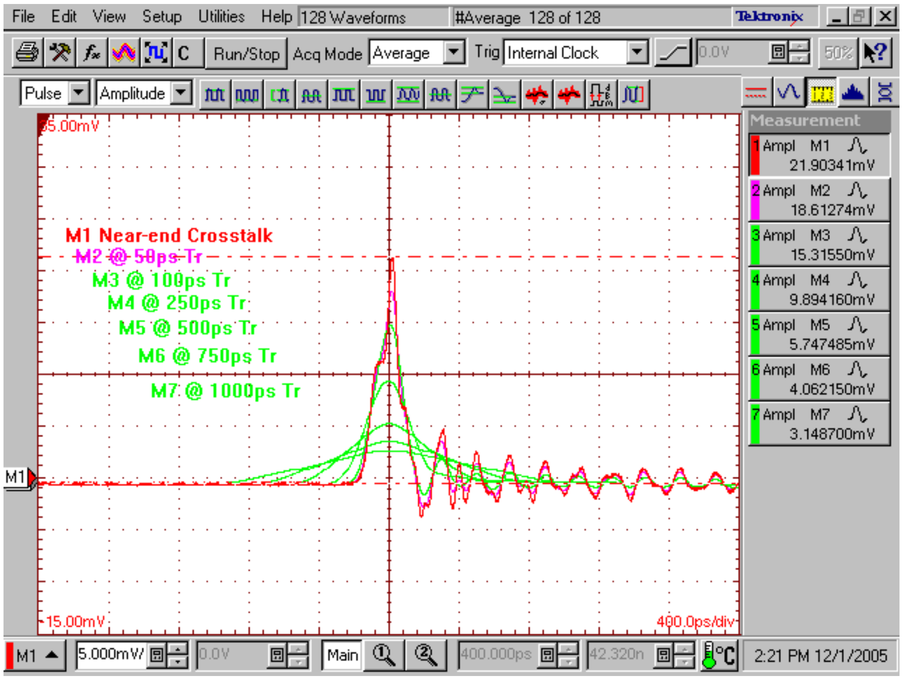
128 Waveforms #Average 128 of 128
Acq Mode Average
Trig Internal Clock
M1 5.000mV/

1 Ampl M1 8.404930mV
2 Ampl M2 5.331621mV
3 Ampl M3 2.584134mV
4 Ampl M4 1.358103mV
5 Ampl M5 567.9614µV
6 Ampl M6 339.4095µV
7 Ampl M7 229.3544µV

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Single-Ended Application – NEXT

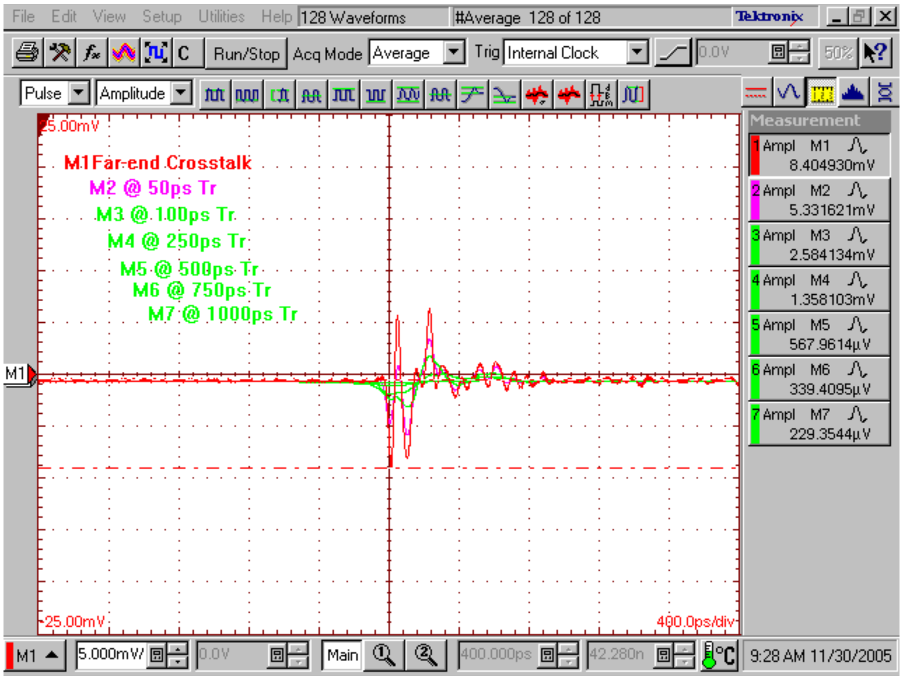
Configuration: (SE2: Source = SOLC J16; Victim = SOLC J17)



1 Ampl M1 21.90341mV
2 Ampl M2 18.61274mV
3 Ampl M3 15.31550mV
4 Ampl M4 9.894160mV
5 Ampl M5 5.747485mV
6 Ampl M6 4.062150mV
7 Ampl M7 3.148700mV

Single-Ended Application – FEXT

Configuration: (SE2: Source = SOLC J16; Victim = TOLC J44)

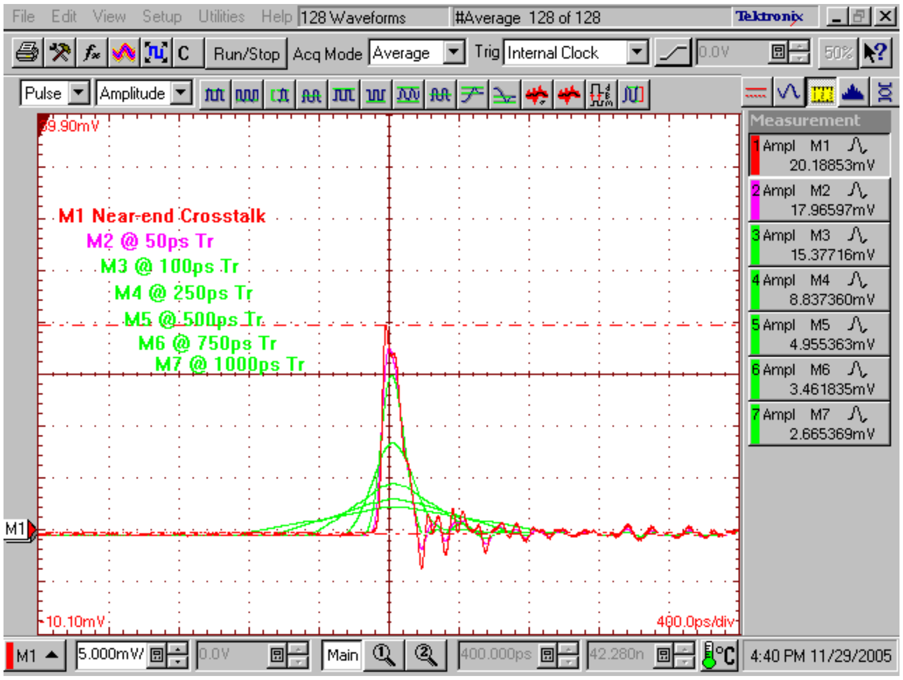


1 Ampl M1 8.404930mV
2 Ampl M2 5.331621mV
3 Ampl M3 2.584134mV
4 Ampl M4 1.358103mV
5 Ampl M5 567.9614µV
6 Ampl M6 339.4095µV
7 Ampl M7 229.3544µV

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Single-Ended Application – NEXT

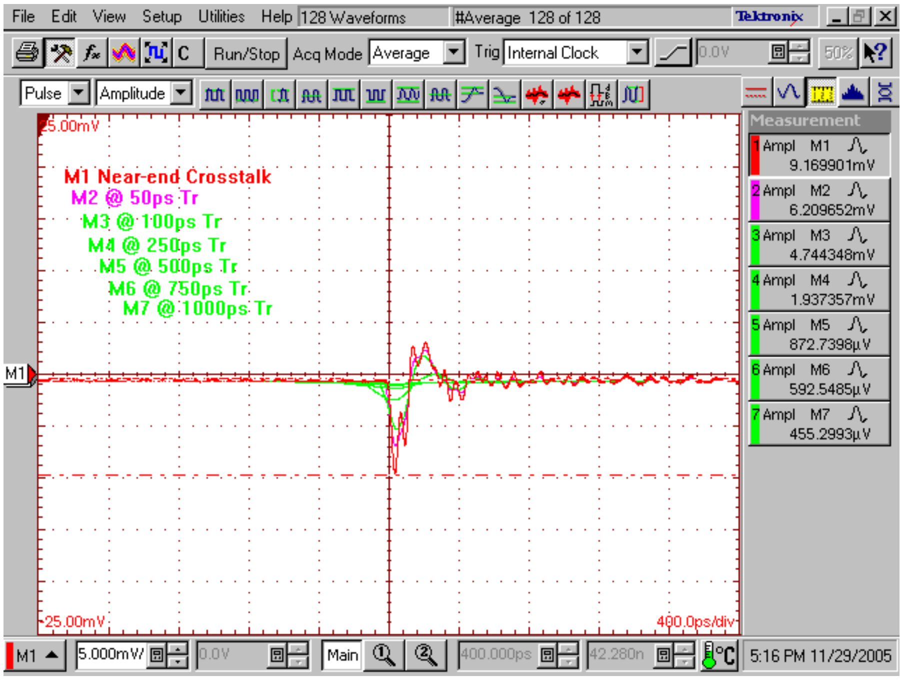
Configuration: (SE1: Source = SOLC J9; Victim = SOLC J11)



1 Ampl M1 20.18853mV
2 Ampl M2 17.96597mV
3 Ampl M3 15.37716mV
4 Ampl M4 8.837360mV
5 Ampl M5 4.955363mV
6 Ampl M6 3.461835mV
7 Ampl M7 2.665369mV

Single-Ended Application – FEXT

Configuration: (SE1: Source = SOLC J9; Victim = TOLC J39)

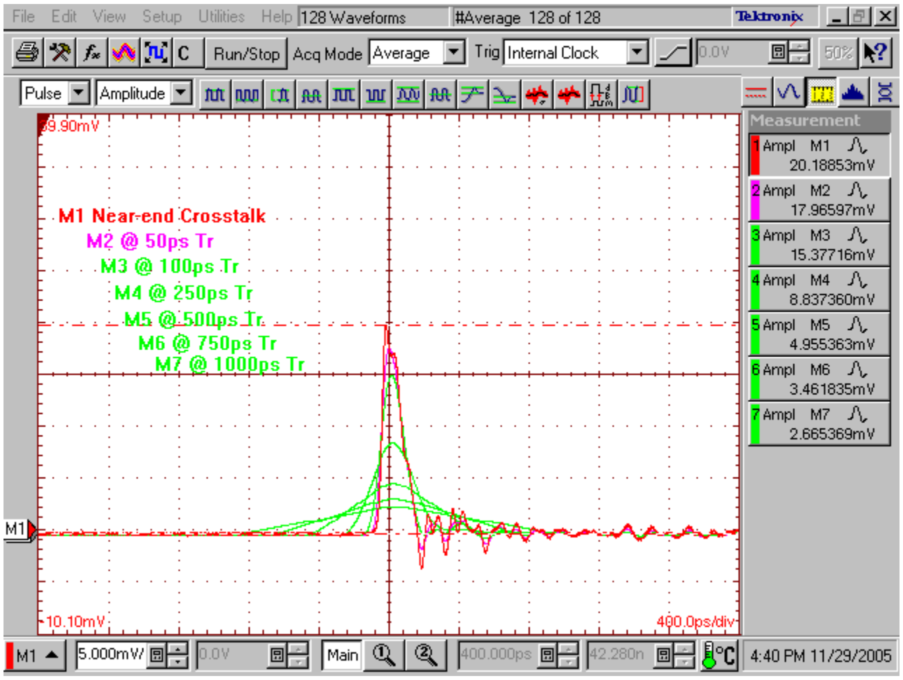


1 Ampl M1 9.169901mV
2 Ampl M2 6.209652mV
3 Ampl M3 4.744348mV
4 Ampl M4 1.937357mV
5 Ampl M5 872.7398µV
6 Ampl M6 592.5485µV
7 Ampl M7 455.2993µV

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Single-Ended Application – NEXT

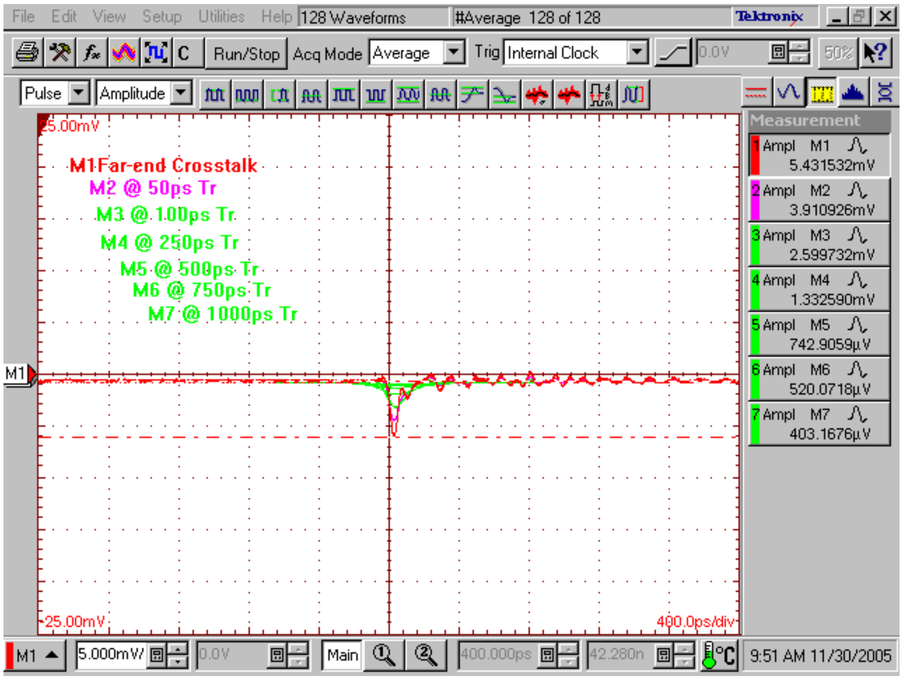
Configuration: (SE1: Source = SOLC J6; Victim = SOLC J7)



Measurement
1 Ampl M1 20.18853mV
2 Ampl M2 17.96597mV
3 Ampl M3 15.37716mV
4 Ampl M4 8.837360mV
5 Ampl M5 4.955363mV
6 Ampl M6 3.461835mV
7 Ampl M7 2.665369mV

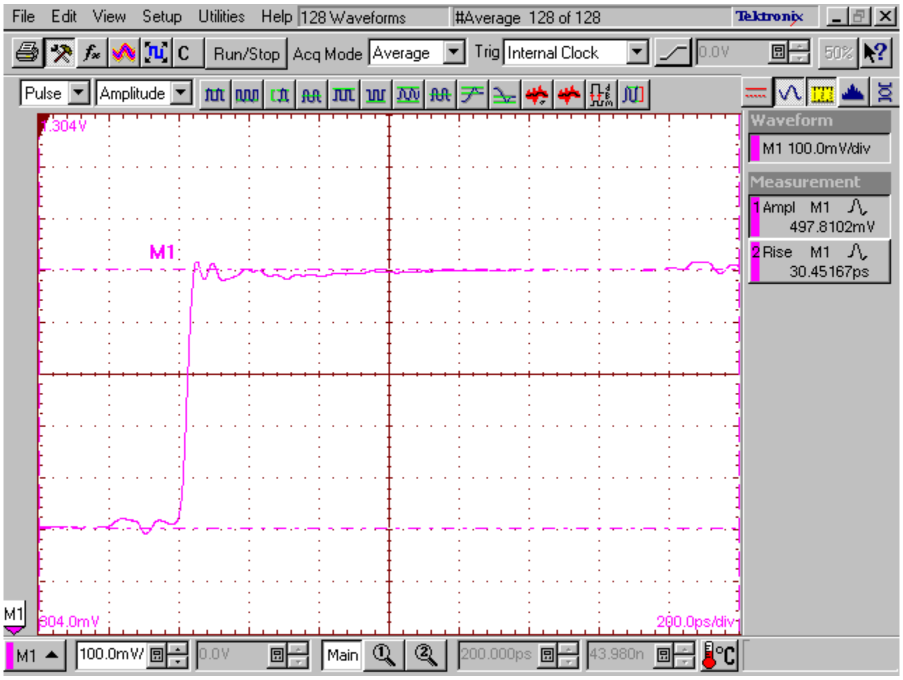
Single-Ended Application – FEXT

Configuration: (SE1: Source = SOLC J6; Victim = SOLC J36)



Measurement
1 Ampl M1 5.431532mV
2 Ampl M2 3.910926mV
3 Ampl M3 2.599732mV
4 Ampl M4 1.332590mV
5 Ampl M5 742.9059µV
6 Ampl M6 520.0718µV
7 Ampl M7 403.1676µV

Differential Application – Input Pulse



128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V
50%

Waveform
M1 100.0mV/div

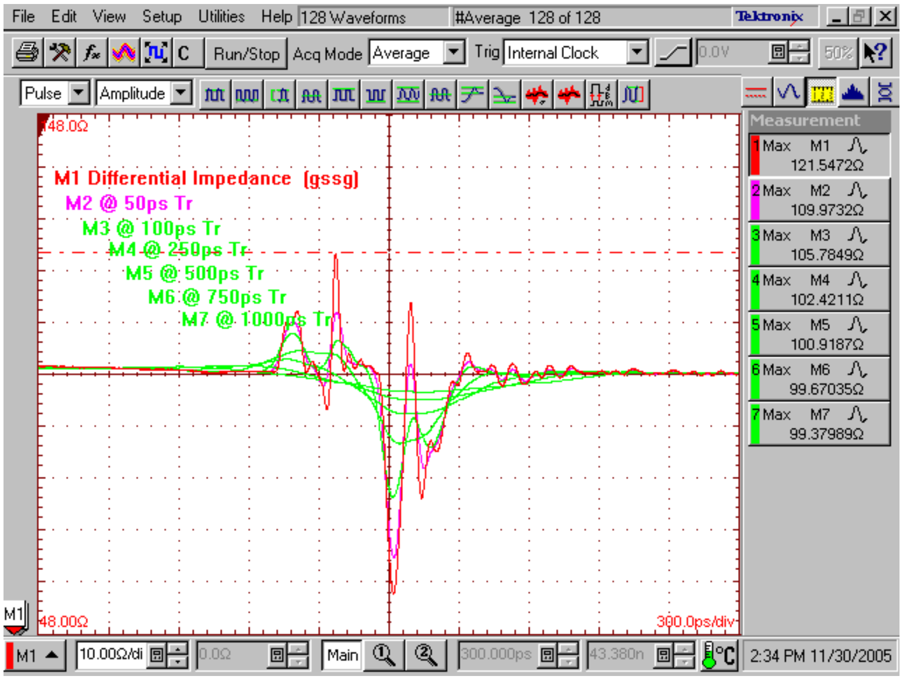
Measurement
1 Ampl M1
497.8102mV
2 Rise M1
30.45167ps

M1 100.0mV/ 0.0V 200.000ps 43.980n

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Differential Application – Impedance

Configuration: (DP1: Source = SOLC J21-J24)



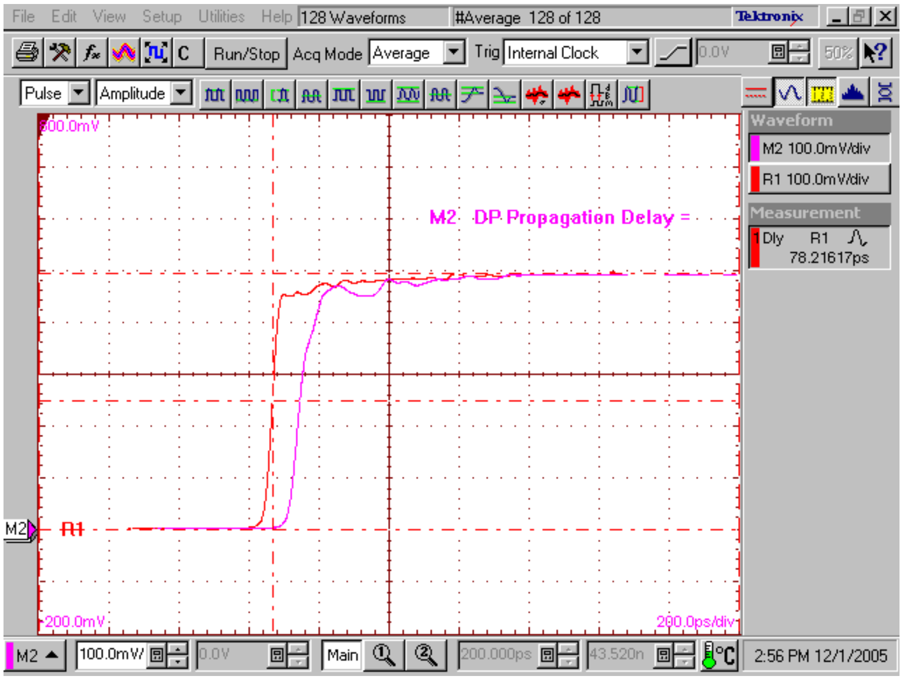
Acq Mode: Average
Trig: Internal Clock

1 Max M1 121.5472Ω
2 Max M2 109.9732Ω
3 Max M3 105.7849Ω
4 Max M4 102.4211Ω
5 Max M5 100.9187Ω
6 Max M6 99.67035Ω
7 Max M7 99.37989Ω

M1 10.00Ω/di 0.0Ω
2:34 PM 11/30/2005

Differential Application – Propagation Delay

Configuration: (SE2: Source = SOLC J14-J17)



Acq Mode: Average
Trig: Internal Clock

M2 100.0mV/div
R1 100.0mV/div

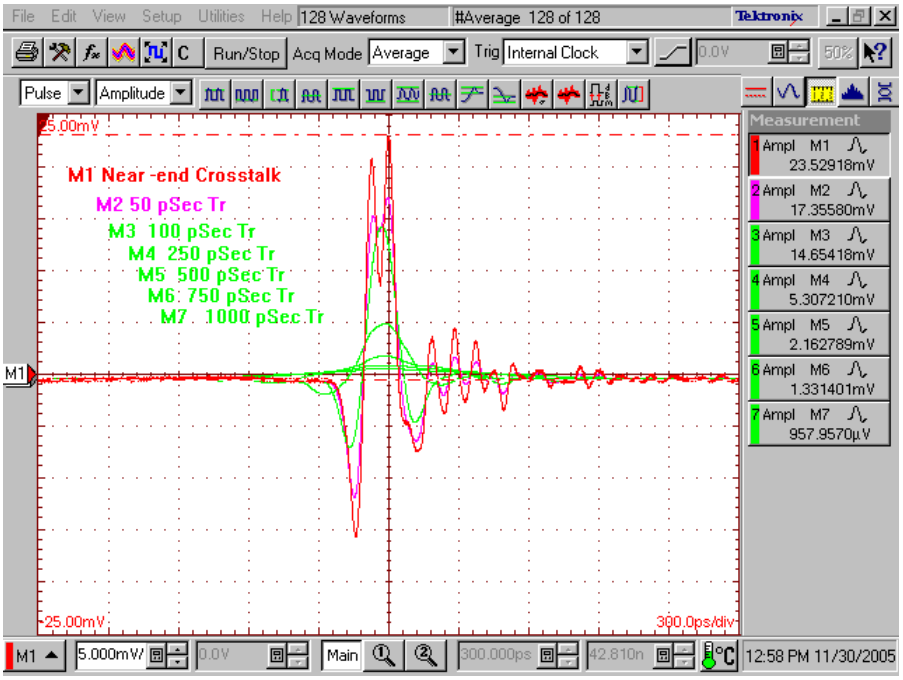
1 Dly R1 78.21617ps

M2 100.0mV/ 0.0V
2:56 PM 12/1/2005

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Differential Application – NEXT

Configuration: (DP2: Source = SOLC J34-J28; Victim = SOLC J33-J27)

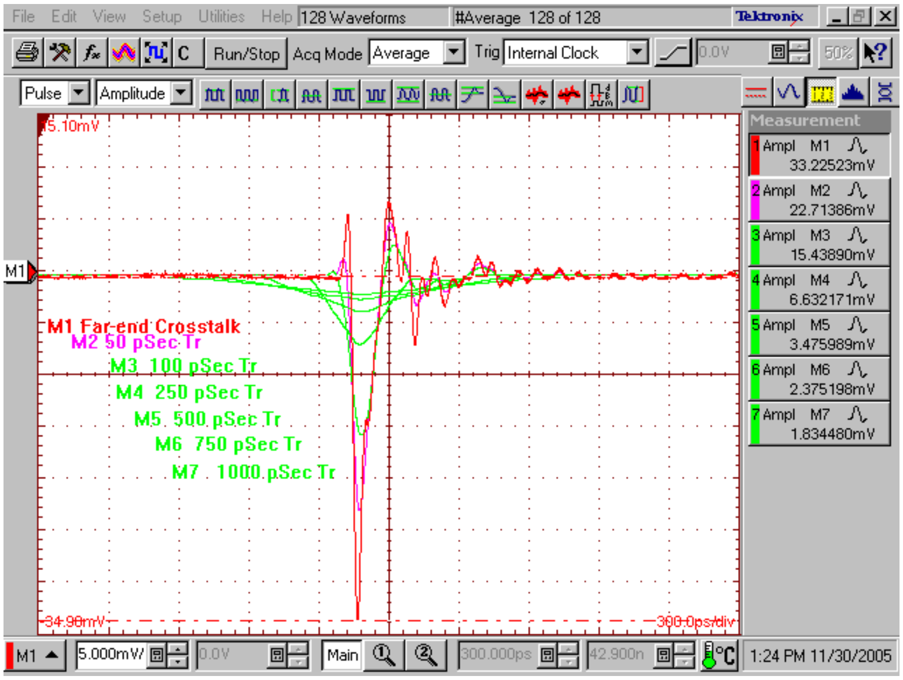


1 Ampl M1 23.52918mV
2 Ampl M2 17.35580mV
3 Ampl M3 14.65418mV
4 Ampl M4 5.307210mV
5 Ampl M5 2.162789mV
6 Ampl M6 1.331401mV
7 Ampl M7 957.9570µV

12:58 PM 11/30/2005

Differential Application – FEXT

Configuration: (DP2: Source = SOLC J34-J28; Victim = TOLC J53-J55)



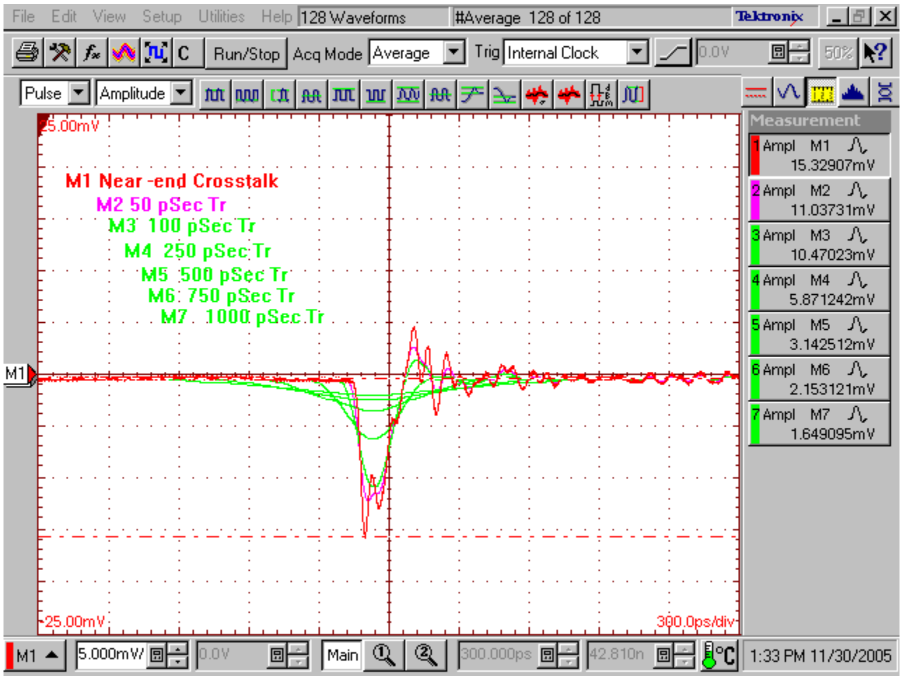
1 Ampl M1 33.22523mV
2 Ampl M2 22.71386mV
3 Ampl M3 15.43890mV
4 Ampl M4 6.632171mV
5 Ampl M5 3.475989mV
6 Ampl M6 2.375198mV
7 Ampl M7 1.834480mV

1:24 PM 11/30/2005

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Differential Application – NEXT

Configuration: (DP2: Source = SOLC J34-J28; Victim = SOLC J30-J32)



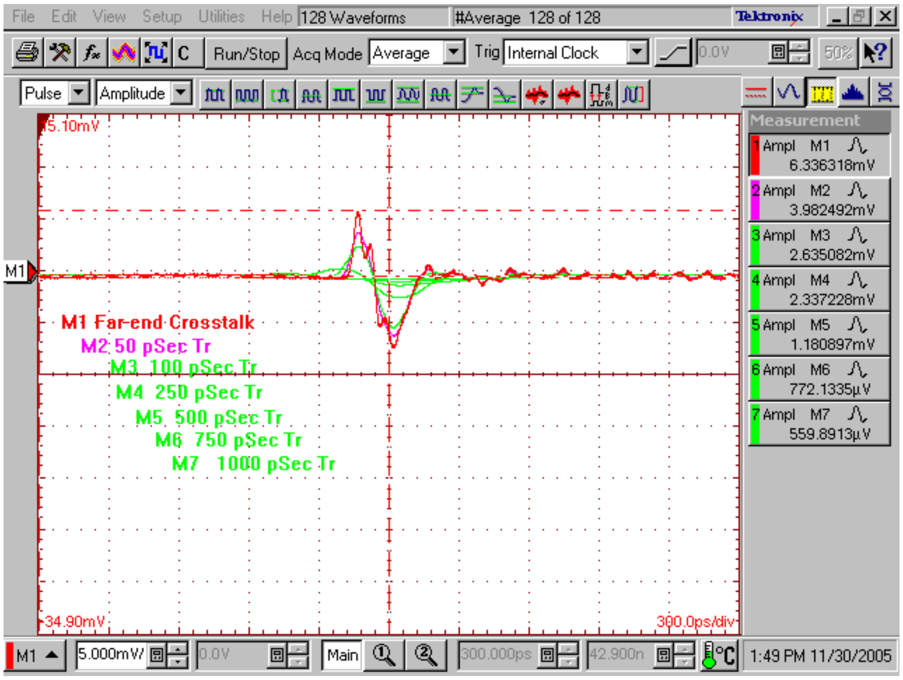
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V

1 Ampl M1 15.32907mV
2 Ampl M2 11.03731mV
3 Ampl M3 10.47023mV
4 Ampl M4 5.871242mV
5 Ampl M5 3.142512mV
6 Ampl M6 2.153121mV
7 Ampl M7 1.649095mV

M1 5.000mV/ 0.0V
300.000ps 42.810n
1:33 PM 11/30/2005

Differential Application – FEXT

Configuration: (DP2: Source = SOLC J34-J28; Victim = TOLC J58-J60)



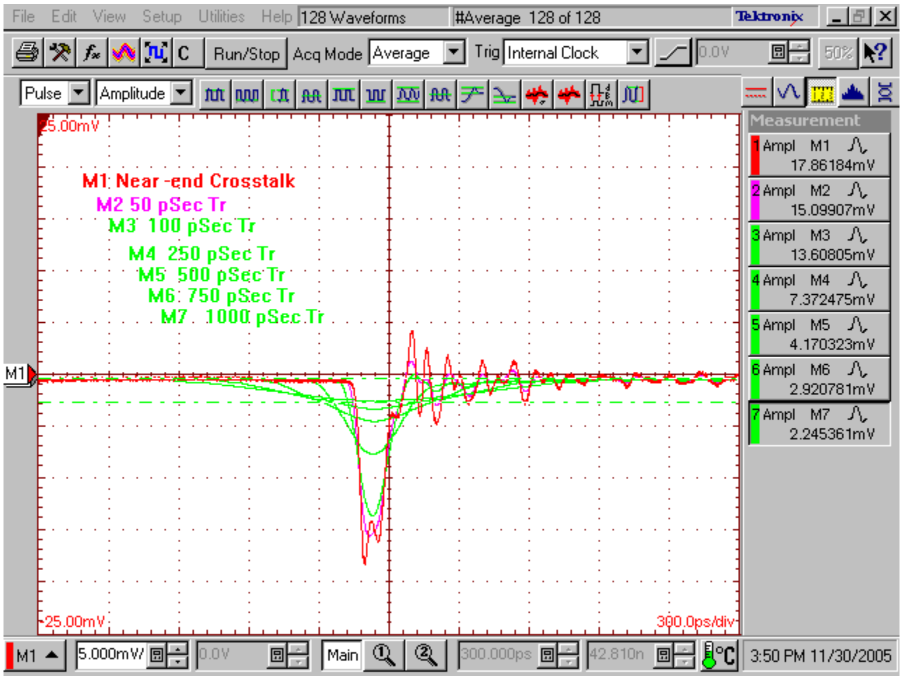
128 Waveforms
#Average 128 of 128
Acq Mode Average
Trig Internal Clock
0.0V

1 Ampl M1 6.336318mV
2 Ampl M2 3.982492mV
3 Ampl M3 2.635082mV
4 Ampl M4 2.337228mV
5 Ampl M5 1.180897mV
6 Ampl M6 772.1335µV
7 Ampl M7 559.8913µV

M1 5.000mV/ 0.0V
300.000ps 42.900n
1:49 PM 11/30/2005

Differential Application – NEXT

Configuration: (DP1: Source = SOLC J21-J24; Victim = SOLC J25-J26)



1 Ampl M1 17.86184mV
2 Ampl M2 15.09907mV
3 Ampl M3 13.60805mV
4 Ampl M4 7.372475mV
5 Ampl M5 4.170323mV
6 Ampl M6 2.920781mV
7 Ampl M7 2.245361mV

Differential Application – FEXT

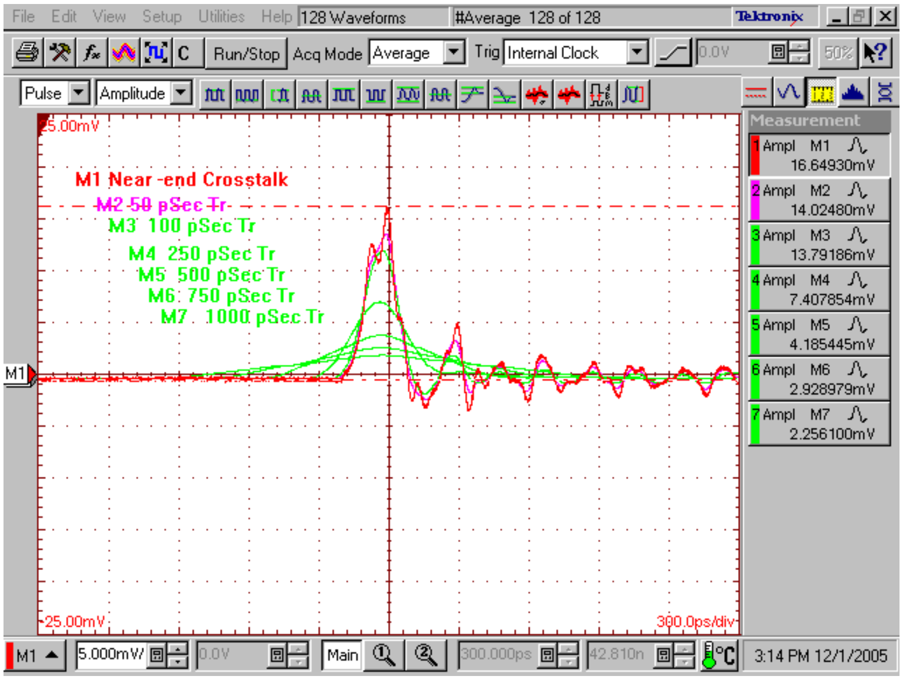
Configuration: (DP1: Source = SOLC J21-J24; Victim = TOLC J51-J52)

1 Ampl M1 5.576668mV
2 Ampl M2 3.222961mV
3 Ampl M3 2.127069mV
4 Ampl M4 1.851777mV
5 Ampl M5 912.5865µV
6 Ampl M6 593.3357µV
7 Ampl M7 428.2474µV

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Differential Application – NEXT

Configuration: (SE2: Source = SOLC J14-J17; Victim = SOLC J13-J16)

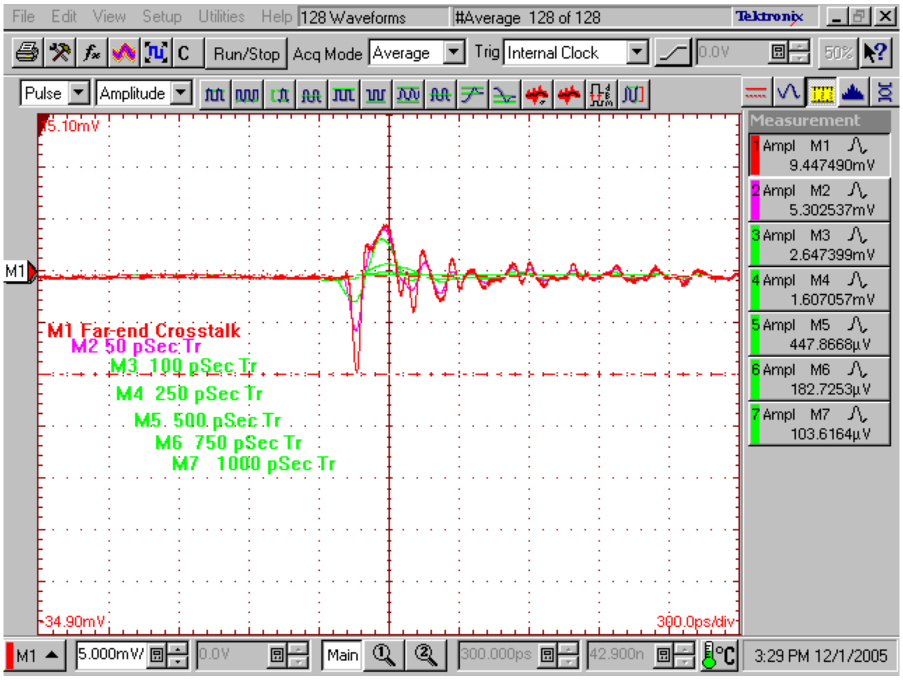


1 Ampl M1 16.64930mV
2 Ampl M2 14.02480mV
3 Ampl M3 13.79186mV
4 Ampl M4 7.407854mV
5 Ampl M5 4.185445mV
6 Ampl M6 2.928979mV
7 Ampl M7 2.256100mV

3:14 PM 12/1/2005

Differential Application – FEXT

Configuration: (SE2: Source = SOLC J14-J17; Victim = TOLC J41-J43)



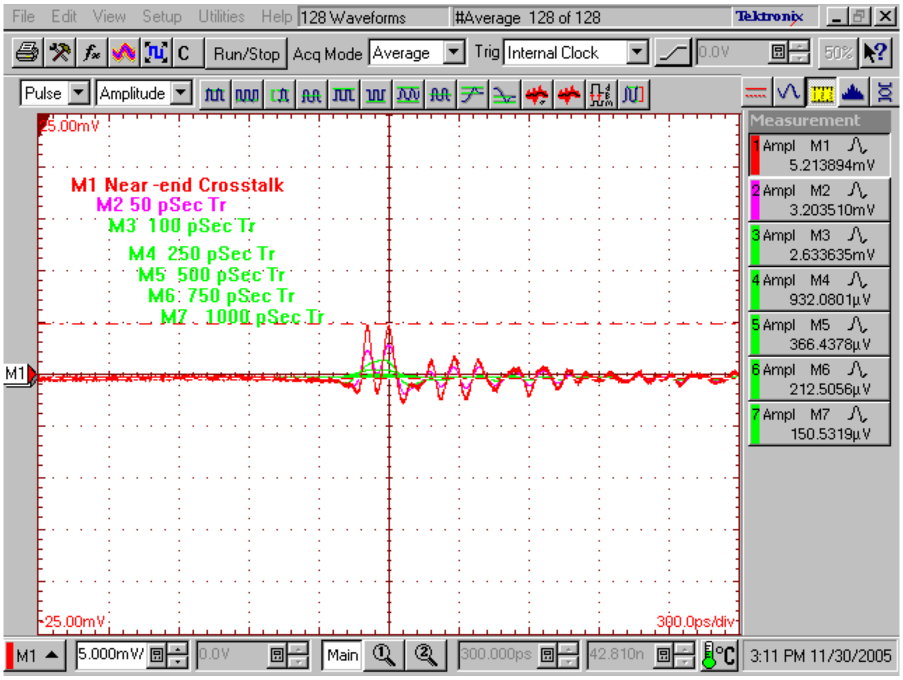
1 Ampl M1 9.447490mV
2 Ampl M2 5.302537mV
3 Ampl M3 2.647399mV
4 Ampl M4 1.607057mV
5 Ampl M5 447.8668µV
6 Ampl M6 182.7253µV
7 Ampl M7 103.6164µV

3:29 PM 12/1/2005

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Differential Application – NEXT

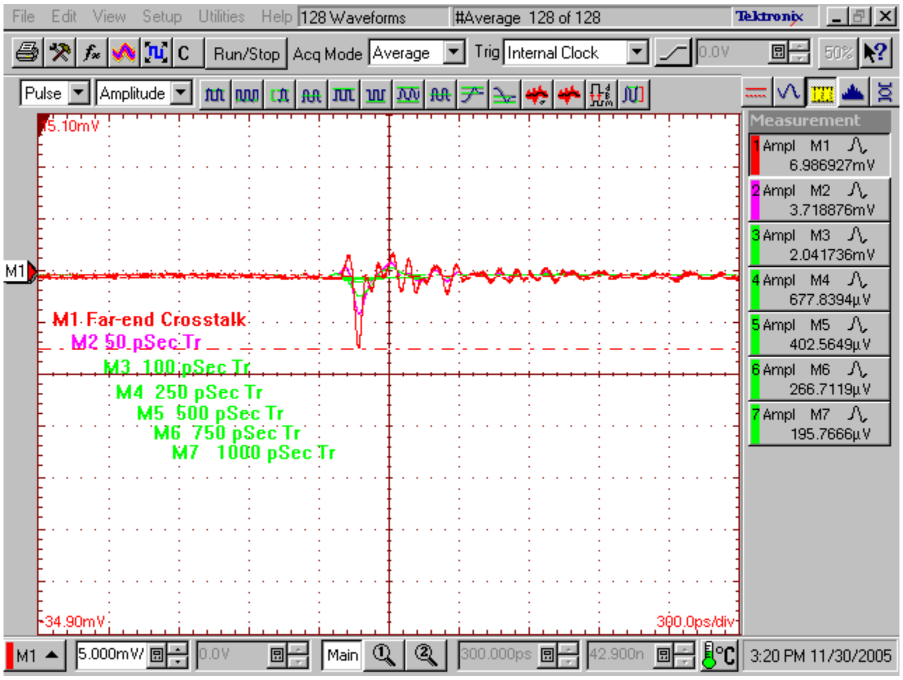
Configuration: (DP1: Source = SOLC J21-J24; Victim = SOLC J20-J23)



Measurement
1 Ampl M1 5.213894mV
2 Ampl M2 3.203510mV
3 Ampl M3 2.633635mV
4 Ampl M4 932.0801µV
5 Ampl M5 366.4378µV
6 Ampl M6 212.5056µV
7 Ampl M7 150.5319µV

Differential Application – FEXT

Configuration: (DP1: Source = SOLC J21-J24; Victim = TOLC J47-J49)



Measurement
1 Ampl M1 6.986927mV
2 Ampl M2 3.718876mV
3 Ampl M3 2.041736mV
4 Ampl M4 677.8394µV
5 Ampl M5 402.5649µV
6 Ampl M6 266.7119µV
7 Ampl M7 195.7666µV

Appendix C – Product and Test System Descriptions

Product Description

Product samples are a staggered quad row connector system. The SOLC socket and TOLC terminal mating system is described by P/N SOLC-110-02-S-Q-LC and P/N TOLC-110-32-S-Q-LC respectively. When mated a board-to-board stack height of 12mm (0.472”) exists between boards. Connector structures consist of 4 rows of 10 contact positions mounted into a plastic housing in a surface mount design. Staggered mating contacts are on a 1.27mm center (.050”) pitch. Surface mount terminals lay 20 to a row on a 0.64mm (.025”) pitch.

Test System Description

The test fixtures are composed of a 4-layer FR-4 material with 50Ω and100Ω signal traces launched from a board mount vertical RF SMA(f) coaxial connector used for the electrical characterization of Samtec hi-speed connector products. The pictured fixtures are specific to the SOLC/TOLC series connector and are identified by Samtec P/N PCB-100364-TST-01 and P/N PCB-100364-TST-02 (Figure 1)

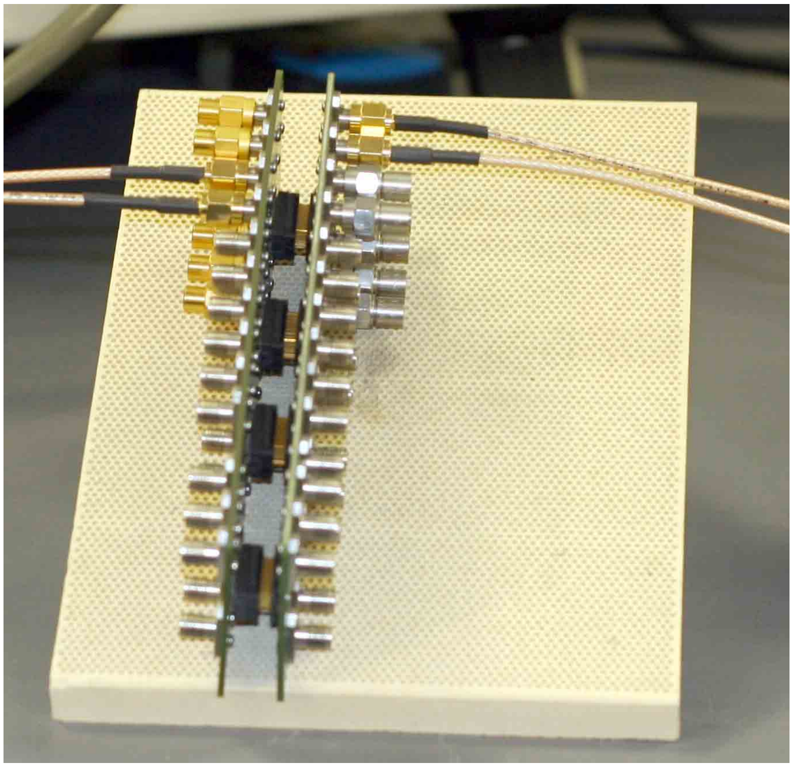
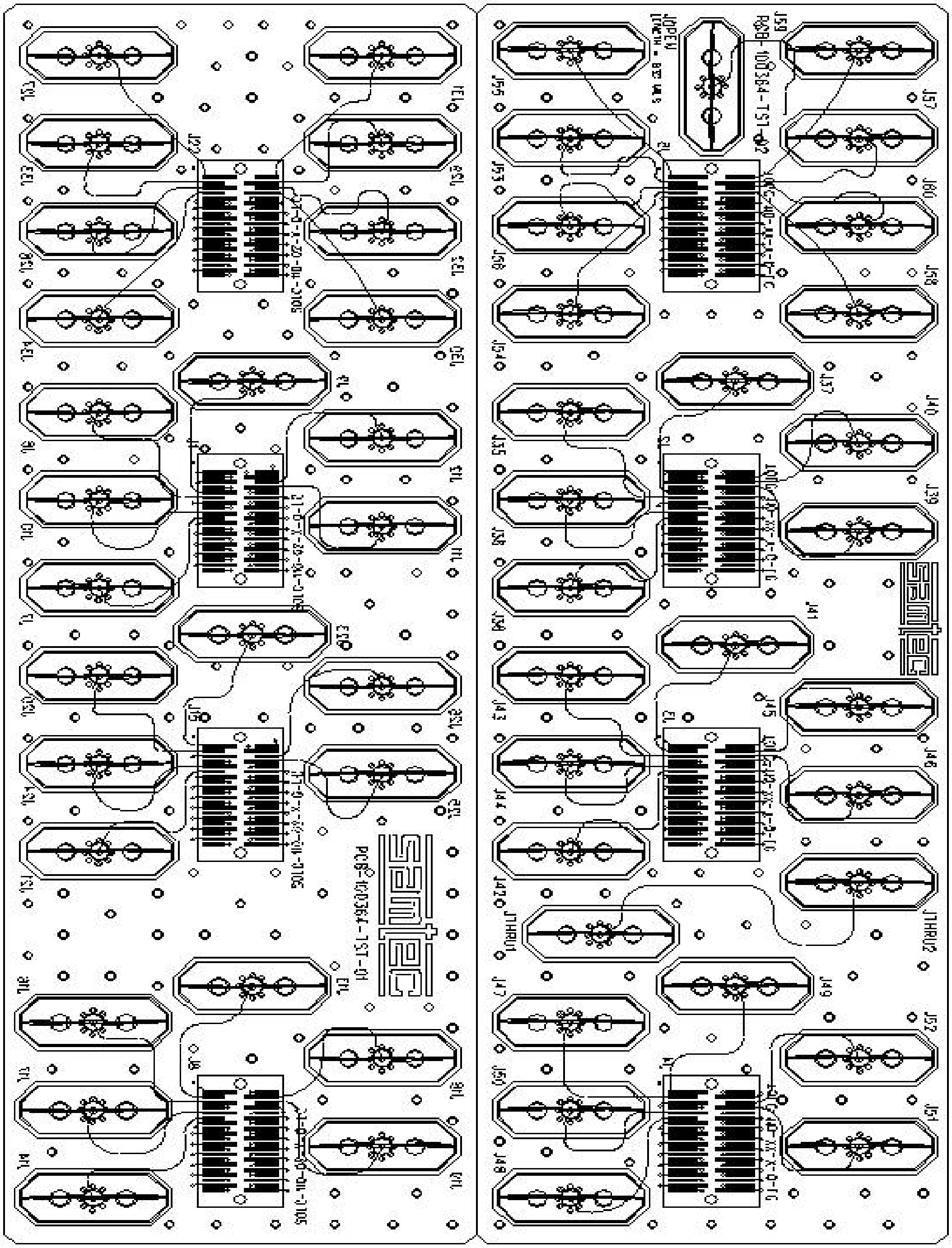


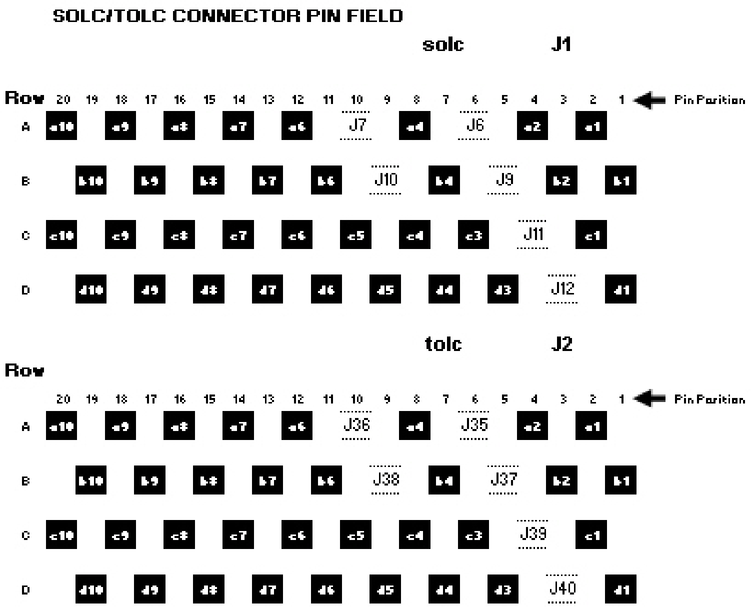
Figure 1 Mated PCB Test Fixtures with Mounted Test Connectors

Signal Launch and Monitoring Map



Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

SOLC, J1 / TOLC, J2 Connector/Footprint Pinout Map (SE1)



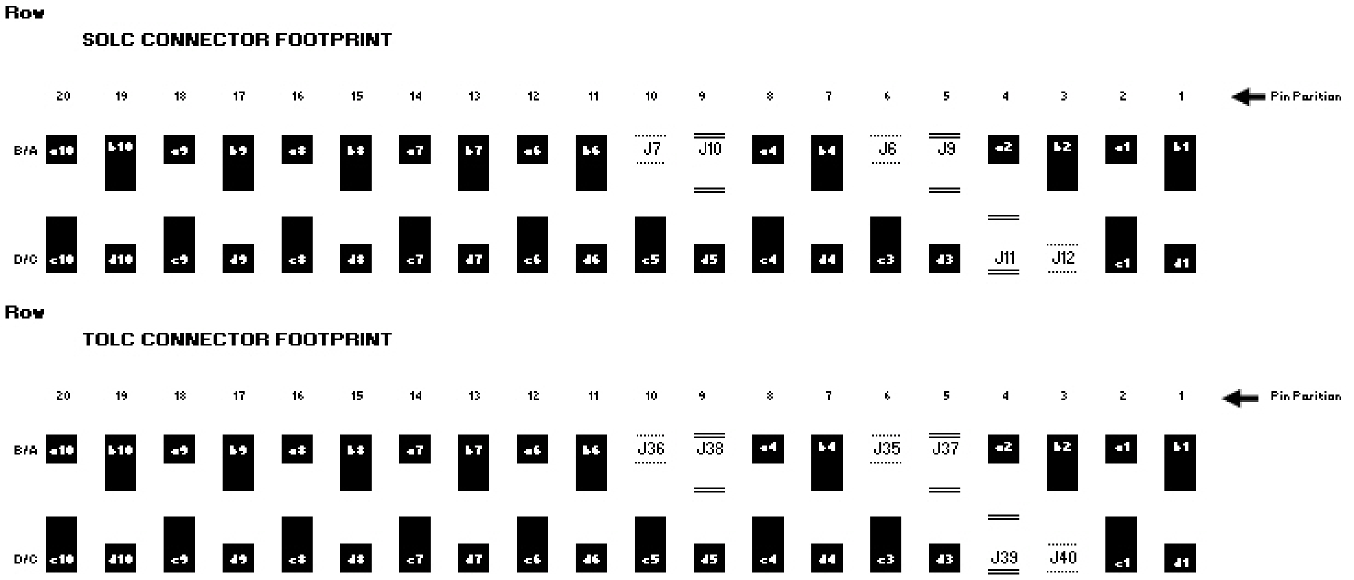
Pin Identifier

a# = PCB Ground Connector /Footprint Position
Row (A #) = Aggressor, SW+, Connector /Footprint Position
Row (b #) = Aggressor, SW -, Connector /Footprint Position
V # = Victim Line Connector /Footprint Position

Pin Field Position Characterization

SE Impedance (solc,J1/ tolc,J2) : A6-A6 = J6-J35
SE Impedance (solc,J1/ tolc,J2) : B5-B5 = J9-J37
SE IL & RL (solc,J1/ tolc,J2) : A6-A6 = J6-J35
SE IL & RL (solc,J1/ tolc,J2) : B5-B5 = J9-J37
SE NEXT: (solc,J1) A6 = J6 - (solc,J1) V10 = J7
SE FEXT: (solc,J1) A6 = J6 - (tolc,J2) V10 = J36
SE NEXT: (solc,J1) A6 = J6 - (solc,J1) V5 = J9
SE FEXT: (solc,J1) A6 = J6 - (tolc,J2) V5 = J37
SE NEXT: (solc,J1) B5 = J9 - (solc,J1) V4 = J11
SE FEXT: (solc,J1) B5 = J9 - (tolc,j2) V4= J39

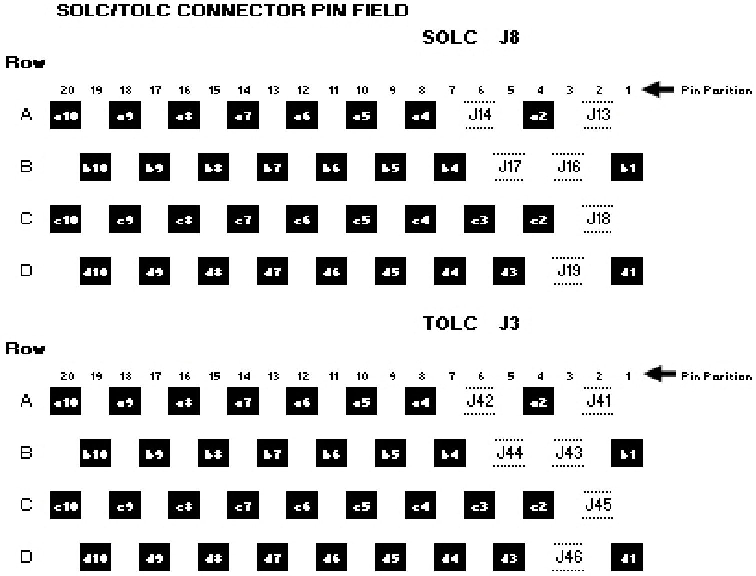
DIFF. NEXT: (solc,J1) A6b5 = J6:J9 - (solc,J1) V4V3 = J11:J12
DIFF. FEXT: (solc,J1) A6b5 = J6:J9 - (tolc,J2) V4V3 = J39:J40



Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

SOLC, J8 / TOLC, J3 Connector/Footprint Pinout Map (SE2)

Fixture Description: Mate single SOLC connector J8 to J3 on multiple TOLC connector PCB-100364-TST-02


SOLC/TOLC CONNECTOR PIN FIELD

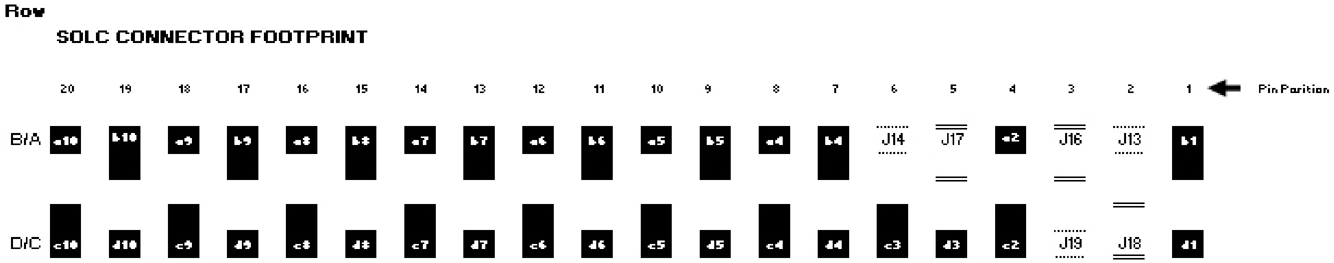
Pin Identifier

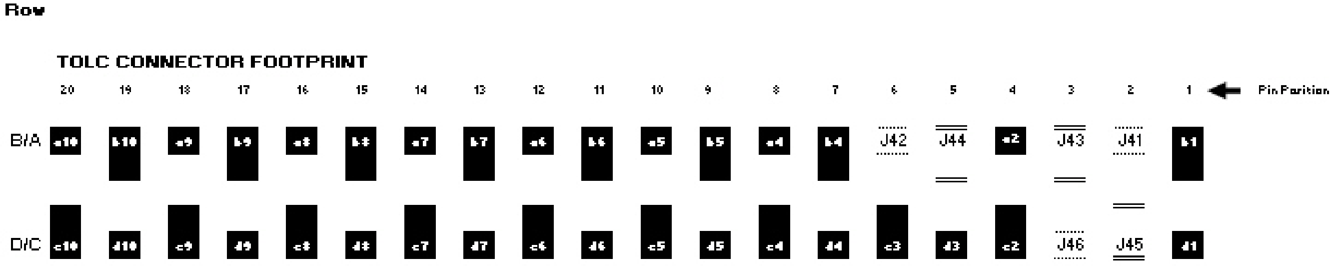
a# = PCB Ground Connector /Footprint Position
Row (A #) = Aggressor, SW+, Connector /Footprint Position
Row (b #) = Aggressor, SW -, Connector /Footprint Position
V # = Victim Line Connector /Footprint Position

Pin Field Position Characterization

SE Impedance (solc,J8 / tolc,J3) : A2-A2 = J13-J41
SE Impedance (solc,J8 / tolc,J3) : A6-A6 = J14-J42
SE NEXT: (solc,J8) B3 = J16 - (solc,J8) V5 = J17
SE FEXT: (solc,J8) B3 = J16 - (solc,J3) V5 = J44

DIFF. Impedance (solc,J8 / tolc,J3) : A3b5 = J16:J17
DIFF. NEXT: (solc,J8) A6b5 = J14:J17 - (solc,J8) V2V3 = J13:J16
DIFF. FEXT: (solc,J8) A6b5 = J14:J17 - (tolc,J3) V4V3 = J41:J43

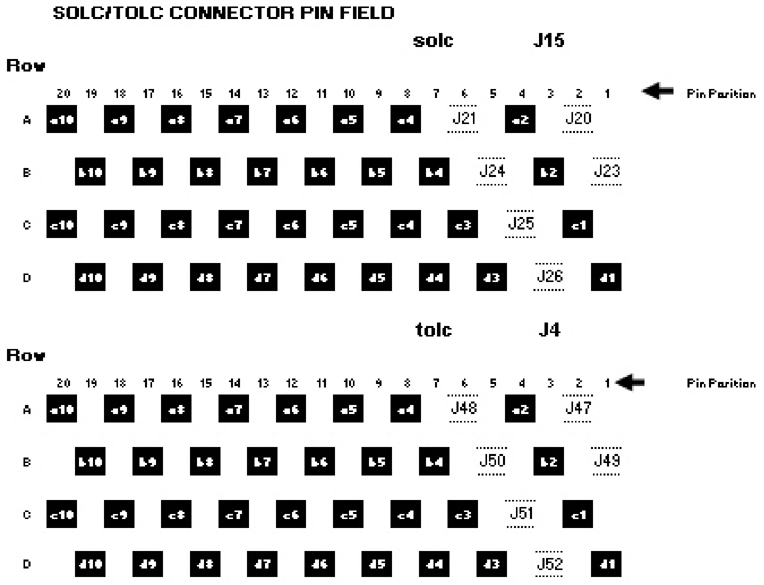

SOLC CONNECTOR FOOTPRINT


TOLC CONNECTOR FOOTPRINT

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

SOLC, J15 / TOLC, J4 Connector/Footprint Pinout Map (DP1)

Fixture Description: Mate single SOLC connector J15 to J4 on multiple TOLC connector PCB-100364-TST-02

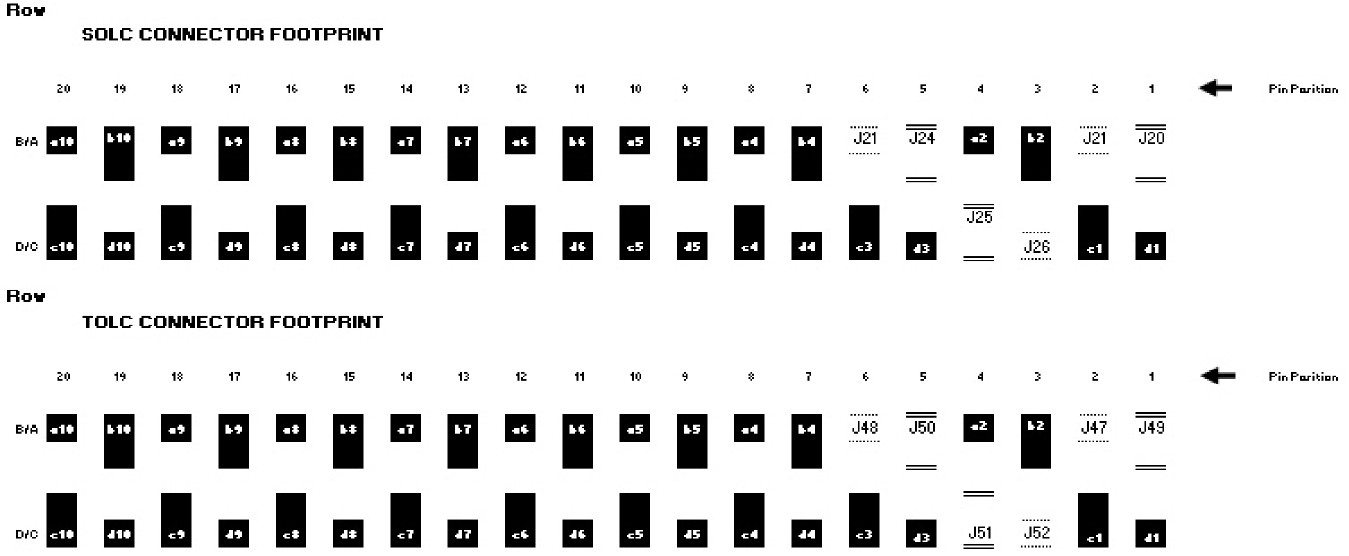


Pin Identifier

a# = PCB Ground Connector /Footprint Position
Row (A #) = Aggressor, SW+, Connector /Footprint Position
Row (b #) = Aggressor, SW -, Connector /Footprint Position
V # = Victim Line Connector /Footprint Position

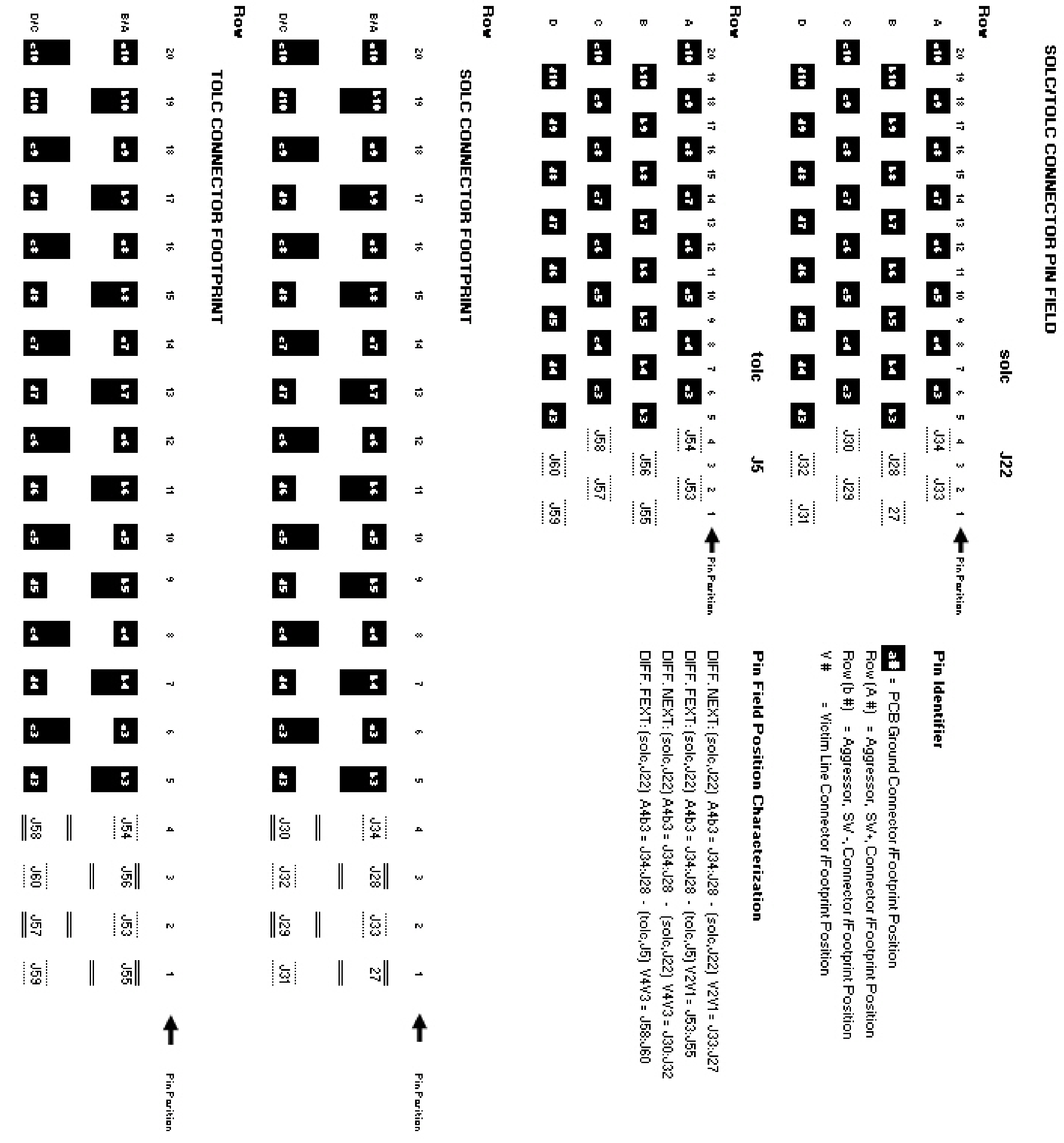
Pin Field Position Characterization

DIFF. IL & RL (solc,J15 - tolc,J4) : A6b5 = J21:J24
DIFF. Impedance (solc,J15 - tolc,J4) : A6b5 = J21:J24
DIFF. Impedance (solc,J15 - tolc,J4) : A2b1 = J20:J23
DIFF. NEXT: (solc,J15) A6b5 = J21:J24 - (solc,J15) V2V1 = J20:J23
DIFF. FEXT: (solc,J15) A6b5 = J21:J24 - (tolc,J4) V2V1 = J47:J49
DIFF. NEXT: (solc,J15) A6b5 = J21:J24 - (solc,J15) V4V3 = J25:J26
DIFF. FEXT: (solc,J15) A6b5 = J21:J24 - (tolc,J4) V4V3 = J51:J52



Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

SOLC, J22 / TOLC, J5 Connector/Footprint Pinout Map (DP2)



Pin Identifier

a# = PCB Ground Connector /Footprint Position
Row (A #) = Aggressor, SW+, Connector /Footprint Position
Row (b #) = Aggressor, SW-, Connector /Footprint Position
V # = Victim Line Connector /Footprint Position

Pin Field Position Characterization

DIFF. NEXT: (solc,J22) A4b3 = J34,J28 - (solc,J22) V2V1 = J33,J27
DIFF. FEXT: (solc,J22) A4b3 = J34,J28 - (tolc,J5) V2V1 = J53,J55
DIFF. NEXT: (solc,J22) A4b3 = J34,J28 - (solc,J22) V4V3 = J30,J32
DIFF. FEXT: (solc,J22) A4b3 = J34,J28 - (tolc,J5) V4V3 = J58,J60

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Appendix D – Test and Measurement Setup

Test instrument is the Tektronix CSA8000 Communication Signal Analyzer Mainframe. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. For this series of tests, four of the eight TDR/Sampling Head capability is used *(Figure 2)*. Scattering parameters presented in this report are generated by TDA Systems IConnect. IConnect is a TDR based measurement software tool used in generating frequency domain related responses from high speed interconnects.

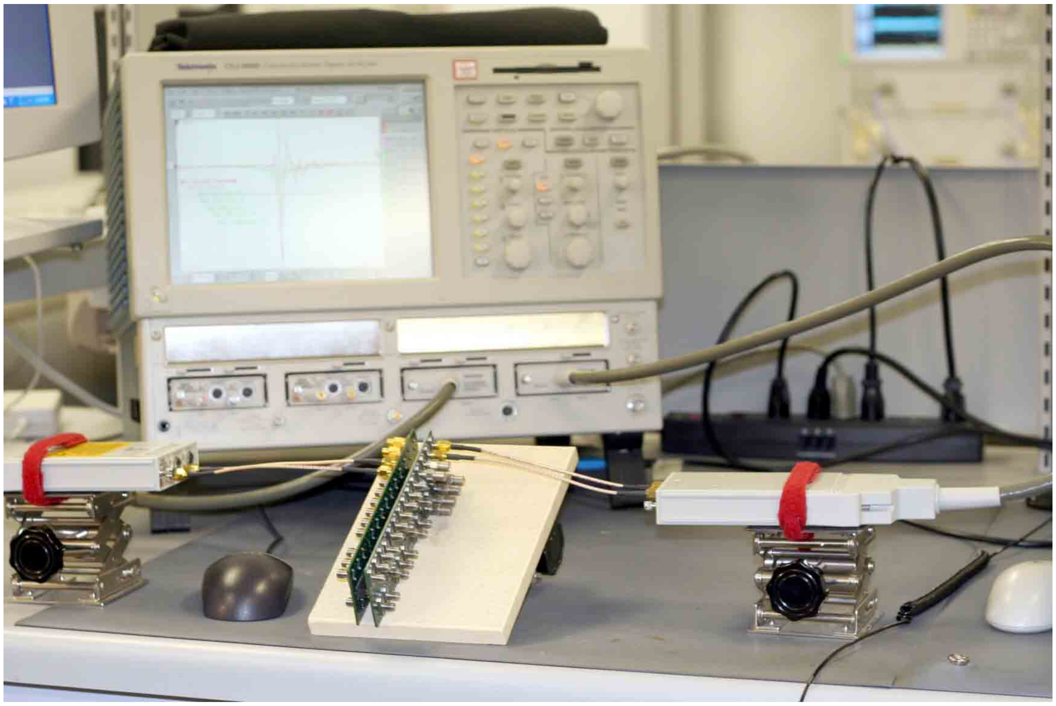


Figure 2 Measurement Setup

Test Instruments & Accessories

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
3	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
4	6 inch RG316 Cable Assemblies (6 GHz)
10	Pasternack SMA 50 Ω Terminations (12 GHz)

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

Test Setup Configurations

The schematics below indicate the Single Ended signal configurations setup for each of the parameters characterized. To setup for differential signal parameters duplicate on the second line the same SE configuration for the parameter of interest.

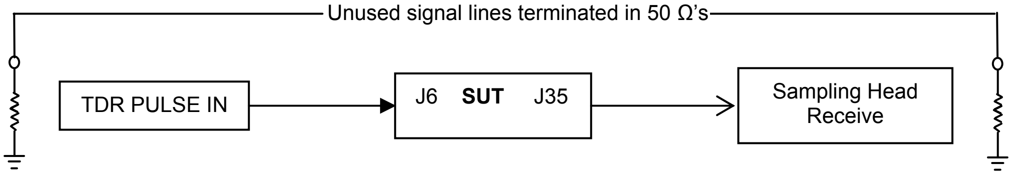


Figure 3 - Insertion Loss, Impedance, Propagation Delay

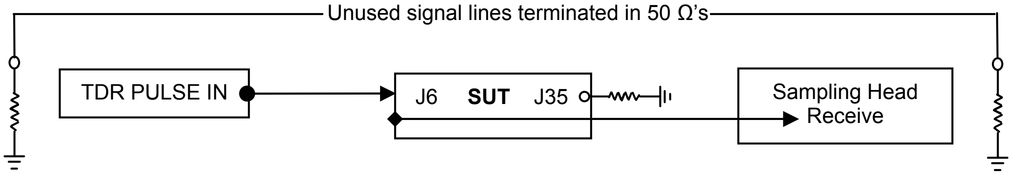


Figure 4 - Return Loss, Impedance

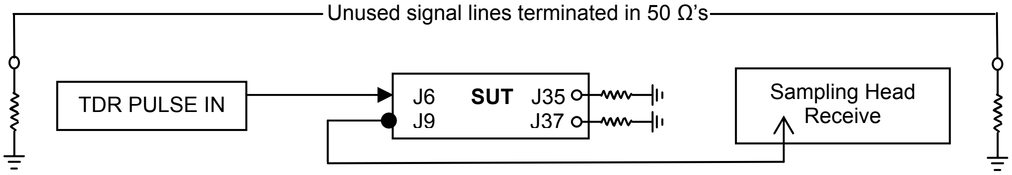


Figure 5 - Near End Crosstalk

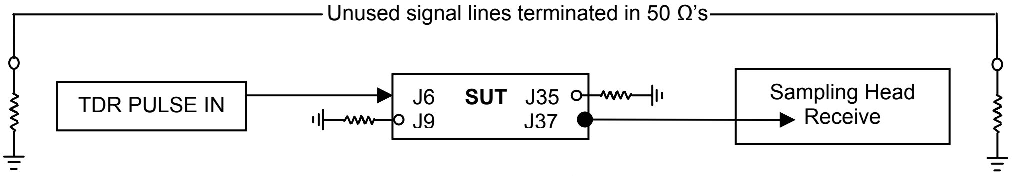


Figure 6 - Far End Crosstalk

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Related time and frequency test parameter data recorded for this report were gathered simultaneously.

Frequency (S-Parameter) Domain Procedures

Frequency data extraction involves two steps that first measure the frequency related time domain waveform followed by post-processing of the time domain waveforms into loss and crosstalk response parameters versus frequency. The first step utilizes the Tektronix CSA8000 time based instrument to capture frequency related single-ended or differential signal types propagating through an appropriately prepared SUT. The second step involves a correlation of the time based waveforms using the TDA Systems IConnect software tool to post-process these waveforms into frequency response parameters. TDA Systems labels these frequency related waveform relationships as the *Step* and *DUT* reference. This report establishes the setup procedures for defining the *Step* and *DUT* reference for frequency parameters of interest. Once established, the *Step* and *DUT* references are post-processed in IConnect's S-parameter computations window.

CSA8000 Setup

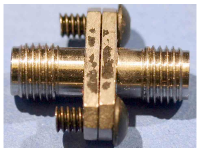
Listed below are the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. These frequency boundaries are determined by a time domain instruments functional settings such as window length, number of points and averaging capability. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process.

Series: TOLC/SOLC, 1.27mm (0.050”) Contact Pitch, 0.64mm (0.025”) Footprint Pitch
Description:, Board-to-Board, Surface Mount, 12mm (0..472”) Stack Height

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss

SUT Preparation (figure 3) –The signal path for single ended transmission measurements was characterized using connector/pcb fixture SOLC, J1 / TOLC, J2 (ie. J6, J35). The differential transmission path measured is located on connector/pcb fixture SOLC, J15 / TOLC (ie. J21-J24, J48-J50). Terminate all unused transmission paths in the connector/pcb fixture bank using 50Ω high frequency (HF) terminations. Reference correct connector/footprint pinout map for insertion loss configuration detail.

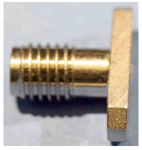


Step Reference - Establish waveform by making a TDT transmission measurement that includes all cables, adapters, and/or probes connected in the test systems transmission path. Complete the transmission path by inserting a piggybacked SMA coaxial launch connector *(pictured on right).* Insert 2 piggybacked SMA launches for differential measurements.

DUT Reference - Establish waveform by making an active TDT transmission measurement that includes all cables, adapters, and/or probes connected in the test systems transmission path. Insert the SUT between the test cables and record measurement.

Return Loss

SUT Preparation (figure 4) – Measure the same signal paths used for the insertion loss characterizations. Terminate the excited paths at the far-end of the connector/pcb fixture. Terminate all unused transmission paths within the connector/pcb fixture bank in 50Ω’s with HF terminations *(Reference Signal Launch and Monitoring Map)*.



Step Reference - Establish waveform by making an active TDR reflection measurement that includes all cables, adapters, and/or probes connected in the test systems electrical path up to and including the open standard. *Use un-terminated SMA (J) coaxial launches for single end and differential open standards. (**Note:** (see picture at right).*

DUT Reference - Establish waveform by making a TDR (matched) reflection measurement that includes all cables, adapters, and/or probes connected in the test systems signal path. A portion of the energy passing through the DUT is absorbed by the HF terminations and portion of the signal is reflected. The portions absorbed form a flat 50Ω single-ended or 100Ω differential impedance waveform response following the reflected response through the DUT.

Near-End Crosstalk (NEXT*)*

SUT Preparation (figure 5) – Four single-ended near end crosstalk configurations were monitored using connector/pcb fixtures SOLC, J1 / TOLC, J2 and SOLC, J8 /TOLC, J3. Five differential near-end crosstalk configurations were monitored using all four fixture convections. They were SOLC, J1/TOLC, J2, SOLC, J8 /TOLC, J3, SOLC, J15 /TOLC, J4 and SOLC, J22 / TOLC, J5. Terminate far end aggressor and victim lines using 50 Ω high frequency (HF) terminations. Also terminate all the unused transmission paths within the connector/pcb fixture bank. Reference connector/footprint pinout map for crosstalk configuration detail.

Step Reference - Establish waveform by making a TDR open measurement that includes all cables, adapters, and/or probes connected in the test systems electrical path up to and including an open standard. *(**Note:** The same step reference waveform generated for return loss is used in conjunction with the FEXT waveforms to post-process crosstalk s-parameters in IConnect . If testing equipment or the DUT is subject to a constant change in environmental conditions, it is recommended a new step reference be generated. Use the* Return Loss *Step Reference procedure.*

DUT Reference - Establish waveform by driving an aggressor signal line (i.e.; J6) and recording the TDR coupled energy at the adjacent near-end victim line (i.e.; J9). Repeat measurement procedures to establish the waveforms for the remaining single-ended and differential configurations. Reference correct connector/ footprint pinout map for crosstalk configuration detail.

Far-End Crosstalk (FEXT)

SUT Preparation (figure 6) - Four single-ended far end crosstalk configurations were monitored using connector/pcb fixtures SOLC, J1 / TOLC, J2 and SOLC, J8 /TOLC, J3. Five differential far end crosstalk configurations were monitored using all four fixture convections. They were SOLC, J1/TOLC, J2, SOLC, J8 /TOLC, J3, SOLC, J15 /TOLC, J4 and SOLC, J22 / TOLC, J5. Reference connector footprint pinout maps for crosstalk configuration details. Terminate the near end victim line and the aggressor line on the far end using 50 Ω high frequency (HF) terminations. Also terminate all unused transmission paths within the connector/pcb fixture bank.

Step Reference - Establish waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Complete the transmission path by inserting a piggybacked SMA coaxial launch connector. Insert 2 SMA launches for differential measurements. *(**Note:** The same step reference waveform generated for insertion loss is used in conjunction with the FEXT waveforms to post-process crosstalk s-parameters in IConnect . If testing equipment or the DUT is subject to a constant change in environmental conditions, it is recommended a new step reference be generated. Use the Insertion Loss Step Reference procedure.*

DUT Reference - Establish waveform by driving an aggressor signal line (i.e.; J6) and recording the TDR coupled energy at the adjacent far-end victim line (i.e.; J37). Repeat measurement procedures to establish the waveforms for the remaining single-ended and differential configurations. Reference correct connector/footprint pinout map for crosstalk configuration detail

Time Domain Procedures

Measurements involving digital type pulses are performed utilizing either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. For this series of tests, TDR methods are employed for the impedance and propagation delay measurements. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to accurately and fully characterize the SUT.

Impedance

The signal line(s) of the SUT’s signal configuration is energized with a TDR pulse. The far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω terminations). Terminating the adjacent signal lines in the test systems characteristic impedance limits unwanted changes to the impedance response. (Figure 3).

Propagation Delay

This connector series uses the fastest edge rate (30ps) of the TDR impedance waveform to measure propagation delay. . Differential or single ended signal delay is the measured difference of propagation between the known signal trace delay and the delay of a mated SUT. The measurement is a one-way propagation result. Termination of the adjacent signal lines into the test systems characteristic impedance eliminate alternate current paths providing for better measurement accuracy (Figure 3). Reference PCB100364-TST-02 boards for PD reference trace delay lines).

Crosstalk

An active pulsed waveform is transmitted through a selected SUT signal line. The adjacent quiet signal lines are monitored for the coupled energy at the near-end and far-end. Active and quiet lines not being monitored are terminated in the test systems characteristic impedance. Signal lines adjacent to the quiet lines remain terminated on both ends throughout the test sequence. Failing to terminate the active near or far end, quiet lines, or in some cases, signal lines adjacent to the quiet line may have an effect on amplitude and shape of the coupled energy (Figures 5 & 6).

Appendix F – Glossary of Terms

BC – Best Case crosstalk configuration

DP – Differential Pair signal configuration

DUT – Device under test; TDA IConnect reference waveform

FEXT – Far-End Crosstalk

GSG – Ground–Signal-Ground; geometric configuration

NEXT – Near-End Crosstalk

PCB – Printed Circuit Board

SE – Single-Ended

SI – Signal Integrity

SUT – System under test

TDR – Time Domain Reflectometry

TDT – Time Domain Transmission

WC – Worse Case crosstalk configuration

Xrow^{se} – Cross ground/ power bar crosstalk, single-ended signal

Xrow^{diff} – Cross ground/ power bar crosstalk, differential signal

Z – Impedance (expressed in ohms)

Static (S) **=** adjacent contact position does not exist, generally the end positions of the connector pin field