

Series: FTE/CLE

Description: Surface Mount, 0.8mm (.0315") Pitch, 5mm (0.197") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω)							
Signal Risetime	35±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	56.3	53.0	52.8	51.7	50.8	50.6	50.5
Minimum Impedance	41.4	46.1	47.6	48.9	49.2	49.2	49.3

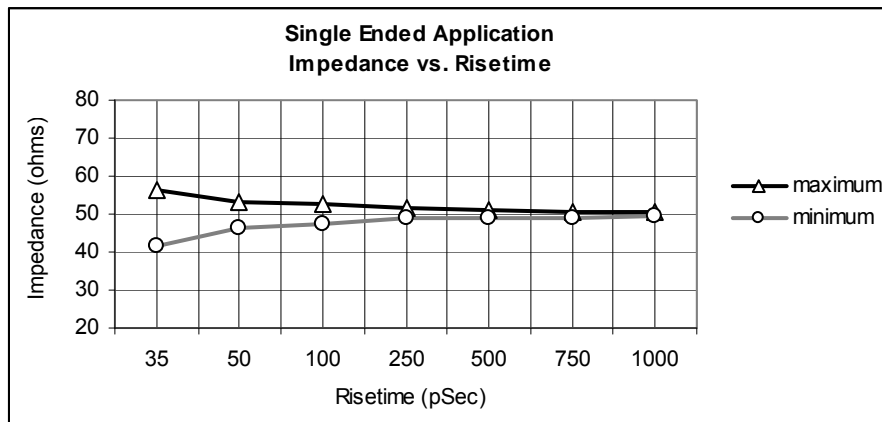
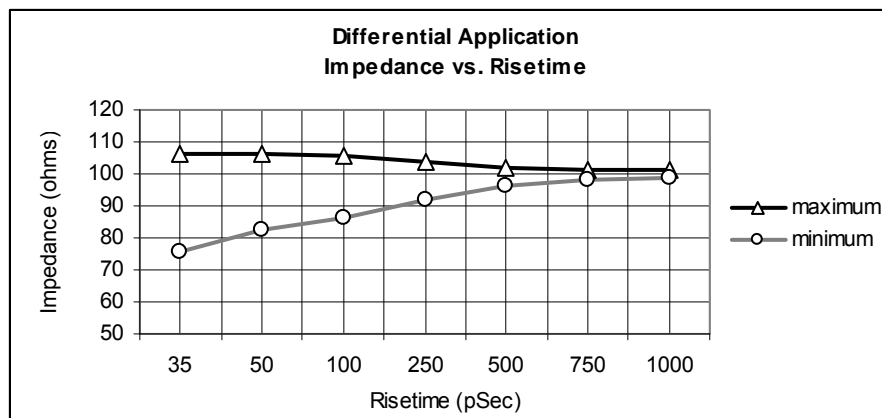


Table 4 - Differential Impedance (Ω)							
Signal Risetime	35±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	106.3	106.1	105.7	104.0	101.9	101.5	101.5
Minimum Impedance	75.9	82.7	86.0	92.2	96.3	98.0	98.8



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Table 5 - Single-Ended Crosstalk (%)										
Input (t _r)	Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns	
N E X T	μp1 to μp3	FTE_40	FTE_44	15.0	13.6	10.2	5.1	2.7	1.9	1.5
		FTE_42	FTE_40	2.7	1.8	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		FTE_7	FTE_8	3.7	2.7	1.9	< 1.0%	< 1.0%	< 1.0%	< 1.0%
F E X T	μp1 to μp5	FTE_40	CLE_44	7.9	5.7	3.7	1.5	< 1.0%	< 1.0%	< 1.0%
		FTE_42	CLE_40	3.2	2.0	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		FTE_7	CLE_8	1.9	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 6 - Differential Crosstalk (%)										
Input (t _r)	Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns	
N E X T	μp1 ⁺ 2 ⁺ to μp3 ⁺ 4 ⁺	FTE_94-92	FTE_90-88	4.5	3.8	2.8	1.6	< 1.0%	< 1.0%	< 1.0%
		FTE_84-86	FTE_90-92	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		FTE_6-4	FTE_3-5	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
F E X T	μp1 ⁺ 2 ⁺ to μp5 ⁺ 6 ⁺	FTE_94-92	CLE_90-88	2.1	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		FTE_84-86	CLE_90-92	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
		FTE_6-4	CLE_3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay			
Configuration		Signal Path	Mated Connector Only
Single-Ended	μp1 to μp8	Tx, port1=FTE_44, Rx, port3=CLE_44	40ps
Differential	μp12 to μp78	Tx, port12=FTE_90-92, Rx, port34=CLE_90-92	39ps

Pin Map (reference Appendix C for full description of test boards)