Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 6mm (0.2365") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω) – SE3, Signal Line 47-53							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	55.3	54.9	54.0	51.4	51.1	51.1	51.1
Minimum Impedance	42.5	45.6	47.5	49.6	50.3	50.4	50.4

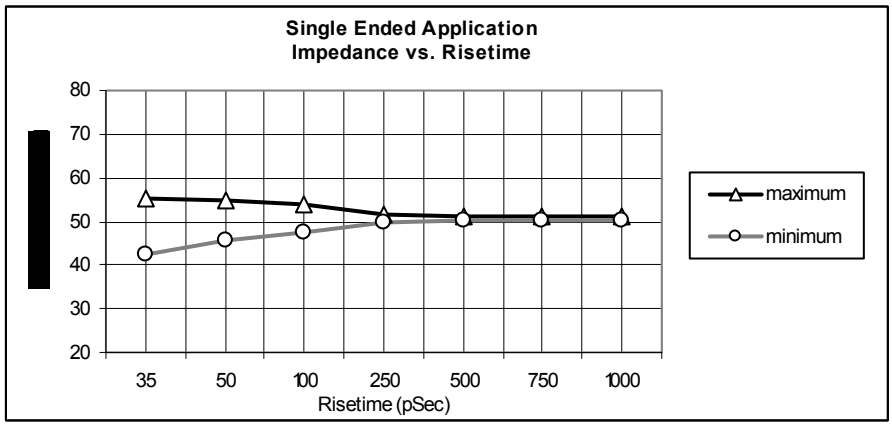
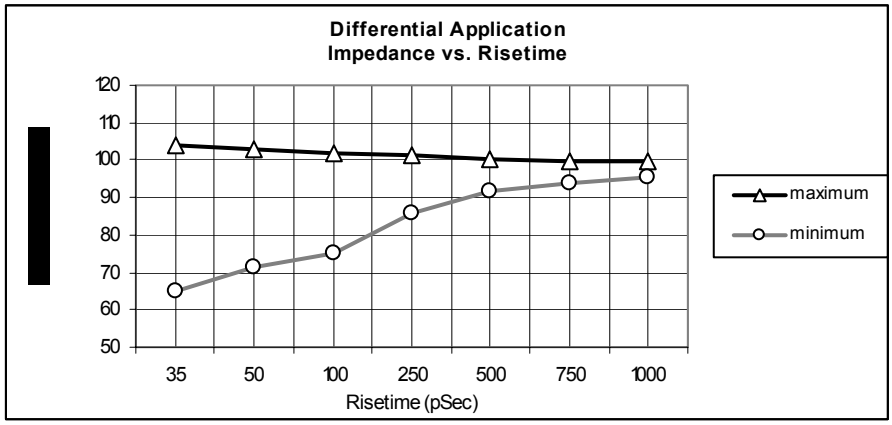


Table 4 - Differential Impedance (Ω) – DP3, Signal Pair 93-95, 5-7							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	103.9	102.9	101.6	101.2	100.4	99.9	99.8
Minimum Impedance	64.8	71.3	75.2	85.9	91.6	94.1	95.5

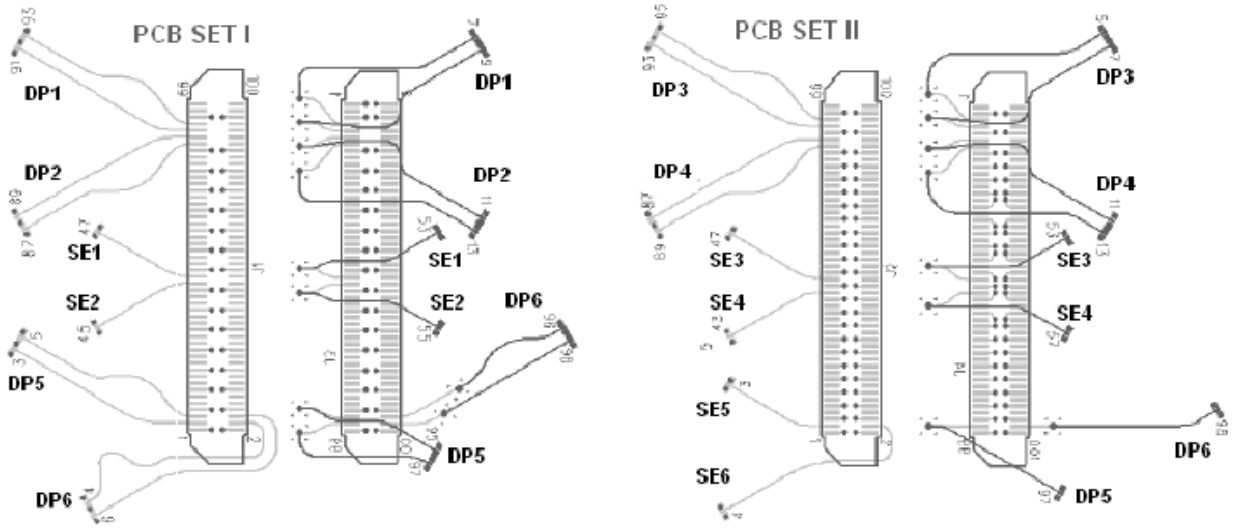


Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 6mm (0.2365") Stack Height

Table 5 - Single-Ended Crosstalk (%)

Input (t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	SE2 to SE1	LSS _45	LSS _47	16.6	15.4	12.6	6.8	3.8	2.7	2.1
	SE4 to SE3	LSS _43	LSS _47	4.5	2.4	1.7	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _3	1.7	1.3	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	SE2 to SE1	LSS _45	LSS _53	5.0	3.2	1.6	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE4 to SE3	LSS _43	LSS _53	4.8	2.8	1.6	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _97	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 6mm (0.2365") Stack Height

Table 6 - Differential Crosstalk (%)

Input(t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	DP2 to DP1	LSS 87-89	LSS 91-93	4.6	4.4	3.8	2.3	1.4	< 1.0%	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 93-95	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DP2 to DP1	LSS 87-89	LSS 7-9	1.8	1.4	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 5-7	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 95-97	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay

Configuration		Signal Path	(Mated Connector Only)
Single-Ended	SE3	LSS; 47 thru LSS; 53	47ps
Differential	DP3	LSS; 93-95 thru LSS; 5-7	49ps

Pin Map (reference Appendix C for full description of test boards)