Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 8mm (0.3150") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω) – SE3, Signal Line 47-53							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	56.3	52.3	52.1	50.7	50.7	50.6	50.6
Minimum Impedance	39.4	42.4	46.0	48.2	49.2	49.6	49.9

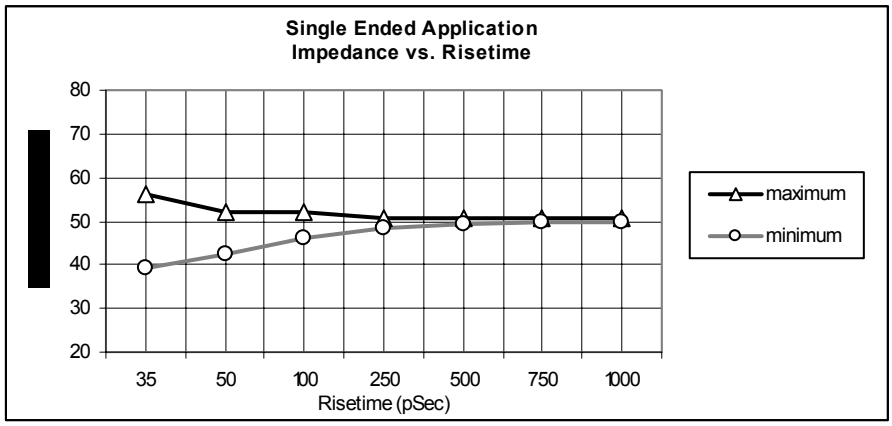
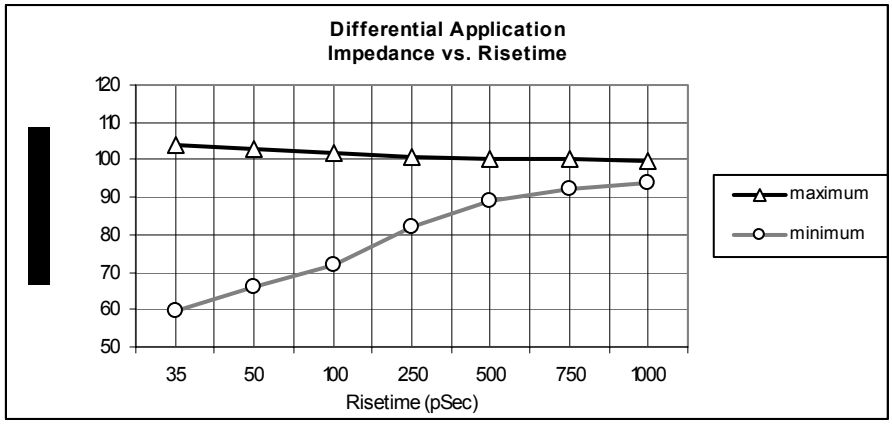


Table 4 - Differential Impedance (Ω) – DP3, Signal Pair 93-95, 5-7							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	103.7	102.8	101.9	100.6	100.3	100.0	99.9
Minimum Impedance	59.7	66.1	71.9	82.1	88.9	92.0	93.9

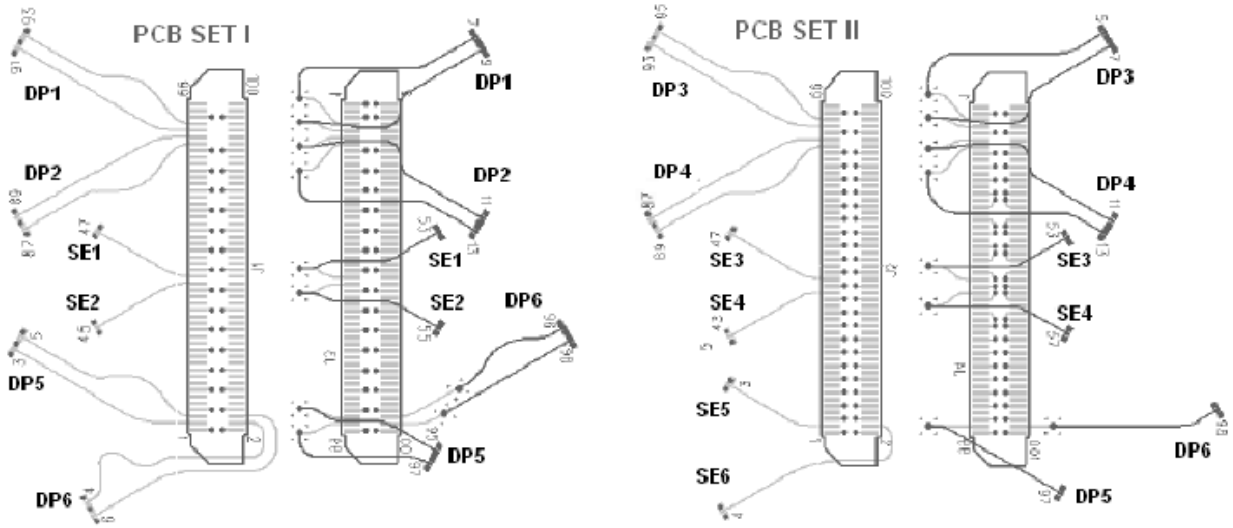


Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 8mm (0.3150") Stack Height

Table 5 - Single-Ended Crosstalk (%)

Input (t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	SE2 to SE1	LSS _45	LSS _47	18.4	16.4	14.3	8.2	4.7	3.3	2.5
	SE4 to SE3	LSS _43	LSS _47	3.6	2.5	1.8	1.1	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _3	1.9	1.5	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	SE2 to SE1	LSS _45	LSS _53	4.9	3.0	2.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE4 to SE3	LSS _43	LSS _53	4.6	2.7	1.5	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _97	1.2	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 8mm (0.3150") Stack Height

Table 6 - Differential Crosstalk (%)										
Input(t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	DP2 to DP1	LSS 87-89	LSS 91-93	5.2	4.9	4.4	2.9	1.7	1.2	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 93-95	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DP2 to DP1	LSS 87-89	LSS 7-9	1.7	1.5	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 5-7	1.0	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 95-97	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay			
Configuration		Signal Path	(Mated Connector Only)
Single-Ended	SE3	LSS; 47 thru LSS; 53	59ps
Differential	DP3	LSS; 93-95 thru LSS; 5-7	66ps

Pin Map (reference Appendix C for full description of test boards)