Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 10mm (0.3937") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω) – SE3, Signal Line 47-53							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	58.2	54.3	53.4	51.5	51.4	51.3	51.2
Minimum Impedance	40.8	43.8	47.6	49.5	50.3	50.4	50.4

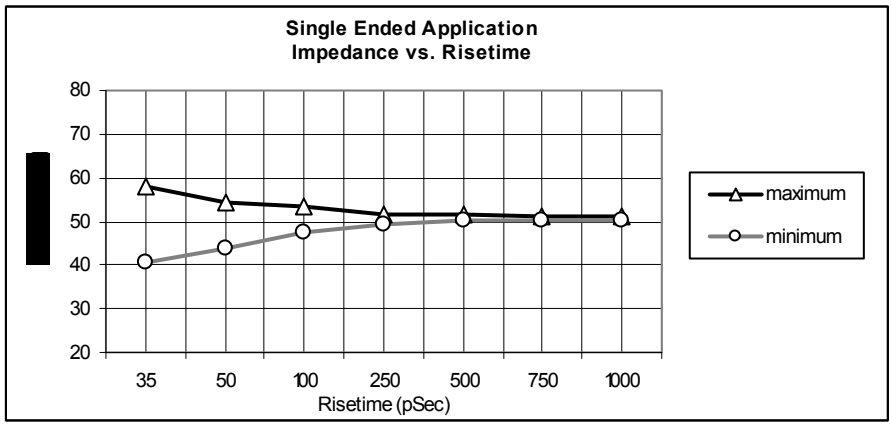
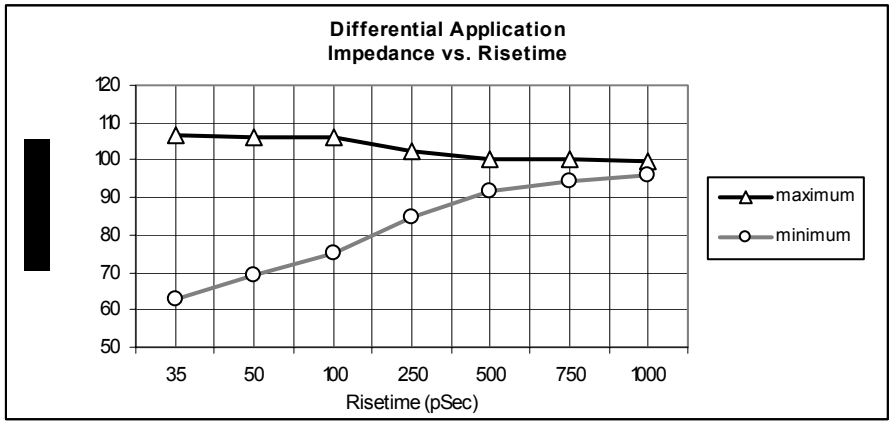


Table 4 - Differential Impedance (Ω) – DP3, Signal Pair 93-95, 5-7							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	106.5	106.3	105.8	102.5	100.3	100.0	99.9
Minimum Impedance	62.7	69.3	74.9	84.5	91.5	94.2	95.7

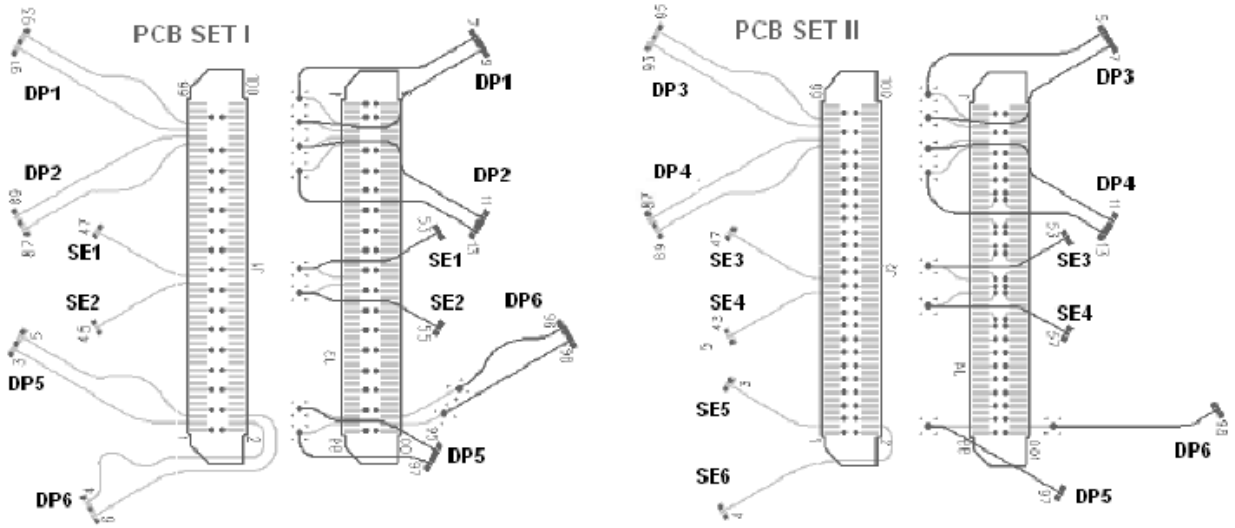


Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 10mm (0.3937") Stack Height

Table 5 - Single-Ended Crosstalk (%)

Input (t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	SE2 to SE1	LSS _45	LSS _47	19.2	17.5	15.5	9.2	5.3	3.7	2.9
	SE4 to SE3	LSS _43	LSS _47	3.4	2.5	1.8	1.2	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _3	1.8	1.6	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	SE2 to SE1	LSS _45	LSS _53	6.0	3.6	2.6	1.1	< 1.0%	< 1.0%	< 1.0%
	SE4 to SE3	LSS _43	LSS _53	4.6	2.6	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _97	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 10mm (0.3937") Stack Height

Table 6 - Differential Crosstalk (%)

Input(t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	DP2 to DP1	LSS 87-89	LSS 91-93	5.5	5.1	4.8	3.2	1.9	1.4	1.1
	DP4 to DP3	LSS 87-89	LSS 93-95	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DP2 to DP1	LSS 87-89	LSS 7-9	2.1	1.6	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 5-7	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 95-97	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay

Configuration		Signal Path	(Mated Connector Only)
Single-Ended	SE3	LSS; 47 thru LSS; 53	65ps
Differential	DP3	LSS; 93-95 thru LSS; 5-7	63ps

Pin Map (reference Appendix C for full description of test boards)