Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω) – SE3, Signal Line 47-53							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	57.1	52.3	52.0	51.2	51.1	50.8	50.7
Minimum Impedance	39.8	42.7	45.2	47.9	49.2	49.8	50.1

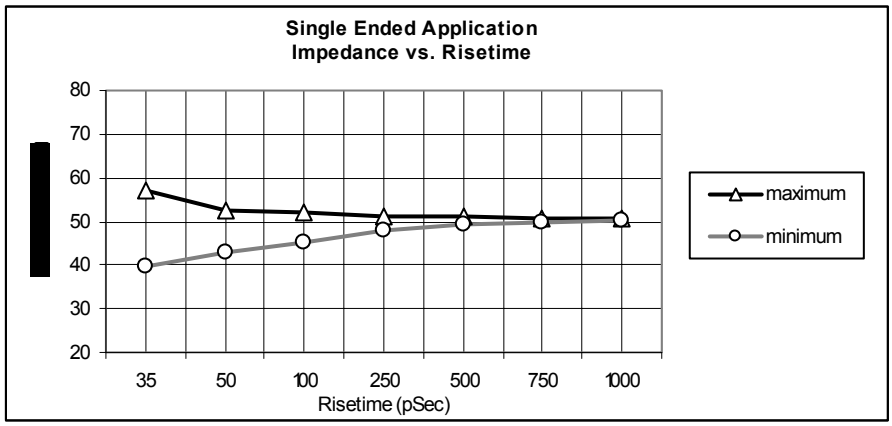
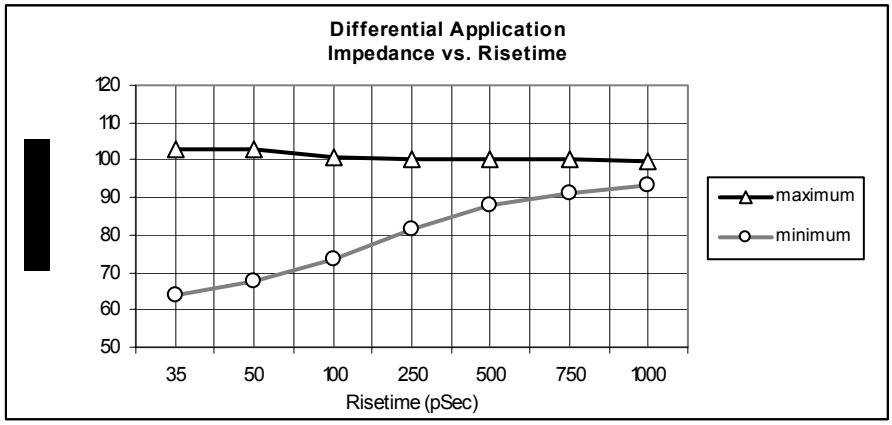


Table 4 - Differential Impedance (Ω) – DP3, Signal Pair 93-95, 5-7							
Signal Risetime	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	103.1	102.9	100.9	100.4	100.2	100.0	99.9
Minimum Impedance	63.8	67.5	73.4	81.4	88.2	91.3	93.2

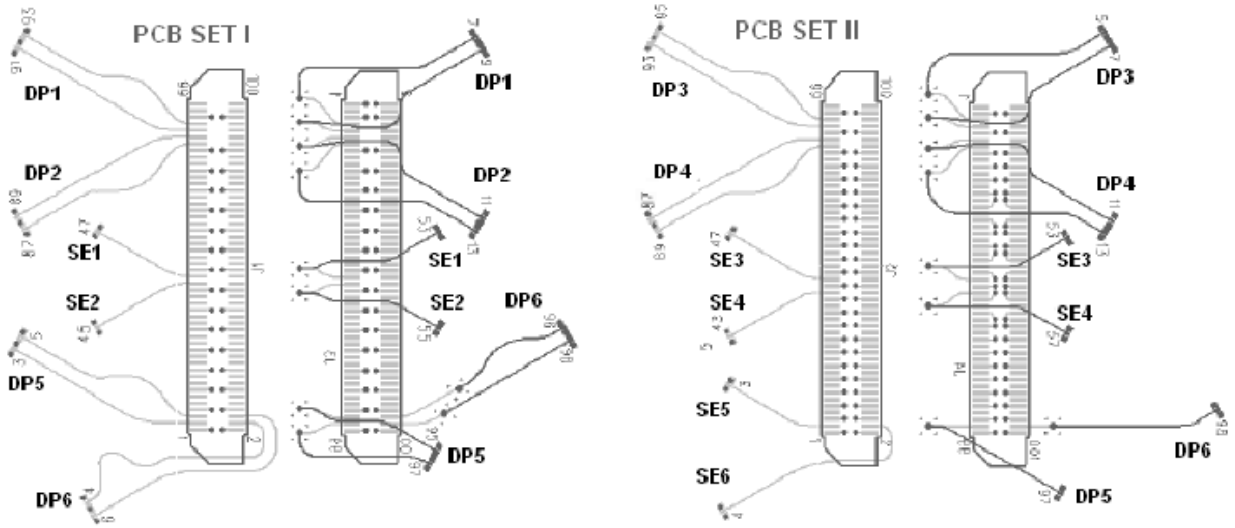


Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

Table 5 - Single-Ended Crosstalk (%)

Input (t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	SE2 to SE1	LSS _45	LSS _47	19.4	17.8	16.6	10.3	6.0	4.2	3.3
	SE4 to SE3	LSS _43	LSS _47	3.3	2.4	1.9	1.2	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _3	1.8	1.6	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	SE2 to SE1	LSS _45	LSS _53	6.3	3.9	2.6	1.2	< 1.0%	< 1.0%	< 1.0%
	SE4 to SE3	LSS _43	LSS _53	4.0	2.3	1.3	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	SE6 to SE5	LSS _4	LSS _97	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Pin Map (reference Appendix C for full description of test boards)



Series: Terminal/Socket LSS Series
Description: 0.635mm (.025") Pitch, 12mm (0.4724") Stack Height

Table 6 - Differential Crosstalk (%)

Input(t_r)		Source	Victim	35±5ps	50ps	100ps	250ps	500ps	750ps	1ns
NEXT	DP2 to DP1	LSS 87-89	LSS 91-93	5.9	5.4	5.1	3.5	2.1	1.5	1.2
	DP4 to DP3	LSS 87-89	LSS 93-95	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 3-5	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	DP2 to DP1	LSS 87-89	LSS 7-9	1.9	1.5	1.4	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP4 to DP3	LSS 87-89	LSS 5-7	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	DP6 to DP5	LSS 4-6	LSS 95-97	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Table 7 - Propagation Delay

Configuration		Signal Path	(Mated Connector Only)
Single-Ended	SE3	LSS; 47 thru LSS; 53	81ps
Differential	DP3	LSS; 93-95 thru LSS; 5-7	78ps

Pin Map (reference Appendix C for full description of test boards)